VHDL. It consists of 4 modules, i.e. Booth Radix-4 mantissa multiplier, normalizer, exponent adder and the signer. Booth radix-4 multiplication is one of the suitable algorithm to be used to design the high speed 24-bit mantissas multiplier because this algorithm is much simpler than the complex Wallace Tree multiplier, thus less gate delay and able to perform such complex multiplication faster. In addition, Booth radix-4 performance is doubled compared to Booth radix-2 that allows high speed multiplication can be achieved. The 32-bit floating point Wallace Tree multiplier operates up to 208.9 MHz with same constrained clock period of 5 ns on Arria II GX FPGA. However, Wallace Tree multiplier consumes more than 90% extra resources compare to Booth radix-4 multiplier to gain only 1% performance improvement. The 32-bit floating point Booth radix-4 multiplier design is a better option because it consumes much lesser resource on FPGA and supports the maximum frequency of 206.14 MHz.

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