Low Power Checks in Multi Voltage Designs

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Abstract: —Leakage power consumption has been almost a serious problem these days in semiconductor industry. Many low power techniques like multi-voltage, power gating etc. are deployed to improve power saving. Power aware verification hence has become a critical issue now. Static low power verification has been developed to verify that low power architectures are designed in correct approach meeting all electrical rules in SoC. The UPF(Unified Power Format) is the standardized format that has all power intent information and can be used throughout the design flow to ensure that the power specification is intact. Firstly, this paper describes the special cells and its operation used in low power techniques. Secondly it describes the major checks examined at each stage using Synopsys VCLP tool and finally debugging with the tool and conclusion.

Key-words – Power domain, UPF, low power cells, electrical connectivity, VCLP, missing special cells, multi-voltage.

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1. Introduction

While wireless devices are rapidly making their way to the consumer electronics market, a key design constraint for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries. So the most important factor to consider while designing SoC for portable devices is 'low power design'.

Growing need for portable communication devices and computing system has increased the need for optimization of power consumption in a chip. Another motivation: some major cells are idle for most of the operating time and some when active might not be critical in terms of timing. Optimization of power should be done at all different stages of VLSI design. While implementing low power techniques at logic synthesis and physical design, several problems arise in implementation. Low power SoC need several implementation level adaptions which uses industry level power format specification known as UPF (Unified Power Format)

Addresing the dynamic or leakage based power consumption using above methods required the use of standard which was different from traditional methods. This lead to development of UPF (Unified Power format), an open standard that allows designers to describe the power design intent. Implementation of design with UPF will cause different issues related to timing, congestion, placement etc. and are dependent on functionality, tech nodes, supply vol etc. Solving this implementation problems requires different methodology to solve each of them

2. Literature Survey

2.1 Power domains and Switching

In multi voltage designs, some domains has switchable supply which are called switchable domains. Power Management Unit is one of the units that controls power up and power down sequences. It toggles the control signals according to power sequence and allows current to the relevant power domains with help of power switches. Main idea of this is turnoff massive unused parts of the design and gain low current consumption.

2.2 Special low power cells

This section explains the working of six special cells used in implementing low power techniques in the design.

2.2.1 Isolation cell

The outputs of powered off domains will be floating as they don't be active. These floating outputs cannot be the inputs of domains which are active. In order to solve this problem, a logic which is used to isolate two power domains is placed when one of them is switching OFF while the other is ON and the signal is going from OFF to ON domains. This isolation cell sends the actual signal to be sent to the ON domain that supposed to go from OFF domain and make sure active domains are no affected. Lack of isolation cell passes unknown signal (X) and causes leakage of power. If the signal passed is to be 1, then OR gate with one input as '1' acts as isolation here. Similarly if '0' to passed, then AND gate acts as isolation. There is one more type of isolation cell which is of latch type. Latch stores the outputs of power off domains and

Schematic - Debugging in VCLP

With VCLP tool, we can easily trace the driver and load information when violations show up the at the domain boundary, in addition all low power related information is shown in the interface. The connectivity information is shown on the left side and low power property of the violation on right side.

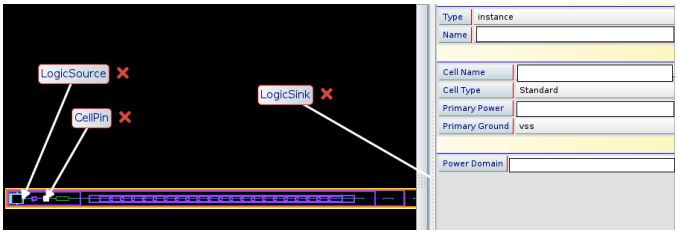

Fig 8.1 Debugging in VCLP

The violations flagged out in our deisgn are as follows. We debugged each violation and tried to lessen the electrical violations in the design.

Management Summary

Stage	Family	Errors	Warnings	Infos	Waived
UPF	Isolation	117	2	0	0
UPF	LevelShifter	29	3	20	0
UPF	UpfConsistency	4	0	0	12
Design	Isolation	91	2	0	0
Design	LevelShifter	186	8	0	0
Total		427	15	20	12

Fig 8.2 Management summary - list violations of all special cells

Tree Summary

Severity	Stage	Tag	Count	Waived
error	UPF	ISO_STRATEGY_IGNORED	110	0
error	UPF	ISO_STRATEGY_MISSING	7	0
error	UPF	LS_STRATEGY_MISSING	29	0
error	UPF	LS_SUPPLY_UNAVAIL	4	0
error	UPF	UPF_SUPPLY_NOSTATE	0	12
error	Design	ISO_BUFINV_STATE	79	0
error	Design	ISO_INST_MISSING	7	0
error	Design	ISO_SINK_STATE	5	0
error	Design	LS_INST_MISSING	186	0
warning	UPF	ISO_STRATCONTROL_GLITCH	2	0
warning	UPF	LS_SCMR_MIXED	3	0
warning	Design	ISO_CONTROL_GLITCH	2	0
warning	Design	LS_LOCATION_WRONG	8	0
info	UPF	LS_MAP_MISSING	20	0
Total			462	12

Fig 8.3 Tree summary – detail each violation

```
Tag             : RAIL_BUFINV_STATE
Description     : Supply off for buffer/inverter [Instance], but sink
                  [LogicSink] supplies on
Violation       : LP:3446
Instance        : BUF_inst_4
Cell            : M10S31_BUFX4
CellPin         : o
EndOfChain      : BUF_inst_1/o
LengthOfChain   : 1
LogicSource
  PinName       : AON_reg_387/q
LogicSink       : AON_phy_top_inst/i_standby
```

Fig 8.4 Detail information about the violation

9 Conclusion

Power aware verification is very well necessary for today's designs. Working and usage of special cells in low power design are explained. And also how the VCLP tool carry out the checks are illustrated. With the help of Synopsys VCLP, we have performed the low power checks in our design and mentioned the challenges we faced with design.

10 References

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