Performance Analysis of Single Event Double Upset Immune D and S-R Flip flops

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Abstract: - The presence of radiation in space environment causes effects in modern electronic devices. This effects range from degradation of performance to functional failures. One of the radiation effects is SEE (Single-event effects). This work presents a design of D and S-R flip flop as variant of the Dual Interlocked storage Cell (DICE) which is tolerant to a single event double upset (SEDU). The design is referred to as modified transistor DICE (TDICE) which uses PMOS and NMOS transistors as a feedback transistors to block the paths that connect a node to the next node. The use of these transistors hardens the cell to tolerate a single event double upset with critical charge at a large value. Extensive simulation results are provided to assess modified TDICE with respect to traditional circuit figures of merit such as number of transistors, power consumption, and delay. The simulation results show the expense of an increased area for the additional transistors, modified TDICE shows a nearly complete tolerance to a single event double upset. All the simulations are done using Tanner EDA tool with 65nm technology.

Key-Words: - D flip flop, DICE, SET, SEU, S-R flip flop, Tanner EDA tool.

1 Introduction

In nanoscale CMOS technology, by means of shrinking transistor feature size and reducing supply voltage, very large scale integration performance is significantly improved. However, the capacitance on a circuit node is aggressively decreased. As a result, the logic state of a node can be easily disturbed when the charges generated by particle striking in silicon are collected by drain diffusion. Hence, the radiation-induced single event effects such as single event transient (SET) or single event multiple-transient in combinational logic blocks and single event upset (SEU)/single event double-upset (SEDU) in memory elements (latches, flip-flops etc.) are becoming increasingly serious with technology evolution [1-2]. Recently researchers have identified SEU and SEDU as notable threats to the operations of terrestrial advanced electronic devices. A number of schemes making a very important contribution to SEU mitigation [3]. These schemes make use of interlocked hold nodes or dual modular redundancy to correctly retain data. However, due to nanoscale CMOS technology, multiple-node charge collection-induced SEDU is becoming more prominent especially in harsh radio-active environments and soft error rate resulting from SEDU is rising. Consequently, existing SEU tolerant latch designs are no longer robust facing to SEDU, and cannot be used in systems requiring high reliability. To overcome this limitation, modified Transistor DICE (TDICE) has been introduced [4] which is a modified structure of TDICE [5].

Latches and flip flops are storage elements used to store one bit information. If a radiation strikes on any one of the internal nodes, it may cause data stored in the latch/flip flop to flip. The solution to this problem is Dual interlocked storage cell (DICE) which eliminates SEU, but it is not tolerant to SEDU [6-7]. To achieve better tolerance against SEDU, we go for modified Transistor DICE (TDICE) based latches and flip flops.

The aim of this work is to design a multiple upset immune flip flops (D & SR) which are having high robustness against SEU and SEDU. The performance of these flip flops are also analyzed in terms of the no. of transistors, power, and delay using Tanner EDA tool for 65nm CMOS technology.

2 SET Immune flip flop topologies

2.1 D Flip flop Design

The simplest way to build a flip-flop is by using two latches in a 'Master-Slave' configuration. The Master-Slave D-flip flop memory cell, shown in Fig. 1, is an electronic device that can be used to store one bit of information.

A D flip flop takes only a single input, the D (data) input. The master-slave configuration has the advantage of being edge-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output. The circuit consists of two D latches connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state. When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state. The result is that output can only change state when the clock makes a transition from high to low [8-9].

The Master slave D-flip flop can either have D as 0 or 1. The Flip flop has only two inputs: D (data) and Clk (clock). If master runs with clock, then it's a negative edge triggered. If master runs with clock bar, then it's a positive edge triggered. The operation of Master slave D flip flop is described below:

- When clock is set to be positive edge triggered (low to high), input D sets to zero and output Q will be zero and $\bar{Q}$ will be one for a one complete clock cycle
- When clock is set to be positive edge triggered (low to high), input D sets to one and output Q will be one and $\bar{Q}$ will be zero for a one complete clock cycle
- When clock is set to be negative edge triggered (high to low), input D sets to zero and output Q will be zero and $\bar{Q}$ will be one for a one complete clock cycle
- When clock is set to be negative edge triggered (high to low), input D sets to one and output Q will be one and $\bar{Q}$ will be zero for a one complete clock cycle

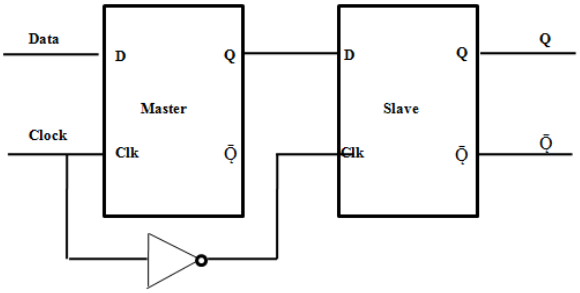

Fig. 1 Master Slave D-flip flop

When clock is set to be one or zero, then output will retains the previous state

2.2 Modified Transistor DICE D Flip flop Design

Modified Transistor DICE D-flip flop is designed to achieve better tolerance against SEDU which is shown in Fig. 2. Modified TDICE D-flip flop uses both PMOS and NMOS transistor as the feedback transistors.

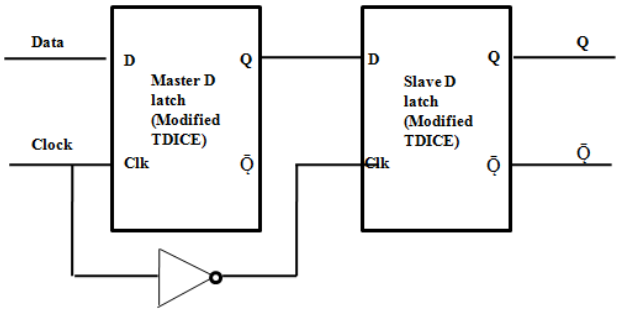

Fig. 2 Modified TDICE D-flip flop

2.3 SR-Flip flop Design

Master-Slave configuration of SR flip flop is shown in Fig. 3. In this configuration, one latch serves as the master receiving the external inputs and the other as a slave, which takes its inputs from the master. When the clock pulse goes high, information at S and R inputs is transmitted to master. The slave flip-flop however remains isolated since its control input is 0. Now when the clock pulse returns to '0', the master gets disabled and blocks the external inputs to get to its outputs whereas slave gets enabled and passes the latched information to its outputs [10].

The latch has only three inputs: Clock, S (Set) and R (Reset).The SR latch circuit has two complementary outputs, Q and $\bar{Q}$. The operation of SR-latch is described below:

- When clock is set to high ,both inputs S and R are set to logic '1', then the SR latch will be forced to logic '1' which conflicts with the complementary of Q and $\bar{Q}$ (not allowed condition)
- When Clock is set to high, inputs S = 0 & R = 1, then the latch is said to be in set state (Q = 1 & $\bar{Q}$ = 0)
- When Clock is sets to high, inputs S = 1 & R = 0, then the latch is said to be in reset state (Q = 0 & $\bar{Q}$ = 1)
- When Clock is set to high , both inputs S and R are set to logic '0', the SR latch will retains its previous state
- When Clock is set to low, then output will retains its previous state whether inputs are in 0 or 1

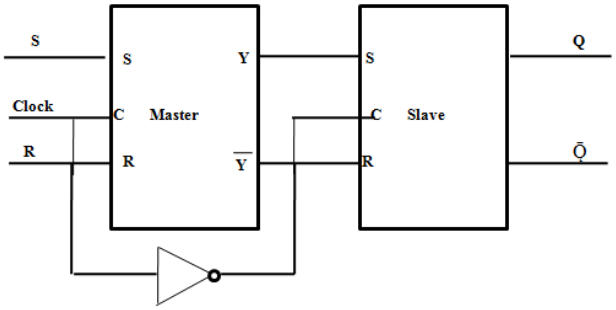

Fig. 3 SR-flip flop memory cell

2.4 Modified Transistor DICE SR Flip flop Design

Modified Transistor DICE SR flip flop is designed to achieve better tolerance against SEDU is shown in Fig. 4. Modified TDICE SR flip flop uses both PMOS and NMOS transistor as the feedback transistors [4].

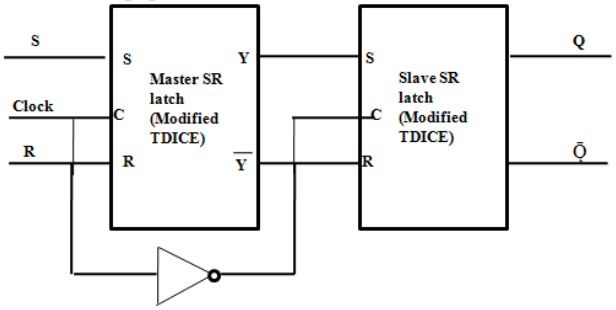

Fig. 4 Modified TDICE SR flip flop

2.5 Modeling of Single Event Transient (SET)

In a memory cell such as latch, when deposited charge by a particle strike in the struck node is greater than the critical charge of that node, an SEU will takes place [11]. Critical charge for a node in a storage cell is defined as the minimum charge needed to alter the stored value of the storage cell when deposited in that node [12].

To model the injection of a particle strike and its associated deposited charge, we use double exponential current source model which is given in the following equation [7].

$$I(t) = \frac{Q}{(\tau_a - \tau_b)}\left[e^{\left(\frac{-t}{\tau_a}\right)} - e^{\left(\frac{-t}{\tau_b}\right)}\right] \quad (1)$$

Where Q - amount of charge deposited as a result of the ion strike

τ_a- the collection time constant for the junction

τ_b - the ion track establishment constant

I(t) - amount of injected charge

For 65nm technology, SET modeling parameters [13] are Q = 24fC, τ_a =145ps, τ_b = 45ps. The graph is shown in Fig. 5.

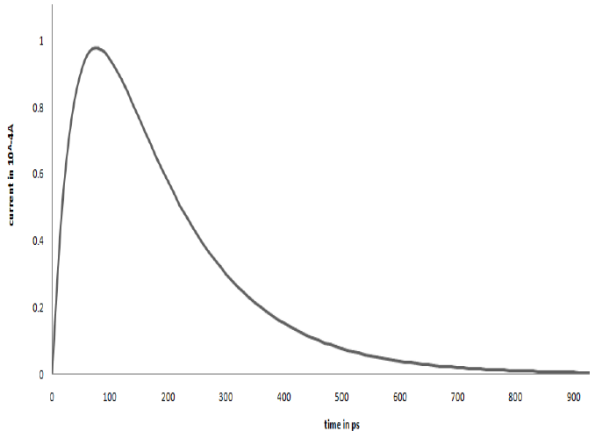

Fig. 5 SET current model for 65nm

3 SEU Results and Discussion

3.1 Impact of SEU in D-Flip flop

Figure 6 shows the realization D-flip flop design. The transient output of D flip flop for 65nm is shown in Fig. 7.

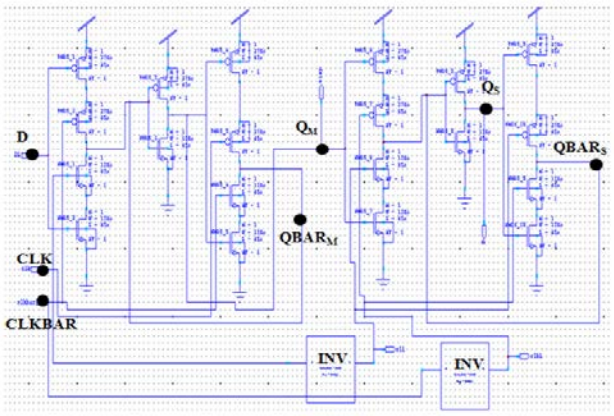

Fig. 6 Structure of D-flip flop

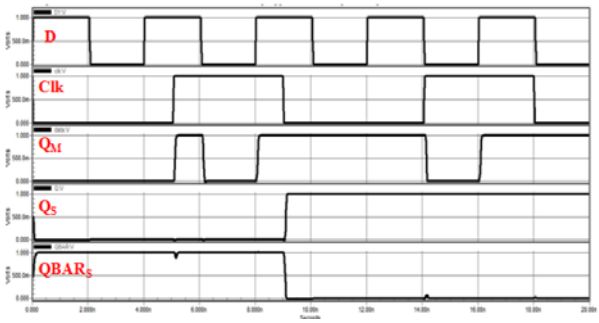

Fig. 7 Transient outputs of D-flip flop

In D-flip flop, there are four storage nodes. An incoming radiation particle strike on any OFF transistor may cause a single event transient (SET) pulse to be generated. The SET pulse causes a flip flop upset if it is able to propagate through the feedback loop of the cell. Hence the necessary condition for an upset is: SET pulse width to be greater than the feedback loop delay. The drawback of D-flip flop is sensitive to SEU.

The impact of single event upset (SEU) in storage node of D-flip flop is shown in Fig. 8 which shows D-flip flop is sensitive to SEU.

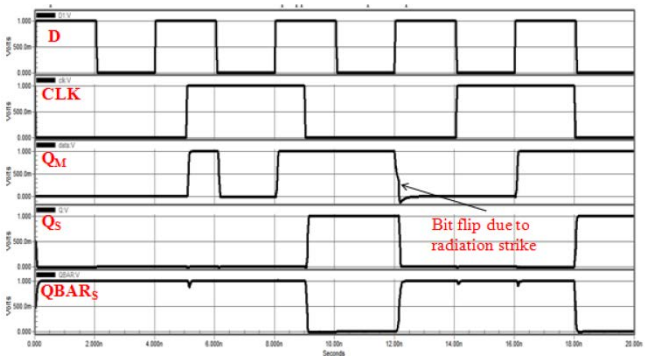

Fig. 8 SEU response of D-flip flop at node Q_M

3.2 Impact of SEU in Modified TDICE D-Flip flop

The structure of modified TDICE D-flip flop is shown in Fig. 9. The transient output of modified TDICE D flip flop is shown in Fig. 10.

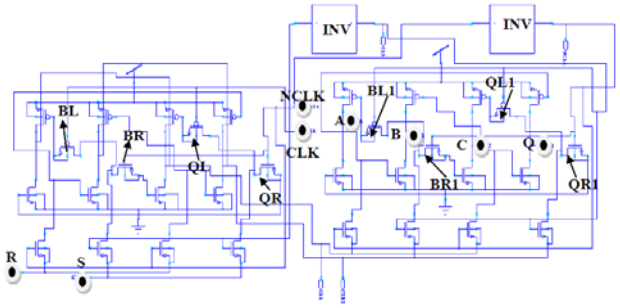

Fig. 9 Structure of Modified TDICE D-flip flop

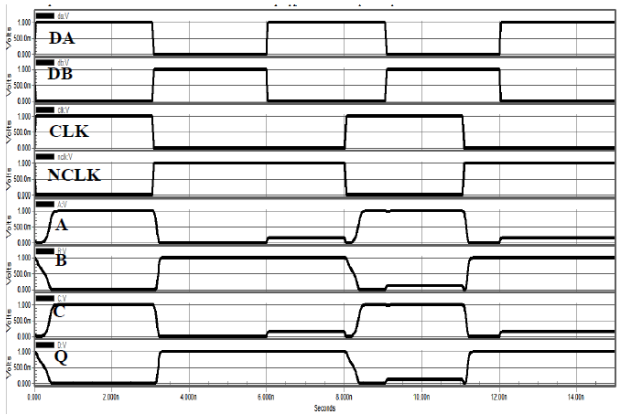

Fig. 10 Transient response of Modified TDICE D flip flop

When there is a single event strike on node C, the induced SET pulse may flip one adjacent node (B or Q). However, the incorrect logic value at this adjacent node is not able to propagate because of the off-state clocked transistors. Once the charge injected to C is removed by the on-state transistors, all nodes return to their original states. The same analysis applies to node A as well.

If node B is struck, the voltage glitch at this node cannot propagate to other nodes because both of the feedback transistors (BL and BR) connected to this struck nodes are turned OFF. The deposited charge will eventually be removed and the state of the hit node will be recovered. This is the same thing for node Q.

Striking one of the additional four nodes BR, BL, QR, and QL does not flip the cell. For example, in one state (A B C Q = 1 0 1 0), the logic values of BR, BL, QR, and QL are logic 0. If node BL sees a positive SET, node A float by turning off P1, and therefore, this will not change the logic state of A.

The impact of single event upset (SEU) at node C is shown in Fig. 11 and the same analysis is done for node A which leads the nodes to insensitive.

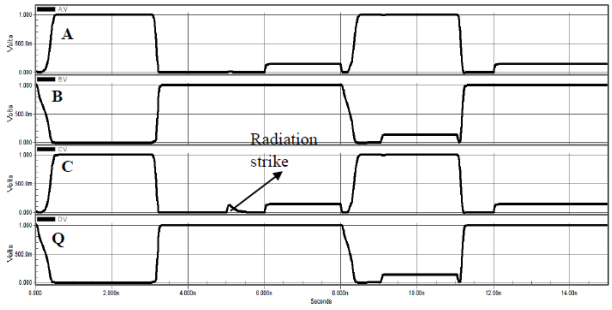

Fig. 11 SEU analysis of Modified TDICE D flip flop at node C

The impact of single event upset (SEU) at node B is shown in Fig. 12 and the same analysis is done for node D which leads the nodes to insensitive. From this result, we conclude that Modified TDICE D flip flop is immune to SEU.

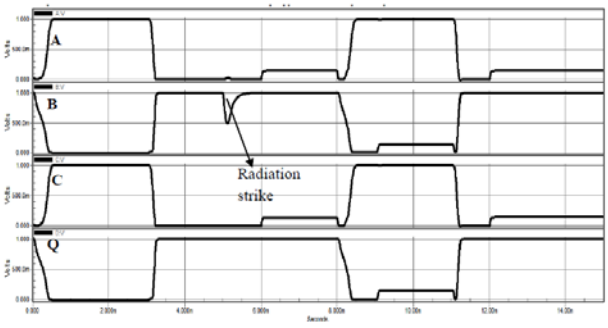

Fig. 12 SEU output of Modified TDICE D flip flop at node B

3.3 Impact of SEDU in Modified TDICE D-Flip flop

In one state (A, B, C, Q = 1, 0, 1, 0), when two transistors P2 and P4(node A and C) are hit simultaneously that causes both alternate nodes (B and Q) to observe positive SET transients, but B and Q are not able to propagate. Since the logic state of A is determined by uncorrupted nodes BL and QR, and the state of C is determined by uncorrupted nodes QL and BR. So, A and C do not flip; and B and Q will then recover.

If node C sees a positive SET pulse and node QL sees a negative SET pulse at the same time, node A will not be able to recover because node QL turns OFF P3 and cuts off the conduction path of node C to the supply rail. As a consequence, node Q may also flip depends on the strength of P4. The only sensitive node pair is QR & C.

The impact of single event double upset (SEDU) at node A and Q is shown in Fig. 13 and the same analysis is done for other node pairs (like node C and A in Fig. 14) which leads the nodes to insensitive.

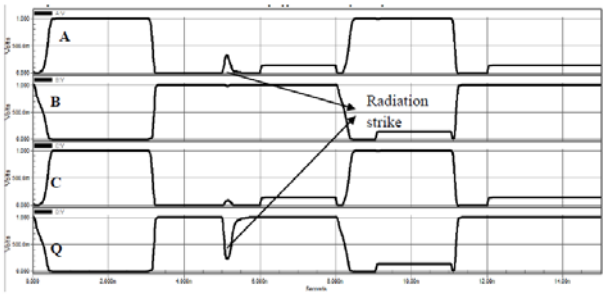

Fig. 13 SEDU output of Modified TDICE D-flip flop at node A and Q

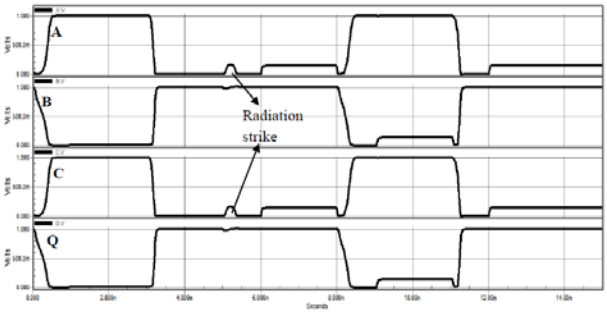

Fig. 14 SEDU output of Modified TDICE D-flip flop at node C and A

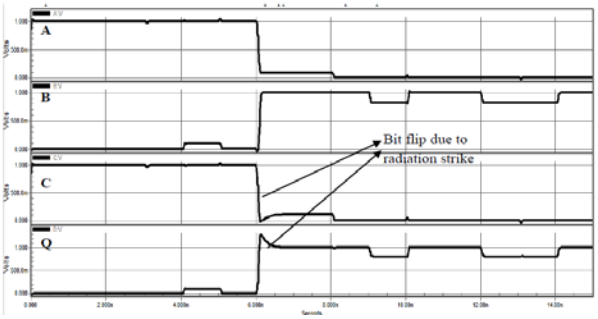

Fig. 15 SEDU output of Modified TDICE D flip flop at node QR and C

The conclusion of this design has four sensitive node pairs, example is shown in Fig. 15. If this node pairs is removed, then the modified TDICE D flip flop design is expected to have better SEU performance.

3.4 Impact of SEU in SR-Flip flop

SR-flip flop is used as storage elements to store one bit of information. Figure 16 shows the structure of SR flip flop design. The transient output of SR flip flop design for 65nm is shown in Fig. 17.

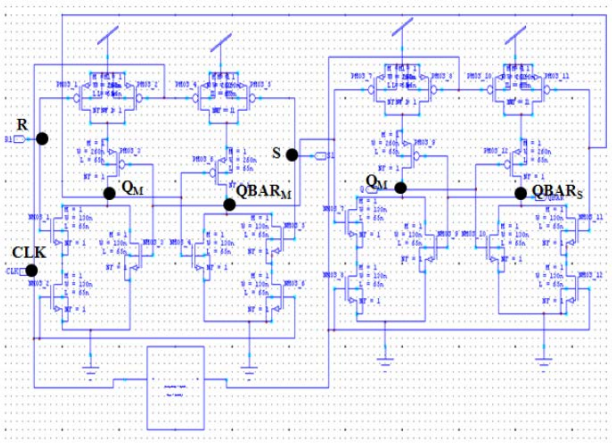

Fig.16 Structure of SR flip flop

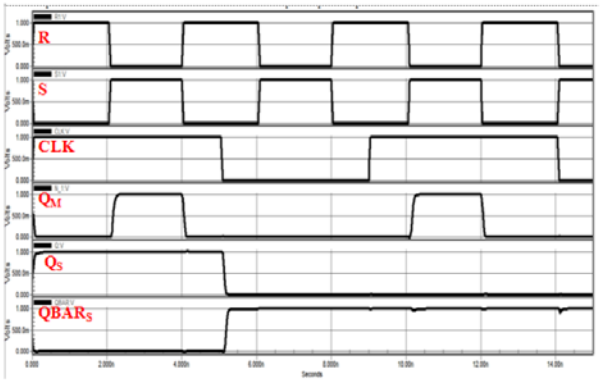

Fig. 17 Transient output of SR-flip flop

In SR-flip flop, there are four storage nodes. An incoming radiation particle strike on any OFF transistor may cause a single event transient (SET) pulse to be generated. The SET pulse causes a latch upset if it is able to propagate through the feedback loop of the cell. Since the SR-latch contains only two storage nodes, even one node could collect enough charge (greater than the critical charge of the node) to generate the SET pulse with the required pulse width to cause a cell upset. The drawback of SR-flip flop is sensitive to SEU.

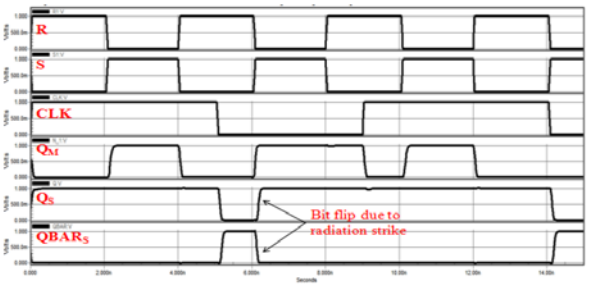

Fig. 18 SEU Output of SR-flip flop at node $QBAR_M$

The impact of single event upset (SEU) in storage node is shown in Fig. 18 which shows SR flip flop is sensitive to SEU.

3.5 Impact of SEU in Modified TDICE SR-Flip flop

Modified Transistor DICE (TDICE) SR flip flop is designed to achieve better tolerance against SEDU is shown in Fig. 19. Modified TDICE SR flip flop uses both PMOS and NMOS transistor as the feedback transistors. The transient output of modified TDICE SR- flip flop design for 65nm is shown in Fig. 20.

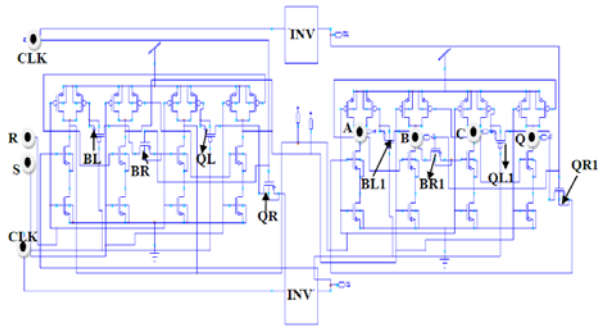

Fig. 19 Structure of Modified TDICE SR-flip flop design

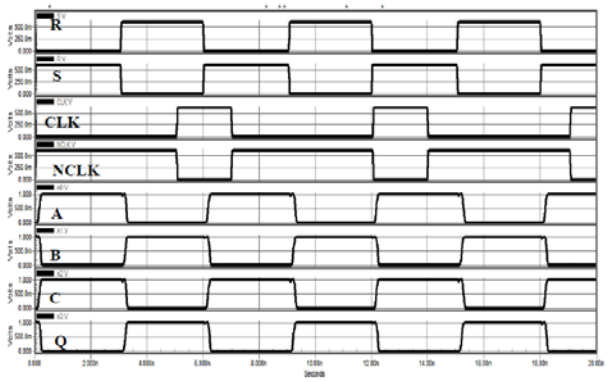

Fig. 20 Transient output of Modified TDICE SR-flip flop

When there is a single event strike on node A, the induced SET pulse may flip one adjacent node (B or Q). However, the incorrect logic value at this adjacent node is not able to propagate because of the off-state clocked transistors. Once the charge injected to A is removed by the on-state transistors, all nodes return to their original states. The same analysis applies to node C as well.

If node B is struck, the voltage glitch at this node cannot propagate to other nodes because both of the feedback transistors (BL1 and BR1) connected to this struck nodes are turned OFF. The deposited charge will eventually be removed and the state of the hit node will be recovered. This is the same thing for node Q.

Striking one of the additional four nodes BR, BL, QR, and QL does not flip the cell. For example, in one state (A B C Q = 1 0 1 0), the logic values of BR, BL, QR, and QL are logic 0. If node BL sees a positive SET, node A float by turning off P1, and therefore, this will not change the logic state of A.

The impact of single event upset (SEU) at node A is shown in Fig. 21 and the same analysis is done for node C which leads the nodes to insensitive.

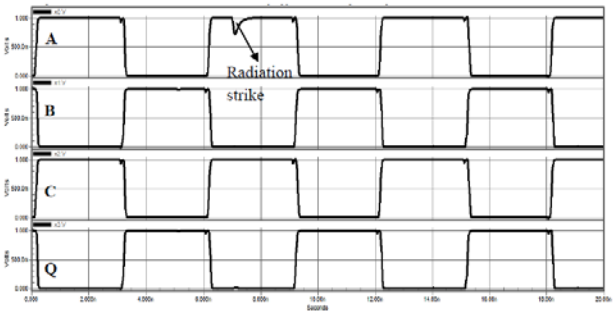

Fig. 21 SEU output of Modified TDICE SR flip flop at node A

The impact of single event upset (SEU) at node B is shown in Fig. 22 and the same analysis is done for node Q which leads the nodes to insensitive. From this result, we conclude that Modified TDICE SR-flip flop is immune to SEU.

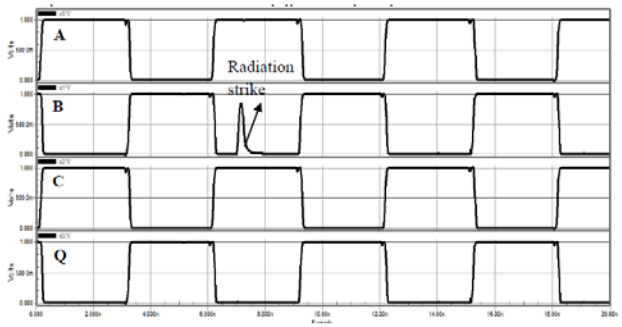

Fig. 22 SEU output of Modified TDICE SR-flip flop at node B

3.6 Impact of SEDU in Modified TDICE SR-Flip flop

In one state (A, B, C, Q = 1, 0, 1, 0), when two transistors P2 and P4(node A and Q) are hit simultaneously that causes both alternate nodes (B and C) to observe positive SET transients, but B and Q are not able to propagate . Since the logic state of A is determined by uncorrupted nodes BL and QR, and the state of Q is determined by uncorrupted nodes QL and BR. So, A and Q do not flip; and B and C will then recover.

If node Q sees a positive SET pulse and node QL1 sees a negative SET pulse at the same time, node A will not be able to recover because node QL1 turns OFF P3 and cuts off the conduction path of node Q to the supply rail. As a consequence, node B may

also flip depends on the strength of P2. The only sensitive node pair is QL1, Q.

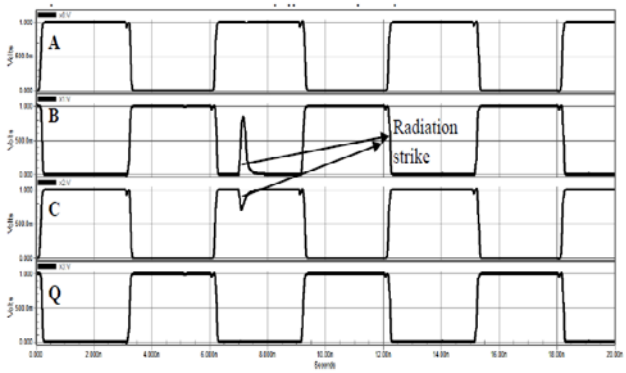

Fig. 23 SEDU output of Modified TDICE SR-flip flop at node C and B

The impact of single event double upset (SEDU) at node B and C is shown in Fig. 23 and the same analysis is done for other node pairs (like node A and Q in Fig. 24) which leads the nodes to insensitive.

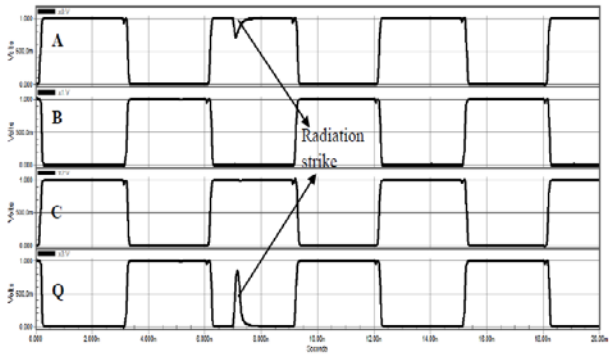

Fig. 24 SEDU output of Modified TDICE SR-flip flop at node A and Q

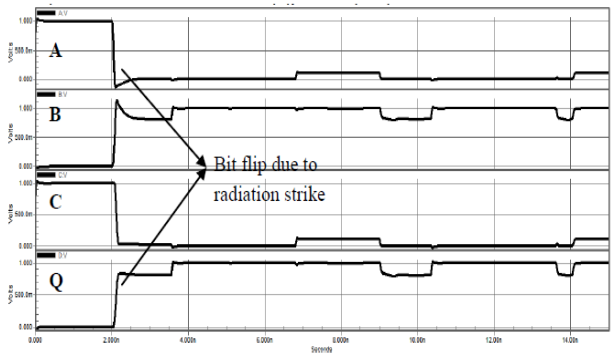

Fig. 25 SEDU output of Modified TDICE SR-flip flop at node QL1 and Q

The conclusion of this design has six sensitive node pairs, example is shown in Fig. 25. If this node pairs is removed, then the modified TDICE SR-flip flop design is expected to have better SEU performance.

The performance of D flip flop and SR flip flop topologies are compared in Table 1.

Table 1 Performance analysis of D-flip flop and SR-flip flop topologies

Topologies (65nm)	**No. of Transistors**	**Power (µw)**	**Delay (ps)**
D-flip flop	22	4.16	182.32
Modified TDICE D-flip flop	42	5.49	235.47
SR-flip flop	26	4.65	204.57
Modified TDICE SR-flip flop	44	5.92	261.93

4 Conclusion

Technology scaling brings more serious challenges to IC reliability issues, one of which is the SEU/SEDU induced soft error in memory elements (latch or flip flop). A memory cell like D & SR flip flops are not immune to single event upset (SEU). To improve SEU ,we go for Dual interlocked storage cell (DICE) but it's not tolerant to single event double upset (SEDU).To achieve better SEDU tolerance, we used modified TDICE D & SR flip flops and calculated their performance parameters such as number of transistors, power and delay. The modified flip flops (D & SR) have SEU tolerance with design overhead in terms of number of transistors, power and delay than conventional one. Simulations have been done in 65nm CMOS technology using Tanner EDA tool.

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