Design and Simulation of First Order One Bit Sigma Delta ADC in 180nm CMOS Technology

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Abstract: - Sigma Delta ADC includes OP-AMP integrator, comparator and d flip-flop. Smoothing operation of OP-AMP integrator with sufficient gain and stability plays a significant role in Sigma Delta ADC for high frequency applications. Low power, Low cost comparator is demanded circuit in a market due to resolution of ADC converter depends on the comparator. Speed and variability of D flip-flop are required in sigma delta ADC to count the number of pulses after comparator. Hence this paper proposed modified zero cancelling method for stability and gain of OP-AMP integrator .This is achieved by modified biasing circuit of series feedback transistor. Resolution of ADC converter is prominently depend on comparator design. Modified comparator circuit appropriates for enhancing gain and for getting low power circuit due to proper biasing of transistor. The paper also aims to simulate Sigma delta ADC using single phase clocked feedback D flip-flop. Sigma Delta ADC is simulated in 180nm CMOS technology in Electric VLSI CAD Tool and TSMC BSIM3 is used as a model library. Supply voltage is 1.8v at 27◦ c temperature and Unity Gain Bandwidth (UGB) =5MHz.
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Key-Words: - OP-AMP, Stability, gain, Comparator, D flip-flop, ADC

1 Introduction

Sigma delta ADC is widely used in many applications like VLC (visible light communication), Gyroscope etc. The need has arisen to do smooth operation of OP-AMP integrator in sigma delta ADC for high frequency. Sigma delta ADC includes Integrator, comparator, DAC and D flip-flop as shown in Fig.1. Comparator switches the output from the positive to negative levels.DAC converts the digital output into the corresponding analog levels to find out the difference between the input signal and analog feedback signal. Main issue in OP-AMP as an integrator design is stability due to open loop poles shows that Fig.2. Integrator is used to integrate the difference signal. Although gain enhancement is possible by cascading of stages, Cascading of stages add poles. Addition of poles means effort for stability improvement. Further Cascade configuration of OP-AMP also strongly affects the output swing. So there is restriction on the several stages .The Design is expected with efficient stability and largest gain in order to integrate high clock frequency signal. In this paper, OP-AMP open loop and close loop configuration is introduced with modified structure to enhance gain. Stability is also achieved with modified zero cancelling method. Compensation is not required in comparator due to rail to rail operation of comparator. In sigma delta ADC, after comparator D flip-flop is used to count the number of pulses. Circuit with minimum transistor is required to accomplish this demand. Consequently, single phase clocked feedback D flip-flop is also introduced [1, 2].

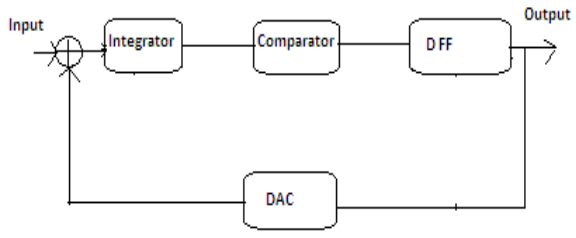

Fig.1 Basic blocks of Sigma Delta ADC

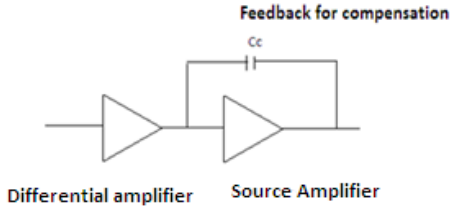

Fig.2 Basic blocks of CMOS OP-AMP

2 Integrator

One stage OPAM limits the gain and a cascade of stages limits the stability. Optimum choice is two stages OP-AMP [3]. Performance of two stages OP-AMP is not enough for sigma delta ADC. Also, it is unstable by connecting two stages together.

2.1 Stability of OP-AMP

Stability is always measured by phase margin means phase shift at unity gain [5].

Phase margin=180◦ + < A (j ω) (1)

Where < A (j w) is the unity gain phase shift and ω is unity gain frequency.
Two stages OPAM introduce poles. These poles shift negative phase shift towards -180◦ earlier than unity gain frequency. Unfortunately, it causes the circuit to oscillate. Hence there is need of compensation to increase phase margin and to stabilize the close loop response of the circuit [8, 15].

2.2 OP-AMP with Miller Compensation

According to Barkhausen's criteria, critical point is nothing but magnitude is equal to one for stability and phase is equal to -180◦.What is more , gain cross over must be well before phase cross over for stability . In miller compensation, pole splitting is achieved by connecting a capacitor in feedback from the output terminal to the input terminal of the second stage. However it introduces right half plane zero, which is located at $Z = \frac{\text{gm1}}{\text{Cc}}$ .This RHP zero decreases phase. It is possible to move RHP zero in left plan or eliminate .Desirable phase margin in this type of OPAM integrator is at least 45◦ .Two stage OP-AMP integrator with miller compensation is shown in Fig.3 [14].

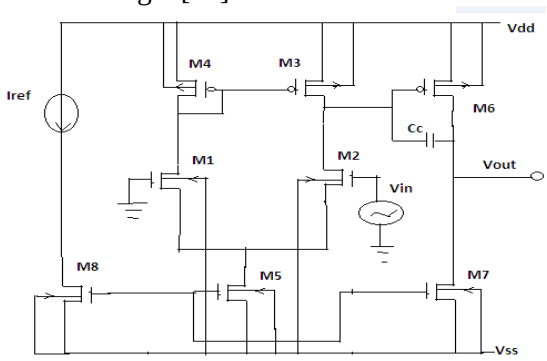

Fig.3 Two stage OP-AMP with Miller Capacitor

2.3 Stability Techniques

Small Signal Model-

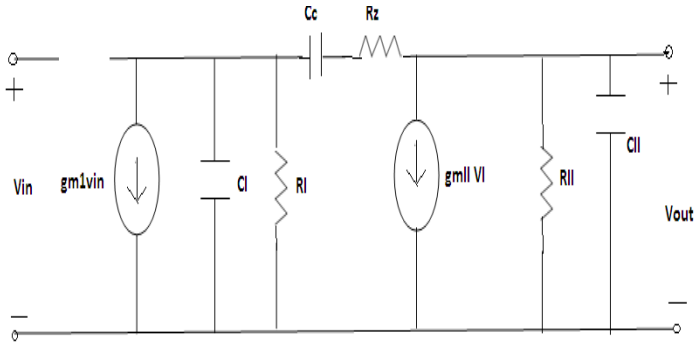

Fig.4 Two stage OP-AMP with indirect compensation

Small Signal Analysis of two stages OP-AMP with miller compensation is shown in Fig.4.

Output equation is,

$$\frac{Vout(s)}{Vin(s)} = \frac{a[1-s\left(\frac{Cc}{gmII}-RzCc\right)]}{1+bs+cs^2+ds^3} \quad (2)$$

Where,

$a = gmI\ gmII\ RI\ RII$

$b = (CII + Cc)RII + (CI + Cc)RI + gmII\ RI\ RII\ Cc + RzCc$

$c = [RIRII(CICII + CcCI + CcCII)$+RzCc (RICI+RIICII)

$d = RI\ RII\ Rz\ CI\ CII\ Cc$

There are there poles and one zero as given in equation 3, 4, 5 and 6 respectively. P1 is dominant pole which is at low frequency and P2 is non-dominant high frequency pole.

$$P1 = \frac{-1}{(1+gmIIRII)RICc} \backsimeq \frac{-1}{gmIIRIIRICc} \quad (3)$$

$$\mathrm{P2} = \frac{-gmIICc}{CICII+CcCI+CcCII} \backsimeq \frac{-gmII}{CII} \quad (4)$$

$$P3 = \frac{-1}{RzCI} \quad (5)$$

$$Z1 = \frac{1}{Cc(\frac{1}{gmII}-Rz)} \quad (6)$$

Either by taking Rz= 1/gmII, RHP zero can be placed on P2 and its effect can be cancelled or another method is Rz > 1/gmII to move zero in left plane as shown in figure 5 [5,7] .

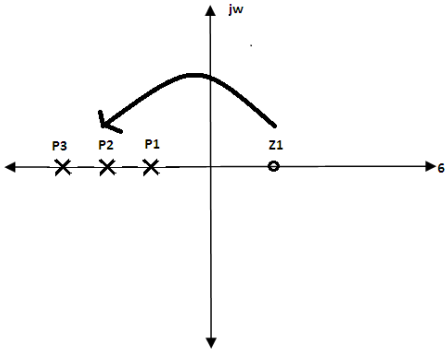

Fig.5 Zero Cancellation Technique

To make a circuit stable, proper compensation is necessary. Modified zero cancelling technique is used as follows [6, 14]-

2.4 Proposed System

To improve stability, biasing circuit is used to run transistor in triode region. Modified circuit is shown in Fig. 6.

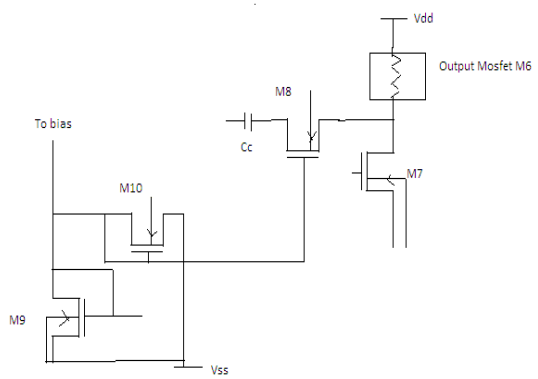

Fig.6 Modified Biasing Circuit

3 Experimental Works

Table 1- process Parameter (kn, kp – transconductance parameter and Vth –threshold voltage) [13]

Sr.No.	**NMOS**	**PMOS**
1	Kn=167.5uA/v.^2	Kp=35.5uA/v.^2
2	Vth=0.3722	Vth=-0.422

Table 2- Design Specifications [15]

Sr.No.	**Parameter**	**Value**
1	Power Supply	±1.8
2	GBW	5Mhz
3	CL	10pF
4	SR	10 v/us

Process parameter and design specifications are shown in table 1 and 2 respectively.

3.1 Integrator

The Optimum value of I10 is designed to increase phase and to keep the minimum power dissipation. For phase margin 60◦, Cc is chosen greater than 0.22 times of C_L [13, 15].

$$I10 = \frac{S10*I9}{S9} \quad (7)$$

$$Rz = \frac{1}{S8}\sqrt{\frac{S10}{2*K*I10}} \quad (8)$$

$$S8 = (\frac{Cc}{Cc+CL})\sqrt{\frac{S10}{2*K*I10}}\sqrt{2*k'*s6*I6} \quad (9)$$

Where

S11=S12=S3=S4

$$gm6 = 10*gm1 \quad (10)$$

$$gm6 = 10*GBW*2\pi*Cc \quad (11)$$

$$\frac{S7}{S5} = \frac{I6}{I5} \quad (12)$$

$$(\frac{S7}{S5}) * \frac{I5}{Cc} = \frac{I6}{Cc} \quad (13)$$

$$Cc * (\frac{S7}{S5}) * SR = I6 \quad (14)$$

$$Rz = \frac{1}{gm6}\left(\frac{CL+Cc}{Cc}\right) \quad (15)$$

Assume $I_{10} = (I_6)/2$ in equation 9], which increases S8 and reduces Rz as in equation 8]. It results in increase in gm6 as shown in equation 15] and hence GBW and Slew rate are increased. Circuit is simulated in Electric VLSI CAD Tool using TSMC 180nm technology. Effect of RHP zero is cancelled and which reduces the effect of non-dominant pole. Modified RHP zero cancelling technique (MRZC) is shown in Fig.7 and Corresponding Gain, Phase are given in Fig.12. RHP zero is equal to pole .Hence effect of non dominant pole is reduced by adjusting $Z = P_2$, It is achieved by putting Rz value in equation 6] from the following equation

$$Rz = \frac{1}{K*S8*(Vgs8-Vt)} \quad (16)$$

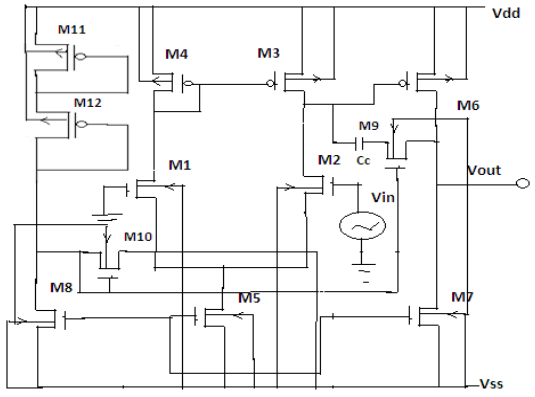

Fig.7 Modified RHP Zero Cancelling Technique

3.2 Comparator

Comparator is as shown in Fig.8; Circuit is modified to increase the gain. Tail transistor M5 and M7 are biased properly. From Small signal analysis is depicted in Fig.9, gain is calculated which is dependent on transconductance and resistance. Gain is inversely proportional to bias current. Consequently, sufficient biasing current is considered to increases gain of two stage comparator. It is done by adjusting $I_9 = 2 * I_4$. Biasing current is designed from differential amplifier in proposed circuit.

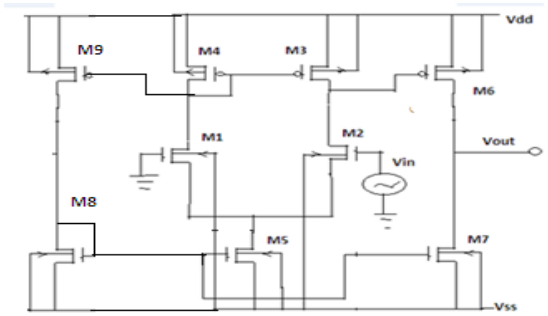

Fig.8 Modified Comparator circuit

Small Signal Circuit Gain-

$$Av = \frac{vout}{vin} = -gm1\ (\ ro1\ \text{II}\ \text{ro2}) \quad (17)$$

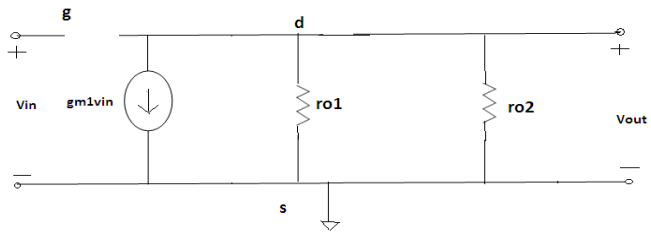

Fig.9 Small signal Circuit of second stage

3.3 D flip-flop

Logic of D flip-flop with minimum transistor is designed to follow the truth table properly as shown in Fig.10. It creates the optimum delay and minimum variability. It consists of a single clocked feedback path with inverter and two transmission gates as a switch. To a N/P MOSFET as a switch, following equations of Ron and R are considered [10, 11, 12].

$$Ron = \frac{1}{k\left(\frac{w}{l}\right)(Vgs - Vth)}$$

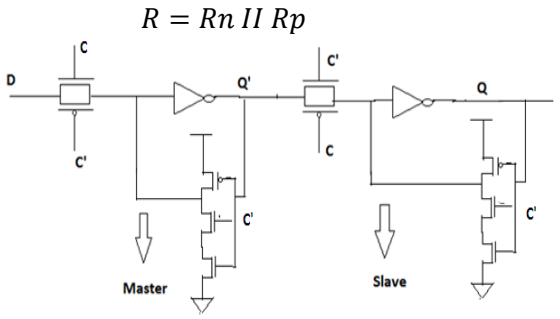

Fig.10 Proposed D flip-flop[9]

The aspect ratio is calculated by properly choosing the value of Ron. Proposed circuit is modified from push pull isolation D flip-flop. In this type feedback isolation is done using single MOSFET. This single transistor is not perfect switching to pass '0' and '1'. This imperfection is removed using a single clocked feedback path with inverter. In this type middle transistor is closed by single clock then either P or N transistor is closed based on input value. There is perfect '1' or '0' value passing from output to the input. Layout is drawn in Electric VLSI CAD Tool as shown in Fig. 9. Proposed circuit is verified for logic of D flip-flop. With condition of clock signal D is passed at input of transmission gate. Based on value of D output will be generated. On disabling of clock signal previous value of output is returned back at the input via switch to maintain stable output signal [9].

4 Sigma Delta ADC

Initially, input sinusoidal signal is applied at the integrator which produces ramp signal based on feedback provided by DAC. Comparator is nothing but the one bit quantizer. It compares signal with ground and produces square wave at the output which switches from positive peak to negative peak. Further, D flip-flop generates digital bit stream of square wave at the rate of Fs.DAC Converts digital signal again into an analog signal in feedback path since to find out the difference between input and feedback signal at the input of integrator as shown in fig.11 [1].

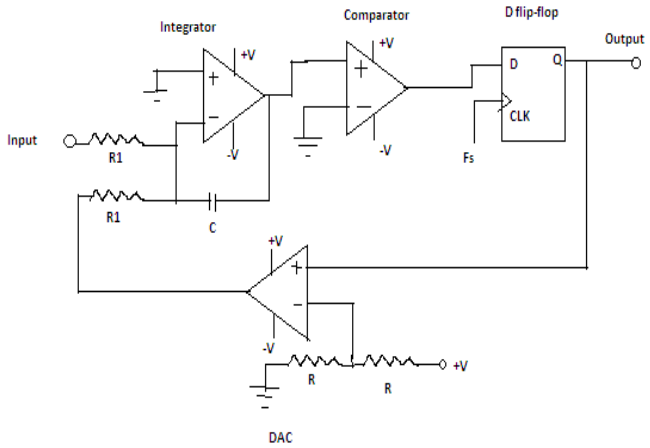

Fig.11 Sigma Delta ADC

5 Results

Electric VLSI CAD tool is used with Winspice simulator. All circuits are simulated using 180nm technology. Minimum phase margin to avoid oscillation in a circuit is 45◦ but at least phase margin of 60◦ is required to improve step response [14]. There is trade off in gain and 3dB bandwidth [4].Table 3 shows comparison of miller compensation technique of OP-AMP integrator with proposed circuit. MRZC gives 112◦ stability with a moderate gain of 34.4dB. PSRR is 48dB as shown in Table 4. Gain of Modified two stage comparator is 52.37dB. Power dissipation is 0.389mW. As compared to existing two stage type [8], slew rate of this comparator is 11V/us and input offset voltage is 0.0048mV as it is indicated in Table 5 and corresponding simulation results are shown in Fig.12 and 13. Table 6 indicates propagation delay of proposed comparator is 140.1ns. Finally Sigma Delta ADC is simulated having input sinusoidal signal of 20Khz and $1V_p$.Over sampling ratio is 8 with a supply voltage of 1.8v.Corresponding simulated waveform is shown in Fig. 14.

Table 3- Comparison of parameters

	Two stage OPAM With miller compensation	**MRZC**
Power supply	1.8	**1.8**

gain	27.6dB	**34.4dB**
Phase	80◦	**112**◦
GBW	5Mhz	**40Mhz**
BW	130Khz	**90Khz**
SR	9.9v/us	**49v/us**

Table 4- Basic Parameter

Parameter	MRZC
PSRR	**48dB**
ICMR	**1v**
Output Swing	**1v**
Input offset voltage	**0.56mV**
PD	**2.85mW**

Table 5-Basic parameter

Parameter	Modified two stage Comparator
gain	**52.37dB**
SR	**11V/us**
UGB	**50Mhz**
Input offset voltage	**0.0048mV**
PD	**0.389mW**
No of transistor	**9**

Table 6-propagation delay

Parameter	Modified two stage Comparator		
	tplh	tphl	Propagation Delay
1.8	**83.9ns**	**196.3ns**	**140.1ns**

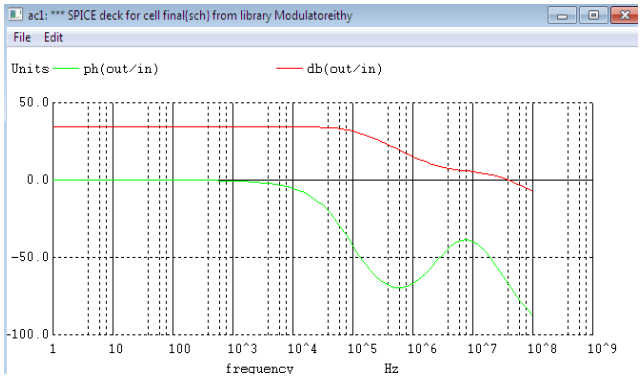

Fig.12 Phase and Gain

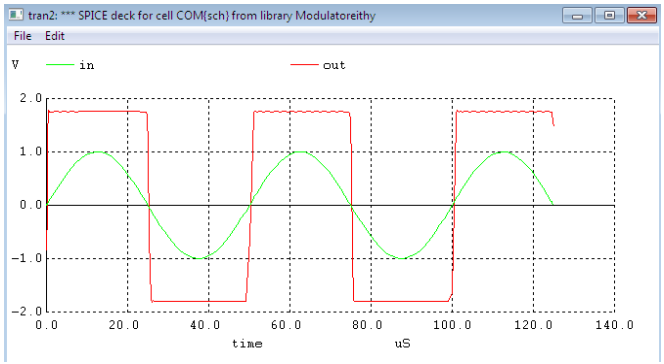

Fig.13 Input and output of comparator

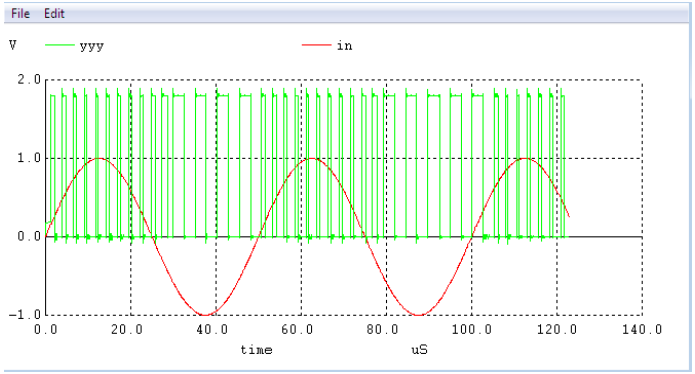

Fig.14 Sigma Delta ADC input Output

6 Conclusion

Modified RHP zero cancellation method of OP-AMP is simulated to consider it as a part of sigma

delta ADC for low power and better stability design requirement. Modified RHP zero cancellation gives much better stability than miller compensation. It increases stability by 40% and gain by 24.6% .Proposed Comparator circuit provides good value of gain due to proper biasing of transistors and power is low. Speed power product and input offset voltage are important parameters to use comparator in Sigma delta ADC. Above proposed circuit gives better value of power speed product than existing comparator. The basic need of D flip-flop is studied for sigma delta ADC .D flip flop gives better robustness and it requires minimum transistors. First order Sigma Delta ADC is simulated by considering all these circuits to generate corresponding digital bit stream.

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