loaded with the *R load* and using the following parameters: $L_1 = 0.8 \cdot 17$ mH, $L_2 = 1.2 \cdot 17$ mH, $C_1 = 1.2 \cdot 80$ μF, $C_2 = 0.8 \cdot 17$ μF. These values were chosen as the worst case scenario that could happen in real Z-network, based on the tolerances of some inductor and capacitor manufacturers. Simulation results obtained by testing the asymmetry with the mentioned parameters are presented in Fig. 10.

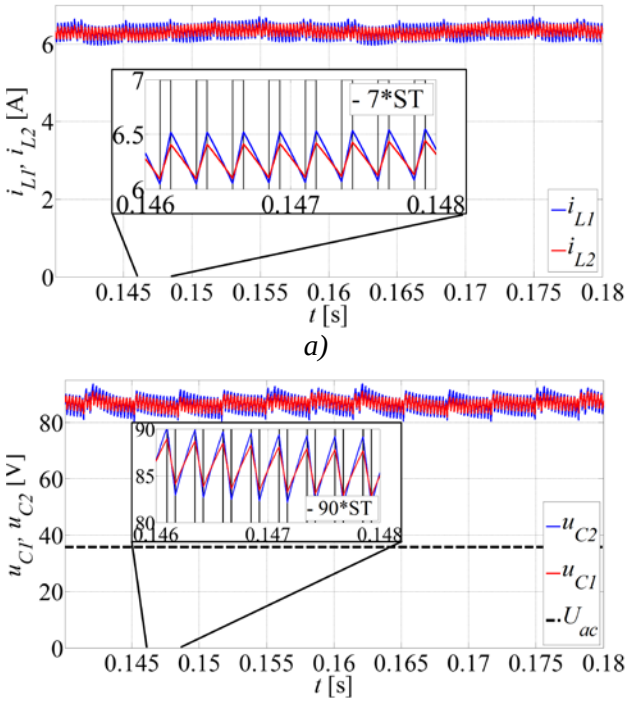

Fig. 10 Simulation waveforms achieved with the "Two-Block" model illustrating asymmetry in inductor currents (a) and capacitor voltages (b).

In Fig. 10a, it can be seen that the maximum difference between i_{L1} and i_{L2} is 0.15 A at any given moment. Also, from Fig. 10b, it can be observed that the maximum difference between u_{C1} and u_{C2} is approximately 2 V (less than 3 % of U_C). In magnified parts of the Fig. 10, the *ST* signal has been multiplied by 7 and 90, respectively, in order to be comparable to the recorded signals. In this way, it is visible when the ZSI switches states. Since the ZSI is evidently robust to tested asymmetries and given the previously mentioned advantages of the "One-Block" model, it can be concluded that the ability to simulate asymmetry between components of the Z-network is not enough to validate further use of the "Two-Block" model. With that in mind, further analysis has been conducted using the "One-Block" model.

Simulation results for the "One-Block" model tested with *RL2 load* are shown in Fig. 11.

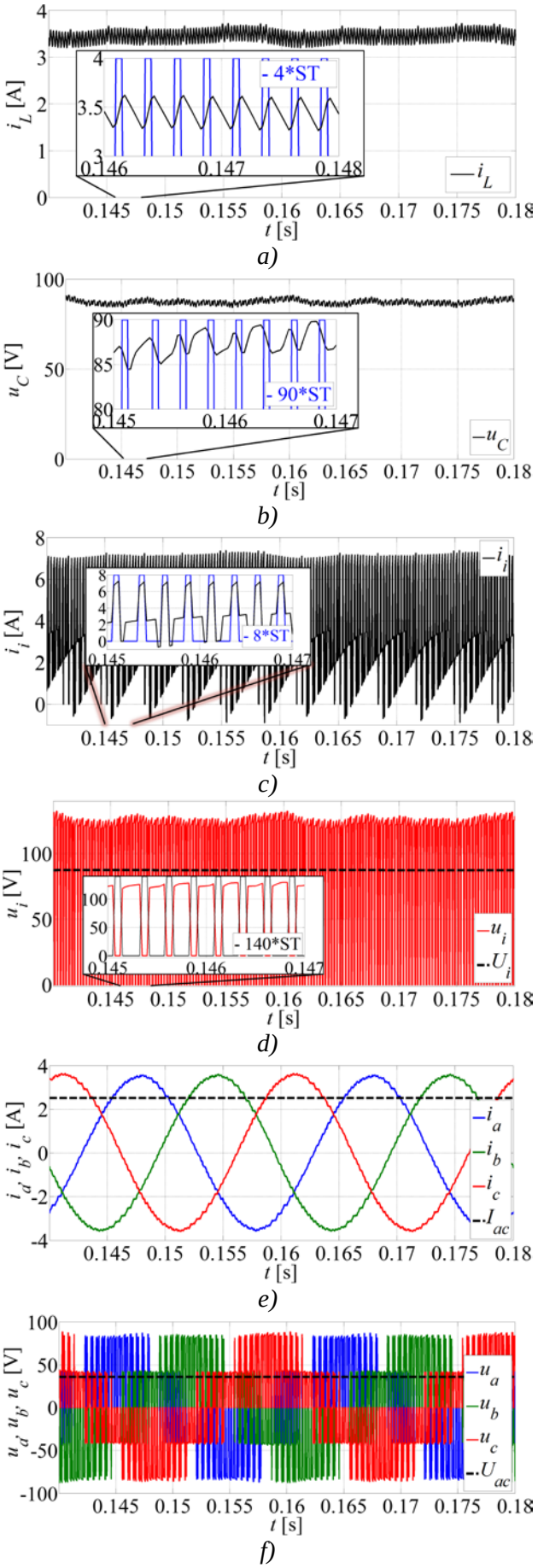

Fig. 11 Simulation results for the proposed model.

Inductor current is shown in Fig. 11a, with the zoomed in portion of the same signal shown alongside the *ST* signal. There, the process of magnetizing the inductor can be observed as the inductor current increases during the ST period. The opposite action happens for the capacitor voltage u_C – it decreases during the ST period, as shown in Fig. 11b. In Fig. 11c, the inverter DC side current i_i is shown. It can easily be observed that it is changing between $i_i^{'}$ and $i_i^{''}$, depending on the ST state, as described by (24). Fig. 11d shows the inverter DC side voltage u_i and its average value U_i, which corresponds to the average value of U_C, presented in Table 1. In magnified parts of the Figs 11a – 11d, the *ST* signal has been multiplied by 4, 90, 8 and 140, respectively, for the reasons explained earlier. In Figs 11e and 11f, three-phase load currents and voltages are shown, respectively, alongside the respective RMS values of the fundamental harmonic, denoted by dashed lines. This demonstrates that the proposed models correctly describe the ZSI system.

For the considered ZSI system, the SPS inverter model does not allow the elimination of the snubber. Although the snubber capacitance was set to *inf*, the same could not be applied for the snubber resistance. Setting the snubber resistance to a value lower than 10^4 Ω lead to overestimated values of the inductor current, whereas with values higher than 10^9 Ω, the simulation would not start. Consequently, the default value of 10^5 Ω was chosen. In addition, running the SPS model in Simulink multitasking mode produced results that are not physically meaningful.

5 Conclusion

In this paper two novel and simple models of the ZSI system have been successfully developed using only basic Simulink libraries. Based on the simulation results, it can be concluded that the proposed models closely match the results of the SPS model for all tested loads.

The "Two-Block", unlike the "One-Block" model, allows simulation of an asymmetrical Z-network. However, the ZSI was proven robust to such asymmetries. Faster performance and the ability of the "One-Block" model to provide accurate results at lower sampling frequencies makes it a better choice of the two proposed models.

The proposed models offer several important advantages over the SPS model such as greater control over model, lower cost, and upgradeability. Moreover, it was noted that the SPS model, unlike the proposed models, does not provide physically plausible results in the Simulink multitasking mode, and also mandates the implementation of a snubber. On the other hand, the SPS model has the advantage in accuracy when simulating the ZSI system supplying loads with power factor lower than 0.5 (although a very small percentage of actual loads fall into this group). This is because the input diode has been modelled as a mechanical switch in the proposed models so the input current is allowed to flow into the DC source, which is not the case in practice. This problem is the subject of the future research.

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