A Transmission Gate based High Frequency Rectifier Designed Using 45nm CMOS process for RF Energy Harvesting Application

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Abstract: - With the emergence of 5G communication there has been considerable emphasis on energy conservation and management along with the prevalent methods and designs. The requirement is to generate reliable and faster data transfer with energy management. Energy harvesting or more specifically RF energy harvesting is very significant for a modern communication system to achieve the self-sustainability of the network in terms of power. A high frequency rectifier is essentially the core of such a system. There are several challenges in the design of a rectifier at high frequency. The major challenge lies in enhancing the percentage conversion efficiency (PCE) for a low power signal which is limited by the leakage in the CMOS device. This paper presents a work related to high frequency rectifier design based on transmission gate (TG) for RF applications which achieves a PCE to 80% at -2dBm in its single stage realization and is highest in class efficiency as compared to reported literatures. The frequency response shows the performance over a wideband and it works in 953 MHz GSM band. Also this performance is achieved with minimal number of devices and with 110nW power dissipation.

Key-Words: - Energy Harvesting, PCE, Transmission Gate, CMOS, RF

1 Introduction

With the emergence of 5G communication, apart from the technological requirements of faster and reliable communication, energy conservation and management is essentially becoming significant. As a matter of fact in all wireless networks, self-sustainability is becoming an issue of potential importance. To address self-sustainability as well as virtual operation energy harvesting capability must be embedded into the network. As the energy harvesting capability of a network makes the life-time of the network augmented, it facilitates the installing a network at any hard to reach location without the requirement of a electrical power source. Hence energy harvesting is a potential candidate to be declared as indispensable in medical as well as surveillance applications in the near future.[1][2]. Several natural and manufactured sources exists which can be well utilized for harvesting energy. As the nature of the sources are diversified and there is a necessity to transfer the harvested energy from node to node, harvesting design has to be of different capabilities and efficiencies [3].

Design of a rectifier or charge pump is the core of the energy harvester design. There are different challenges in a rectifier designs. Some of them are high frequency compatibility, low power consumption, low area in silicon substrate etc. But to maximize the power conversion efficiency (PCE), the most important criteria which the designer must address to formulate an efficient design. Cross coupled bridge configuration with differential RF input can be designed which give low on state current and small leakage current and thereby offering better PCE[4]. Voltage doubler Ultra High Frequency (UHF) rectification unit is also designed with the technique of internal cancellation to achieve a zero-threshold transistor and thereby an accepted PCE is achieved with reduced area [5]. Dickson charge pump is one of the most widely used structure for this purpose and different modifications have been presented by several designers for specific applications and efficiencies. The Dickson charge pump has been modified to reduce the leakage current with linear regulator and thereby total power consumption can be reduced [6]. Rectifier based on improved Dickson charge pump in two configurations is presented which works in GSM band with a satisfactory PCE [7]. Also dynamic threshold reduction technique based CMOS rectifier has been designed with the use of a clamper to reduce the effective threshold voltage

and increase the sensitivity and hence achieving a high PCE [8].

This paper presents the design of a high frequency rectifier based on transmission gate using the 45nm CMOS process for RF energy harvesting applications with the achievement of a PCE of 80% at -2dBm in single stage. This is the highest in-class PCE achieved in single stage with the use of only 4-transistors and a significantly lower power consumption of 110nW.

The remaining of the paper is organised as follows. Section 2 briefly explains a basic RF energy harvesting system. Section 3 deals with the proposed design with explanation of the functionality, section 4 deals with simulation results, comparative analysis and discussion and section 5 includes the concluding research summary.

2 Proposed RF Energy Harvesting System using TG Dickson Rectifier

The basic system of RF energy harvesting consists of three units. These are matching network, a high frequency rectifier and a power management unit. This is shown in Fig. 1. The purpose of the matching network is to ensure impedance matching with the used antenna. This basically facilitates the maximum power transfer from the antenna to the rectification unit succeeding this network.

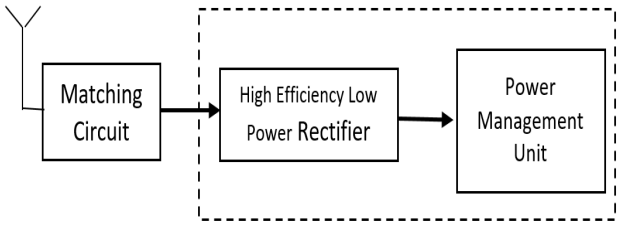

Figure. 1: System diagram of RF energy harvesting

The power management unit is responsible for management of the rectified power depending on the system configuration and battery capacity and also to distribute the surplus power to the neighboring nodes if necessary. This design can be different depending on the battery capacity intended to use viz. zero battery or finite sized battery. As stated earlier the rectifier unit is the heart of such a set-up as its PCE decides the successful functioning of the system. There happens to be different design challenges of the rectifier and among these achieving higher PCE at lower dBm level is one of the basic and significant challenge which needs to be addressed with a simpler and cost effective design. The low power rectifier which is the critical element of the work is designed using Dickson based rectifier which utilizes the concept of TG to achieve high PCE.

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The proposed TG based design of the Dickson rectifier is shown in Fig. 2. The transmission gate (TG) finds application in many CMOS based design. As the nMOS pass transistor allows the negative voltage efficiently with less propagation time while the pMOS pass transistor permits the positive voltage to develop efficiently with less propagation time; hence transmission can be a solution to such situations where the circuit is subjected to encounter both the voltage levels. Moreover the TG generates a sufficiently higher on state current for a wide range of input voltage.

The design presented here is a modification to the Dickson Charge Pump with the use of TG to produce a higher output power. Dickson charge pump is a circuit which is based on the principle of charge multiplication. A simple Dickson charge pump is configured similar to the circuit shown in Fig.2 with two diode-connected MOSFETs. In the negative half of the cycle the left hand side device conducts and thereby provides a charging path for the input capacitor. In the positive half of the cycle the device in the right hand side conducts and provides the discharging path to the input capacitor which ultimately facilitates the transfer of charge from the input capacitor to the output capacitor. This configuration works fine but when the circuit needs to be modelled in finer resolution technology nodes it is limited by the drain current as all the dimensions of the device as well as the supply voltage value needs to be scaled.

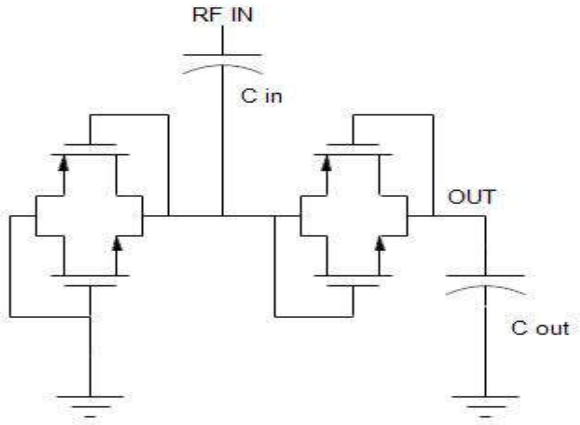

Figure 2: Proposed TG based circuit schematic of Dickson Charge Pump

Hence the output current falls and thereby showing impact on the PCE. Since TG is known for

its higher current drive and successful transmission of both the logic states, hence the conventional Dickson charge pump is re-configured with TG.

For a negative cycle the input capacitor will get charged by finding the path through the left side TG while in the positive cycle the charge in the input capacitor gets transferred to the output capacitor through the TG in the right side of the schematic. As the current through the TG is high, hence the output power is also high.

In a TG structure when input is positive; the pMOS will be initially saturated and then shall switch to non-saturation state while the nMOS will be in saturation state. If we consider the I_{Dn} and I_{Dp} be the current through the nMOS and the pMOS respectively and V(t) be the RF signal voltage, then the total output current is

$$I_{out} = I_{Dn} + I_{Dp} \quad (1)$$

Again, initially

$$I_{Dp} = \beta_p/2\ [V(t) - |V_{Tp}|\ ] \quad (2)$$

But as the output voltage rises

$$I_{Dp} = \beta_p/2\ [2(V(t) - |\ V_{Tp}\ |)(V(t) - V_{out}) - (V(t) - V_{out})^2] \quad (3)$$

Also the on state current of nMOS is

$$I_{Dn} = \beta_n/2\ [V(t) - V_{out} - V_{Tn}\ ] \quad (4)$$

So the output power is

$$P_{out} = V_{out}\ .\ I_{out} = V_{out}\ (I_{Dn} + I_{Dp}) \quad (5)$$

The power conversion efficiency (PCE) can be calculated as

$$PCE = (P_{out} / P_{in})*100\% \quad (6)$$

Previously without the use of TG the P_{out} would have been either V_{out} (I_{Dn}) or V_{out} (I_{Dp}). So the P_{out} would have lower and thereby resulting a low PCE. Thus, by using TG based configuration, better PCE is achieved.

3 Results and Discussion

The designed circuit is simulated and we discuss the results obtained in following Sub sections.

3.1 Optimization

Optimization of the aspect ratio the devices is important to ensure maximum possible performance of the circuit for a specific configuration. Without this the circuit will remain under performing or even non performing. Hence this may be regarded as the the preliminary step of this design. The basic purpose of the aspect ratio (W/L) tailoring for both the nMOS and pMOS in this circuit is to get a minimum or zero AC component at the output so as to maximize the DC output and thereby achieve higher efficiency. So the AC component of the output is plotted by sweeping nMOS channel length (Ln) and width (Wn) and pMOS channel length (Lp) and width (Wp). This can ensure the maximum possible output with optimum aspect ratio.

From the Fig. 3 it is observed that the AC component in the output is minimum at around 45nm of the nMOS channel length which is the minimum permissible channel length in 45 nm Generic Process Design Kit (GPDK) technology node.

Similarly Fig.4 shows that the at 65nm channel length of pMOS, the output AC component can be achieved a minimum value.

Fig.5 and Fig.6 indicates that as the value of width in both the nMOS and pMOS decreases, the AC component reduces. As the minimum width supported in 45nm technology node is 150nm hence this value is set for both the devices.

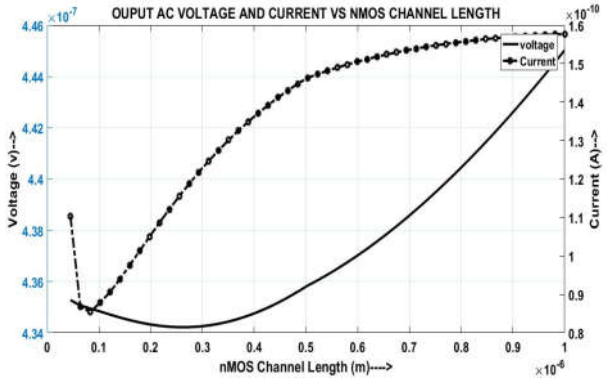

Figure 3: Output AC component vs L_n

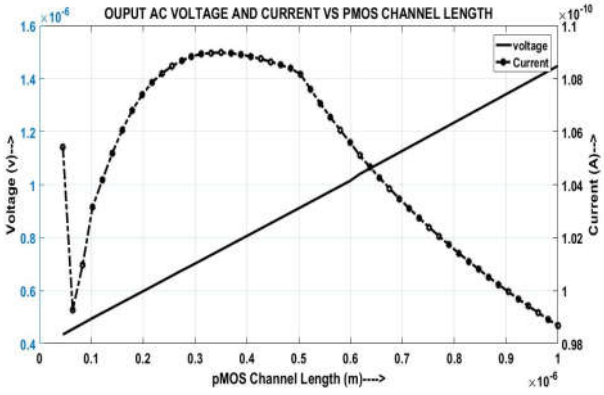

Figure 4: Output AC component vs L_p

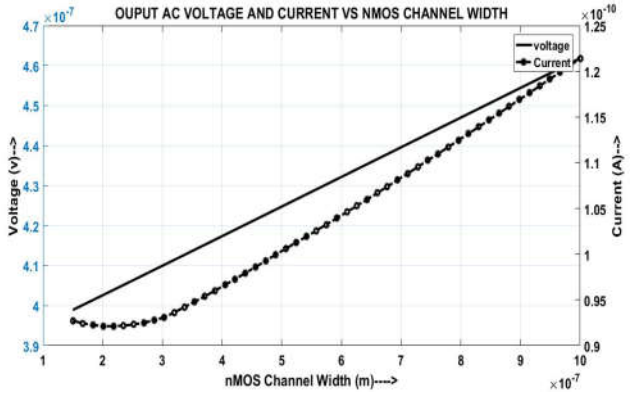

Figure 5: Output AC component vs W_n

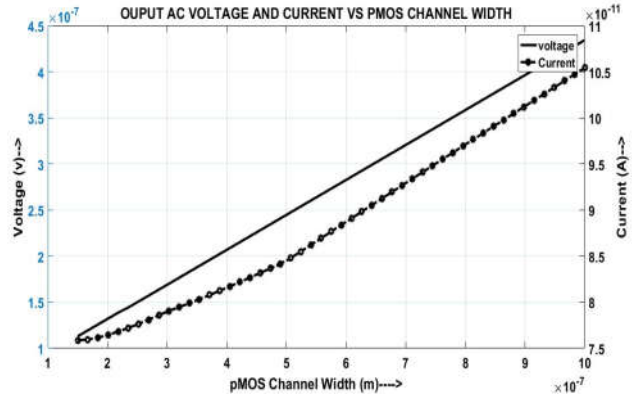

Figure 6: Output AC component vs W_p

So the aspect ratio of both the nMOS and the pMOS is tailored as follows

L_n	W_n	L_p	W_p
45nm	150nm	65nm	150nm

Table 1: Aspect Ratios of both nMOS and pMOS devices

3.2 Design Simulation

The transient response of the designed circuit is simulated. The output voltage shows a dependence on the value of output capacitance as well as input capacitance. Fig. 7 shows the transient response of different values of output capacitances and the maximum output voltage observed is 506 mV.

The change in output voltage with the variation in the output capacitance is shown in Fig. 8. It shows that output DC voltage increases with the decrease in the capacitance value.

The dependence of input capacitance is shown in Fig. 9 and 10. The transient response for different values of C_{in} is shown in Fig. 9. Fig. 10 depicts that with the increase in the value of C_{in} the output DC voltage increases marginally. From Fig. 8 and 10 it is clear that the values of input and output

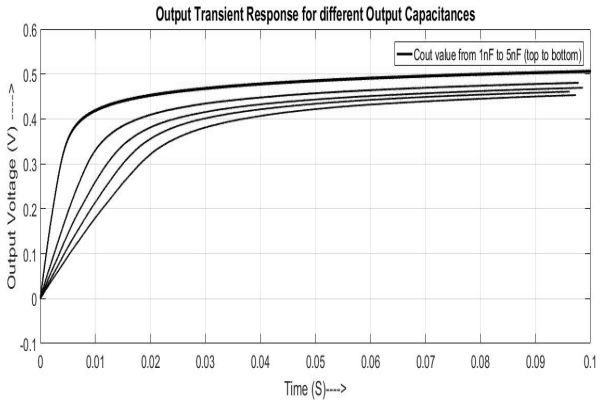

Figure 7: Output DC Voltage for different C_{out}

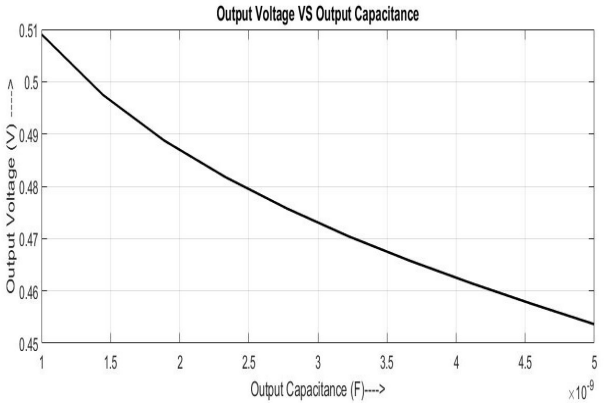

Figure 8: Output voltage vs C_{out}

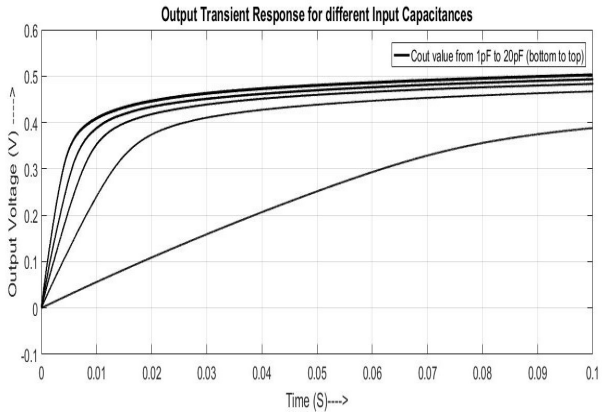

Figure 9: Output DC Voltage for different C_{in}

capacitance can be determined and used to achieve better performances.

The frequency response of the designed circuit is shown in Fig. 11 which validates the working of the circuit in the complete RF band upto GHz mark. It can facilitate almost all types of RF transmission with high PCE and smoothly ensure energy harvesting in several known 3G/4G spectrum slots.

Another important aspect is the temperature stability of the circuit. The output AC component is plotted against the temperature and it depicts that

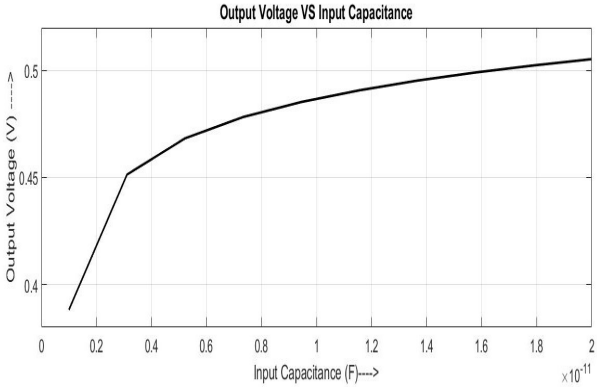

Figure 10: Output voltage vs C_{in}

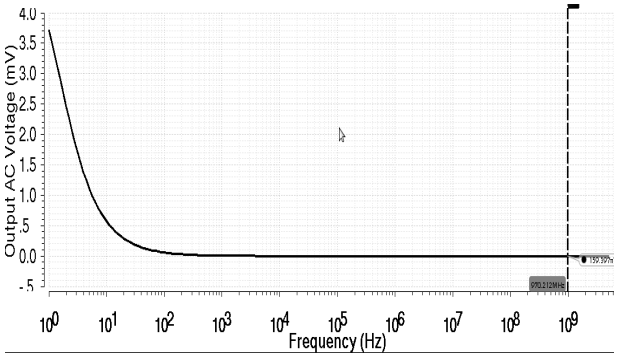

Figure 11: Frequency Response of the circuit

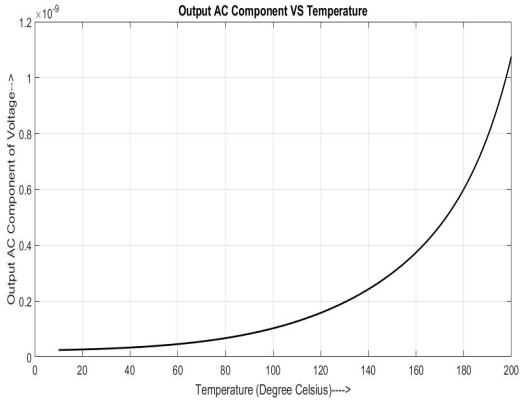

Figure 12: Output AC voltage vs temperature

the AC component changes negligibly upto around 100^0 C and increases marginally beyond that temperature which is expected due to the rise in the leakage current. This is shown in Figure 12.

Finally the output voltage is plotted against the input power (Fig. 13). Also the PCE is plotted against the input power. The output DC voltage increases with input power. The maximum PCE is achieved 80% at -2dbm and 70% at -2.5dbm while the PCE is 40% at -5dbm. This is shown in Fig. 14.

The results obtained are compared with the recent reported works by considering different parameters. This is presented in Table 2.

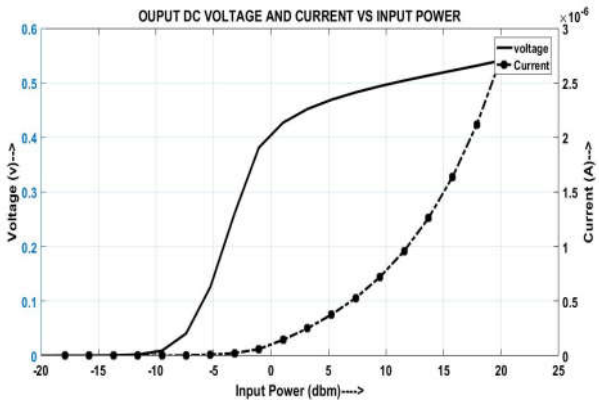

Figure 13: Output DC voltage and current vs P_{in}

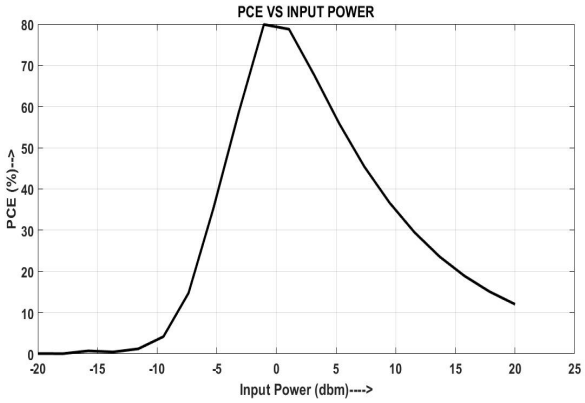

Figure 14: PCE vs P_{in}

Table 2 clearly indicates the effectiveness of the designed system.

4 Conclusion

The TG based rectifier presented here is simulated for a wide range of frequencies and is observed that the design is suitable for working at almost all known 3G/4G bands commercially available for wireless networking. The maximum power conversion efficiency is achieved is 80% at -2db which is significantly high in single stage as compared to the recently reported literatures. This makes the circuit suitable to be used as part of an energy harvesting system in a green communication set-up to convert the RF signal energy to an equivalent DC energy and store in some battery and thereby making the nodes self-sufficient in terms of power. The number of transistors used is 4 and hence it takes less surface area and silicon being the costliest real estate it can lead to a cost effective design. Also the power dissipation is achieved to be 110nW which is an important aspect because a power hungry design makes the implementation less

Work	Comparison with the reported works					
	Technology	*Stage*	*Frequency (MHz)*	*Input Power (dbm)*	*Output Voltage (V)*	*Max PCE (%)*
[9]	Schottky Diode	1	868	10	-	48
[10]	Schottky Diode	1	900	-10	0.66	40
[11]	Schottky Diode	2	868	-10	0.649	44
[12]	Schottky Diode in 0.35 µm CMOS	5	900	-14.8	1.5	36
[13]	TSMC 0.18 µm	8	925	-21.2	0.78	43
[4]	0.18 µm CMOS	1, Diff	953	-12.5	0.62	67
[14]	TSMC 90 nm CMOS	5, Diff	868	-17	1.62	40
[15]	65 nm CMOS	5	900	18	6	31
[7]	65 nm CMOS	2	953	-15	0.402	56
This work	45 nm CMOS	1	953	-2	0.485	80

Table 2: Comparative Analysis

viable despite high energy conversion. So the importance of this design lies in the fact that it has a better PCE at almost all popular wireless frequency range with lower power consumption and less silicon area. The subsequent challenge shall be to achieve better PCE at a lower input signal (< -2dBm). Further, the system should be able to execute multi-frequency harvesting.

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