# Single Active Element Based Variable Gain Multifunction Filter with MOS-C Implementation

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*Abstract:* This paper introduces a new voltage-mode multifunction filter employing single current differencing transconductance amplifier (CDTA) and its MOS-C implementation. The proposed filter topology can synthesize all filter types, i.e. low-pass, high-pass, band-pass, band-stop and all-pass filters by modifying three admittances and gain of the filters can be adjusted independently by a resistor. Central frequency of the filters can be tuned electronically. The operability of the circuit is confirmed in close agreement with the theory by PSPICE simulation software using TSMC 0.18 micron CMOS model parameters at ±0.9 V supply voltage. The proposed circuit is suitable for integration technique through the MOS-C implementation.

*Key-Words:* Current differencing transconductance amplifier, MOS-C, Multifunction filter, Variable gain.

## 1 Introduction

Analog filters play an essential role in signal processing circuits and communication, instrumentation, sound system applications. In recent years, a considerable attention given to a particular type of filter circuits, which is called as multifunction filter because of its versatility and flexibility for the applications require same circuit topology which provides different type filter functions. Single active element based multifunction filters can be considered as an economic utilization especially where simple circuitry and low power consumption are important design criteria. Due to their extensive usage, several multifunction filters based on different type active building blocks have been presented in recent years.

The CDTA active building block is introduced by Dalibor Biolek in 2003 to be employed in analog signal processing applications [1]. Since then, CDTA and its modifications are still emerging as the most efficient active elements. The CDTA has advantages of better bandwidth, higher speed, electronic tunability and it is free from parasitic input capacitances [2]. Due to these advantages, a significant attention given to CDTA in filter realization [3-9].

The aim of this work is to introduce a new single input-single output (SISO) type, gain variable and electronically tunable multifunction filter using single CDTA suitable for low voltage applications. The proposed circuit is voltage-mode and all the filter functions i.e. low-pass (LP), high-pass (HP), band-pass (BP), all-pass (AP) and band-stop (BS) are synthesized using the same circuit topology with MOS-C realization.

The remaining content of this paper is composed as following: Section 2 provides the circuit definition of CDTA active element. Proposed circuit topology is introduced and circuit analysis is carried out in Section 3. MOS-C realization of the introduced circuit is also depicted in this section. Section 4 includes the simulation results of the filter circuits. Electronic tunability of gain and central frequency is also demonstrated in Section 4. Section 5 contains the conclusions of the presented paper. A comparison table of CDTA based multifunction filters available in open literature is also given in this section to show the originality of this work.

## 2 Definition of CDTA

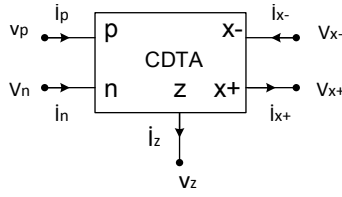The circuit schematic of CDTA is shown in Fig. 1.



Fig.1. Circuit schematic of CDTA

The CDTA's definition equation can be represented as

$$\begin{bmatrix} v_p \\ v_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ v_x \\ v_z \end{bmatrix} \quad (1)$$

$p$ and $n$ indicate the input terminals, $x$ and $z$ indicate the output terminals of CDTA and $g_m$ is the transconductance gain, which can be adjusted by a bias current. $i_x$ denotes the output current and it is assumed that $i_{x+}=-i_{x-}$ in dual output CDTA. $z$ terminal current ($i_z$) is equal to difference of $p$ and $n$ terminal currents. The voltage of $z$ terminal is transferred by a transconductance $g_m$ to a pair of output currents at $x$ terminals.

Taking into consideration the nonidealities of CDTA, the definition equation becomes as follows.

$$\begin{bmatrix} v_p \\ v_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ v_x \\ v_z \end{bmatrix} \quad (2)$$

In (2), $\alpha_p$ and $\alpha_n$ denote the current gains defined by $\alpha_p=1-\varepsilon_p$ and $\alpha_n=1-\varepsilon_n$. Here, $\varepsilon_p$ and $\varepsilon_n$ are

current tracking errors and their absolute values approache to zero.

The CDTA circuit can be considered as a structure of cascade connection of current differencing stage and operational transconductance amplifier (OTA) and it can be implemented using both BJT and CMOS technology as well as commercial ICs. The CDTA used in this study contains only MOS transistors implemented in 0.18 micron CMOS technology.

## 3 Proposed Filter Topology

The proposed filter topology consists of single CDTA active element and four admittances as shown in Fig. 2.
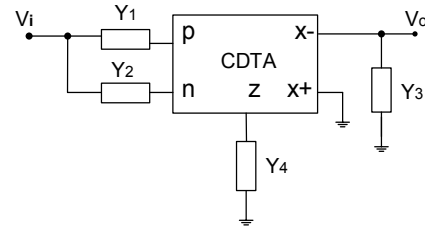


Fig.2. Proposed filter topology

Circuit analysis using (1) yields transfer function as

$$\frac{V_0}{V_i} = \frac{g_m(Y_2-Y_1)}{Y_3Y_4} \quad (3)$$

If $g_m/Y_4$ considered as the gain of the filter and $Y_4$ chosen as $G_4$, then the filter gain become adjustable by a resistor without affecting the central frequency. If the admittance combinations are taken as given in Table 1, all filter types, i.e. LP, HP, BP, AP and BS filter circuits can be synthesized.

Table 1. Admittance combinations of the proposed filters

| Filter Type | $Y_1$ | $Y_2$ | $Y_3$ | Condition | Radian Frequency ($\omega_0$) | Quality Factor (Q) |
|---|---|---|---|---|---|---|
| LP | $\dfrac{1}{\frac{1}{sC_1}+\frac{1}{G_1}}$ | $G_2$ | $sC_3+G_3$ | $R_1=R_2$ | $\dfrac{1}{\sqrt{R_1R_3C_1C_3}}$ | $\dfrac{\sqrt{R_1R_3C_1C_3}}{R_1C_1+R_3C_3}$ |
| HP | $\dfrac{1}{\frac{1}{sC_1}+\frac{1}{G_1}}$ | $sC_2$ | $sC_3+G_3$ | $C_1=C_2$ | $\dfrac{1}{\sqrt{R_1R_3C_1C_2}}$ | $\dfrac{\sqrt{R_1R_3C_1C_2}}{R_1C_1+R_3C_3}$ |
| BP | $\dfrac{1}{\frac{1}{sC_1}+\frac{1}{G_1}}$ | $0$ | $sC_3+G_3$ | - | $\dfrac{1}{\sqrt{R_1R_3C_1C_3}}$ | $\dfrac{\sqrt{R_1R_3C_1C_3}}{R_1C_1+R_3C_3}$ |
| AP | $\dfrac{1}{\frac{1}{sC_1}+\frac{1}{G_1}}$ | $sC_2+G_2$ | $sC_3+G_3$ | $C_1G_1=2(C_1G_2+C_2G_1)$ | $\dfrac{1}{\sqrt{R_1R_2C_1C_2}}$ | $\dfrac{R_3C_3}{R_1C_1+R_3C_3}\sqrt{\dfrac{R_1C_1}{R_2C_2}}$ |
| BS | $\dfrac{1}{\frac{1}{sC_1}+\frac{1}{G_1}}$ | $sC_2+G_2$ | $sC_3+G_3$ | $C_1G_1=C_1G_2+C_2G_1$ | $\dfrac{1}{\sqrt{R_1R_2C_1C_2}}$ | $\dfrac{R_3C_3}{R_1C_1+R_3C_3}\sqrt{\dfrac{R_1C_1}{R_2C_2}}$ |

By assuming that $g_m/G_4$ is equal to unity, transfer functions of the filters become as follows:

$$T(s)_{LP} = \frac{G_1 G_2}{s^2 C_1 C_3 + s(C_1 G_3 + C_3 G_1) + G_1 G_3} \quad (4)$$

$$T(s)_{HP} = \frac{s^2 C_1 C_2}{s^2 C_1 C_3 + s(C_1 G_3 + C_3 G_1) + G_1 G_3} \quad (5)$$

$$T(s)_{BP} = -\frac{s C_1 G_1}{s^2 C_1 C_3 + s(C_1 G_3 + C_3 G_1) + G_1 G_3} \quad (6)$$

$$T(s)_{AP} = \frac{s^2 C_1 C_2 - s(C_1 G_3 + C_3 G_1) + G_1 G_2}{s^2 C_1 C_3 + s(C_1 G_3 + C_3 G_1) + G_1 G_3} \quad (7)$$

$$T(s)_{BS} = \frac{s^2 C_1 C_2 + G_1 G_2}{s^2 C_1 C_3 + s(C_1 G_3 + C_3 G_1) + G_1 G_3} \quad (8)$$

The conditions must be fulfilled to realize the filter functions, radian frequency of the filters and quality factor equations are also given in Table 1.

The passive component sensitivities are all calculated as

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{R_3}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{C_3}^{\omega_0} = -1/2 \quad (9)$$

It can be seen from (9) that the radian frequency sensitivity to the passive components is less than unity.

MOS-C implementation of a circuit can be achieved by replace the resistors with their MOSFET conjugates. A linear resistor can be implemented using two parallel connected depletion type MOSFETs working in linear region [10]. Fig. 3 represents MOS-C implementation of the filters synthesized from the proposed topology. It should be noted that tuning of central frequency, quality factor and gain adjustment of each filter can be done by MOSFET's gate voltages.
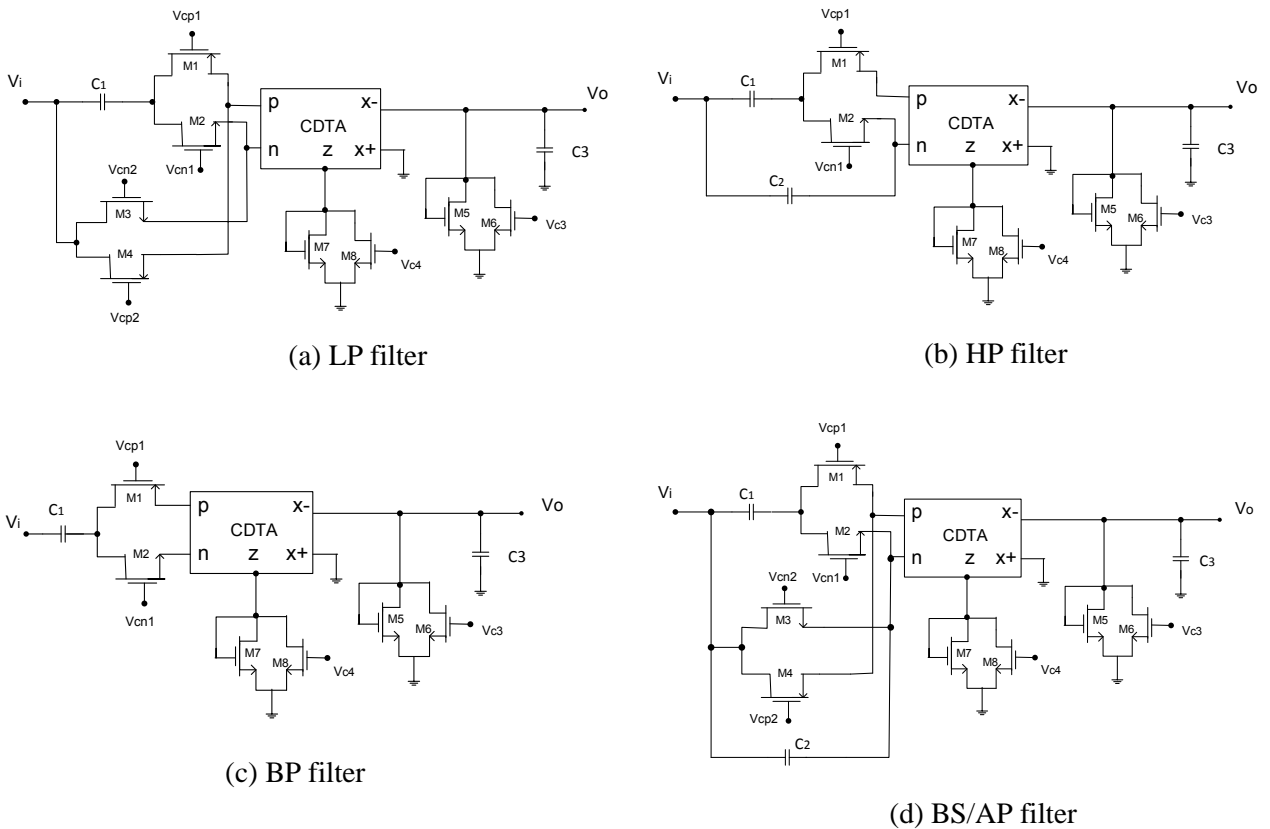


(a) LP filter



(b) HP filter



(c) BP filter



(d) BS/AP filter

Fig.3. MOS-C implementation of the filters

## 4 Simulation Results

To validate the workability of the proposed circuit, PSPICE simulation has been done using TSMC 0.18 micron CMOS model parameters. Table 2 shows the passive component values taken in simulation.

Dimensions of MOSFETs used to implement the resistors located in Fig.3 are set to W=0.38 μm, L=0.18 μm for M1-M8 in LP, HP and BP filters, W=0.38 μm, L=0.18 μm for M1-M6, W=0.76 μm, L=0.18 μm for M7-M8 in BS filter, W=1.52 μm,

L=0.18 µm for M1- M2, W=0.38 µm, L=0.18 µm for M3-M8 in AP filter. MOSFET gate voltages yielding the required resistor values are given in Table 3.

Table 2. Passive component values

| Component | LP | HP | BP | AP | BS |
|---|---|---|---|---|---|
| $R_1$ | 1.25 kΩ | 1.25 kΩ | 1.25 kΩ | 312.5 Ω | 520 Ω |
| $R_2$ | 1.25 kΩ | - | - | 1.25 kΩ | 1.04 kΩ |
| $R_3$ | 2.5 kΩ | 2.5 kΩ | 2.5 kΩ | 1.25 kΩ | 1.04 kΩ |
| $R_4$ | 2.5 kΩ | 1.4 kΩ | 2.5 kΩ | 1.25 kΩ | 1.7 kΩ |
| $C_1$ | 80 pF | 60 pF | 120 pF | 340 pF | 210 pF |
| $C_2$ | - | 60 pF | - | 85 pF | 105 pF |
| $C_3$ | 45 pF | 0.1 pF | 30 pF | 0.1 pF | 0.1 pF |

Table 3. MOSFET gate voltages

| Gate | LP | HP | BP | AP | BS |
|---|---|---|---|---|---|
| $V_{cn1}$(V) | 0.65 | 0.375 | 0.375 | 0.65 | 0.9 |
| $V_{cp1}$(V) | -0.1 | -0.375 | -0.375 | -0.1 | -0.9 |
| $V_{cn2}$(V) | 0.48 | - | - | 0.65 | 0.45 |
| $V_{cp2}$(V) | -0.27 | - | - | -0.1 | -0.45 |
| $V_{cn3}$(V) | 0.375 | 0.375 | 0.375 | 0.75 | 0.9 |
| $V_{cn4}$(V) | 0.375 | 0.67 | 0.375 | 0.75 | 0.55 |

In simulation, MOS implementation of CDTA given in [6] is used. MOSFET dimensions are modified as given in Table 4 and supply voltage of the circuit is taken as symmetrical ±0.9 V. Bias current of the CDTA ($I_{BIAS}$) is set to 400 µA.

Table 4. Transistor dimensions

| Transistor | W (µm) | L (µm) |
|---|---|---|
| M1-M6 | 1.4 | 0.18 |
| M7-M10 | 0.9 | 0.18 |
| M11-M12 | 1.8 | 0.18 |
| M13-M14 | 2.8 | 0.18 |
| M15-M20 | 1 | 0.18 |
| M21-M24 | 0.7 | 0.18 |

The central frequency is calculated as 1.5 MHz by using the component values given in Table 2. In simulation of the MOS-C circuits, the frequency is measured to be 1.45 MHz for LP filter, 1.52 MHz for HP filter, 1.40 MHz for BP filter, 1.47 MHz for AP and BS filters. Power dissipation of the circuits are 2.97 mW for LP, 2.19 mW for HP, 4.12 mW for BP, 4.13 mW for AP and 3.14 mW for BS filter. Frequency responses of the filters are given in Fig.4.

To demonstrate the tunability of the central frequency, BS filter is chosen to be worked by adjusting the MOSFET gate voltages at the range of 0.7 V - 0.9 V and 0.35 V - 0.45 V. Frequency tuning graphic is given in Fig.5.

To examine the total harmonic distortion (THD) performance of the circuit, a sinusoidal signal with amplitude up to 100 mV is gradually applied to the

input of the HP filter. The measured THD values are given in Fig.6. Fig. 7 represents the gain adjustment graphic of the HP filter using $V_{cn4}$ (gate voltage of MOSFETs used to realize the $R_4$ resistor) without affecting the central frequency.
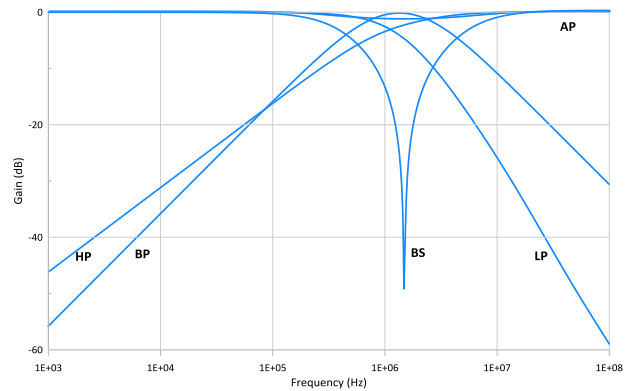


Fig.4. Frequency response of the proposed multifunction filter
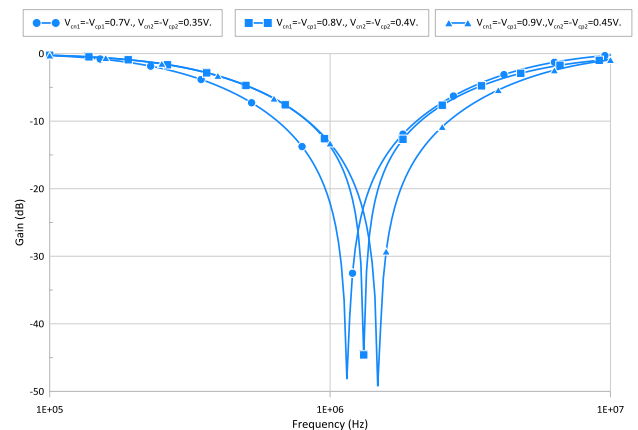


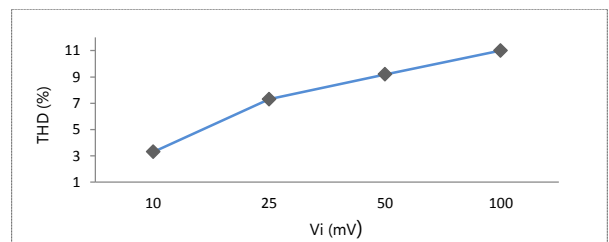Fig.5. Tuning of the band-stop filter



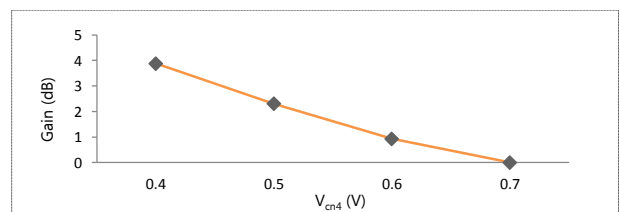Fig.6. THD graphic of the HP filter



Fig.7. Gain adjustment of the HP filter

# 5 Conclusions

A new variable gain voltage-mode multifunction filter with MOS-C implementation has been presented in this paper. All filter types are synthesized by using single CDTA active element based on same topology. Simulation results confirmed the validation of the filter circuits. The circuit also features suitability for integration and independent control of frequency tuning and gain adjustment. These features qualify the proposed circuit to be a good alternative in applications where simple circuitry, operability at low voltage and independent control of gain and frequency tuning are important design parameters. Table 5 shows a comparison of previous implementations of CDTA based multifunction filters available in the open literature to represent the advancements of the introduced circuit.

Table 5. Comparison of previously reported CDTA based multifunction filters

| Ref. number | Technology | Supply voltage | Suitability for integration | Available filter functions | Independent gain adjustment |
|---|---|---|---|---|---|
| [2] | Commercial IC | ±12V | Yes | HP, LP, BP | No |
| [3] | Commercial IC | N/A | Yes | HP, LP, BP | No |
| [4] | 0.35 μm CMOS | ±1.5 | Yes | HP, LP, BP | No |
| [5] | Commercial IC | ±12V | Yes | HP, LP, BP, AP, BS | No |
| [6] | 0.5 μm CMOS | ±2.5 V | Yes | HP, LP, BP | No |
| [7] | 0.25 μm CMOS | ±1.2 V | Yes | HP, LP, BP, BS | No |
| [8] | Commercial IC | ±12 V | No | HP, LP, BP, BS | No |
| [9] | N/A | N/A | No | HP, LP, BP | No |
| Proposed | 0.18 μm CMOS | ±0.9 V | Yes | HP, LP, BP, AP, BS | Yes |

N/A: Not available

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