Highly Efficient Ultra-Compact Isolated DC-DC Converter with Fully Integrated Active Clamping H-Bridge and Synchronous Rectifier

JAN DOUTRELOIGNE
Center for Microsystems Technology (CMST)
Ghent University – IMEC
iGent, Technologiepark 15, 9052 Zwijnaarde
BELGIUM
jdoutrel@elis.ugent.be http://www.cmst.be

Abstract: - An isolated forward DC-DC converter with monolithically integrated electronics at both sides of the pulse transformer is presented. It converts a 48V DC input voltage into a 12V DC output voltage at 7A load current with a 90.8% overall power efficiency, employing an 800kHz switching frequency, and it occupies a physical volume of 55mm x 35mm x 10mm only. The primary winding of the planar pulse transformer is driven by a new 4-transistor active clamping H-bridge circuit topology that significantly reduces the voltage requirements for the DMOS power devices, thereby enabling monolithic integration of the primary-side electronics in an 80V 0.35μm junction-isolated smart-power IC technology. The switching signal at the secondary winding of the planar pulse transformer is converted into a stable DC output voltage by means of a new synchronous rectifier circuit topology that employs an additional DC-DC buck converter and drastically reduces the dynamic switching losses in the DMOS power devices, thereby boosting the power efficiency and enabling monolithic integration of the secondary-side electronics in an 80V 0.35μm junction-isolated smart-power IC technology.

Key-Words: - Active clamping, H-bridge, synchronous rectifier, forward converter, DC-DC converter, isolated converter, integrated circuit, smart-power technology

1 Introduction

In many applications the electronic circuitry is powered by isolated DC-DC converters for safety reasons or other system requirements. Typical examples are the power supplies in central-office DSL telecommunication equipment or the power supply units in Power-over-Ethernet devices. Widely used isolated converter topologies are the fly-back, the forward and the combined forward/fly-back architectures [1,2], where the driving electronics at the primary side of the pulse transformer and the rectifying electronics at the secondary side are employing discrete power transistors (MOSFETs or bipolar devices) and/or diodes [3]. When trying to optimize the power efficiency and reduce the physical size of the system, monolithic integration of the driving and rectifying electronics in an appropriate high-voltage smart-power IC technology seems an attractive approach, but the practical IC design is not straightforward because of extremely stringent specifications imposed to the active devices. This paper describes the single-chip implementation of the driving electronics at the primary side and the rectifying electronics at the secondary side of the pulse transformer, as well as the use of the designed ICs in a highly efficient ultra-compact isolated forward DC-DC converter module for specific application in advanced central-office DSL telecommunication equipment.

2 Forward DC-DC Converter

The basic architecture of an isolated forward DC-DC converter is shown in Fig.1. Switch 1, actually a power DMOS transistor, is the main driving transistor and is activated during the power transfer phase of the clock cycle. During this power transfer phase, energy is transferred from the primary side of the transformer to the secondary side, and the load current is flowing through the synchronously activated transistor 3, which can be replaced by a diode at the expense of increased conduction losses. The load current is reflected to a proportional current in the primary coil, its precise value being determined by the transformer turns ratio. It's important to note that both windings of the pulse transformer are carrying current simultaneously during this power transfer phase, which is an inherent characteristic of the forward converter in contrast to the fly-back converter.

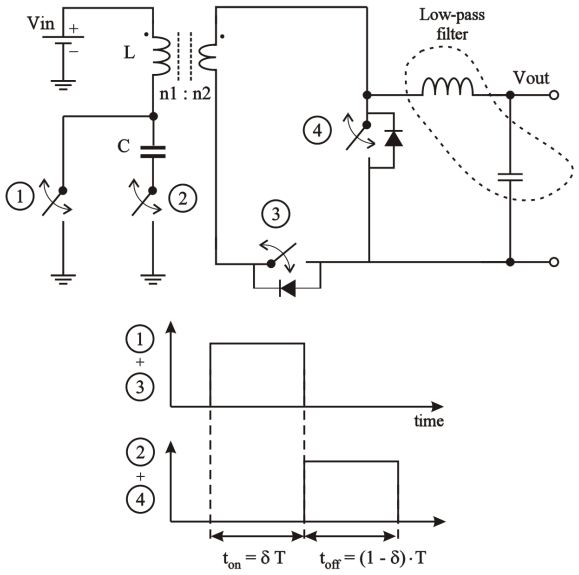

Fig.1: Basic architecture of an isolated forward DC-DC converter.

During this same power transfer phase, a magnetization current is also being built up in the primary coil. The maximum value of this current depends on different factors, mainly the primary coil inductance, the supply voltage, the clock period and the duty ratio, but it's typically much smaller than the reflected load current.

After the power transfer phase, the forward converter enters the active clamping phase where the main transistor 1 is switched off and power isn't transferred anymore from the primary to the secondary side. The load current is now flowing through the synchronously activated transistor or diode 4, acting as a free-wheeling device. The reflected load current isn't present anymore in the primary coil of the pulse transformer, and the magnetization current of the primary coil now has to flow through the branch with the clamping capacitor C and the additional DMOS transistor 2. An appropriate voltage is automatically being built up in this clamping capacitor, creating a polarity inversion of the voltage across the primary coil, so that in steady-state circumstances the magnetization of the primary coil during the power transfer phase is perfectly compensated by the demagnetization of the coil during the active clamping phase of the same clock cycle. The exact value of the voltage on the clamping capacitor depends on the supply voltage of the circuit, and more important, also on the duty ratio of the clock signal.

Due to the presence of the LC low-pass filter, having a 3dB cut-off frequency much below the switching frequency, the converter produces an almost perfect DC output voltage equal to the supply voltage of the primary circuit, multiplied by the transformer turns ratio and the duty ratio of the clock signal.

3 Driving Electronics

We will now examine the possibility of integrating the driving electronics at the primary side of the pulse transformer into a single IC. We will start from the state-of-the-art converter topology shown in Fig.1 and then modify the circuit to make it compatible with monolithic integration.

3.1 Basic 2T Active Clamping Circuit

In the classic converter architecture of Fig.1, the pulse transformer is driven by the basic 2-transistor (2T) active clamping circuit shown in Fig.2. The devices T1 and T2 represent the main driving n-type DMOS transistor and the active clamping p-type DMOS transistor respectively, while the 2 diodes are the built-in drain-bulk diodes of these DMOS devices. The main low-side switch T1 is activated during a fraction δ (the duty ratio or duty cycle) of a clock period T, while the active clamping switch T2 is enabled during the remainder of the clock period.

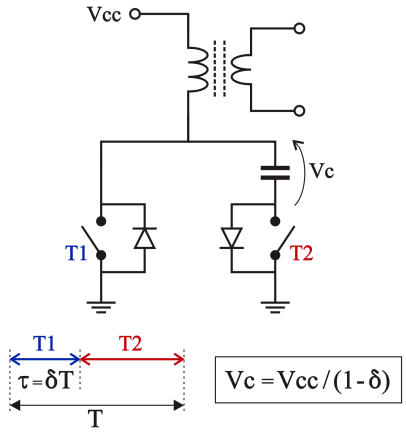

Fig.2: The basic 2T active clamping circuit for driving the pulse transformer.

The equation for the clamping capacitor voltage V_c can be deduced from the observation that in steady-state regime, the average voltage across the primary coil during 1 clock cycle must be zero. When the capacitor value is large enough so that the capacitor voltage V_c can be assumed constant during 1 clock period, the formula for the clamping capacitor voltage V_c as a function of the supply voltage V_{cc} and the duty ratio δ becomes:

$$V_c = \frac{V_{cc}}{1-\delta}$$

It's a very interesting exercise to put some values of the duty ratio into this equation:

$$\delta = 0.25 \rightarrow V_c = 1.33V_{cc}$$
$$\delta = 0.5 \rightarrow V_c = 2V_{cc}$$
$$\delta = 0.75 \rightarrow V_c = 4V_{cc}$$

Apparently, the clamping capacitor voltage increases rapidly with the duty ratio. In a practical application, the duty ratio is typically varied in the range from 0 to 50%, meaning that the internal node voltages can reach levels up to 2 times the supply voltage. E.g. in the specific case of the power supplies in central-office ADSL and VDSL telecommunication equipment where the supply voltage is nominally 48V but can go up as high as 72V according to the specifications, this means that the devices within the circuit should withstand voltages up to 144V, which already makes integration in a smart-power IC technology, i.e. a high-voltage extension of a core CMOS process, rather problematic. And that's not all! During the power transfer phase, the top electrode of switch T2 (i.e. the drain of the p-type DMOS transistor) is polarized to an electric potential of $-V_c$, or in other words, the drain potential of T2 should be able to go 144V negative with respect to the system ground for a duty ratio of 50%. For most junction-isolated smart-power technologies, this is not possible! And even if the technology allows doing so, it means that a total node voltage range of 288V must be tolerated by the IC technology! Obviously, junction-isolated smart-power technologies are no longer an option when such operating voltages are required, but very expensive dielectrically isolated SOI technologies (Silicon On Insulator) must be used instead.

3.2 New 4T Active Clamping Circuit

This issue was thoroughly analyzed in an attempt to reduce the required voltage swing in the circuit, so that integration in a less expensive junction-isolated smart-power IC technology would become possible anyway. This study has lead to an alternative driving circuit topology containing 4 solid-state switches in an H-bridge configuration, where the clamping capacitor is incorporated in one of the 2 branches of the H-bridge. An idealized version of the new 4-transistor (4T) H-bridge driving circuit is shown in Fig.3.

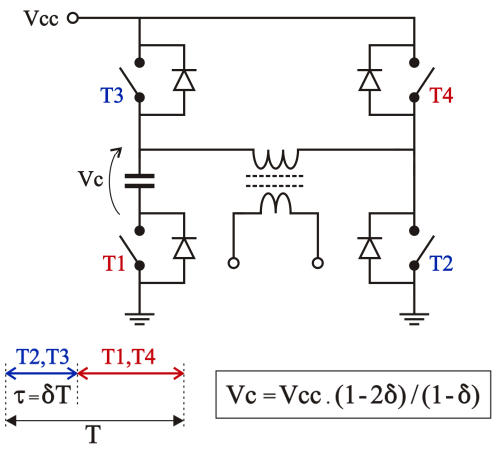

Fig.3: The new 4T active clamping circuit (H-bridge).

During the power transfer phase, the main switches T2 and T3 are activated, thereby connecting the supply voltage V_{cc} directly to the primary transformer coil. During the active clamping phase, on the other hand, the switches T1 and T4 are turned on, causing the clamping capacitor to apply an appropriate voltage with changed polarity across the primary coil and initiating the demagnetization of the coil. When analyzing the operation of this circuit in more detail, it turns out that the voltage and current waveforms in the primary coil are 100% identical to the waveforms in the conventional 2T circuit of Fig.2, and hence, there is absolutely no change in the behaviour of the whole isolated forward DC-DC converter. But there is a very important change in the voltage across the clamping capacitor, caused by the fact that the H-bridge configuration inherently produces a voltage polarity inversion in the primary coil, unlike the 2T circuit of Fig.2 where the polarity inversion entirely relies on the effect of the clamping capacitor. Therefore it's logical that the dependence of the clamping capacitor voltage on the duty ratio behaves very differently in the new 4T circuit of Fig.3 compared to the 2T circuit of Fig.2.

A calculation very similar to the one for the 2T circuit of Fig.2 leads to the following expression of the clamping capacitor voltage V_c as a function of the supply voltage V_{cc} and the duty ratio δ for the new 4T H-bridge circuit of Fig.3:

$$V_c = V_{cc} \cdot \frac{1-2\delta}{1-\delta}$$

Putting some values of the duty ratio into this equation yields:

$$\delta = 0.25 \rightarrow V_c = 0.67V_{cc}$$
$$\delta = 0.5 \rightarrow V_c = 0$$
$$\delta = 0.75 \rightarrow V_c = -2V_{cc}$$

These values prove that the new circuit imposes much less stringent voltage requirements on the switches than the conventional circuit. For a duty ratio in the range from 0 to 50%, the clamping capacitor voltage never exceeds the supply voltage! Moreover, in the same duty ratio range, the node potentials in the circuit never get negative with respect to the system ground. This is of course excellent news when aiming at integration in a junction-isolated smart-power technology!

3.3 Practical Implementation

The presented 4T active clamping circuit from Fig.3 was integrated in a prototype IC employing the 80V 0.35µm I3T80 smart-power technology from ON Semiconductor. The block diagram of the chip is depicted in Fig.4.

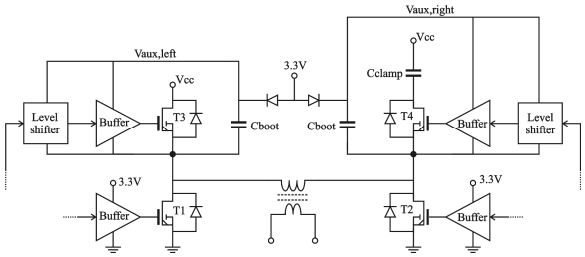

Fig.4: Integrated 4T active clamping circuit.

Apart from the active clamping H-bridge itself, the chip also contains the necessary electronics for controlling and driving the 4 n-type DMOS power transistors, including the bootstrapping circuitry for driving the high-side switches.

The die measures 13.4mm^2 and the IC was packaged in a 7x7mm^2 48-pins TQFP carrier. Experiments revealed satisfactory operation of the developed IC for supply voltages up to 60V and average H-bridge currents up to 2.5A.

4 Rectifying Electronics

As a next step, we will now examine the possibility of integrating the rectifying electronics at the secondary side of the pulse transformer into a single IC. We will start from a conventional discrete implementation of a synchronous rectifier and then modify the circuit to make it compatible with monolithic integration.

4.1 Basic Synchronous Rectifier Circuit

A conventional discrete implementation of the synchronous rectifier at the secondary side of the pulse transformer is depicted in Fig.5. It corresponds to the specific application of a forward DC-DC converter with 48V supply voltage at the input of the pulse transformer and a maximum of 7A load current at a DC output voltage of 12V, as used in central-office ADSL and VDSL telecommunication equipment. The devices nDMOS1 and nDMOS2 correspond to the switches 3 and 4 from Fig. 1. When the pulse transformer produces a positive voltage at its output, the gate of nDMOS1 will be charged directly from the secondary transformer winding through the bipolar transistor NPN1 to a voltage determined by the Zener diode Z1. As a result, nDMOS1 will be in the ON-state, thereby carrying the entire load current at a very small voltage drop. As soon as the voltage polarity at the transformer output has been reversed, the gate of nDMOS1 will be rapidly discharged through diode D1, and consequently nDMOS1 will enter the OFF-state. At the same time, a similar driving circuit will turn on nDMOS2 that will act as an almost ideal free-wheeling diode for the entire load current.

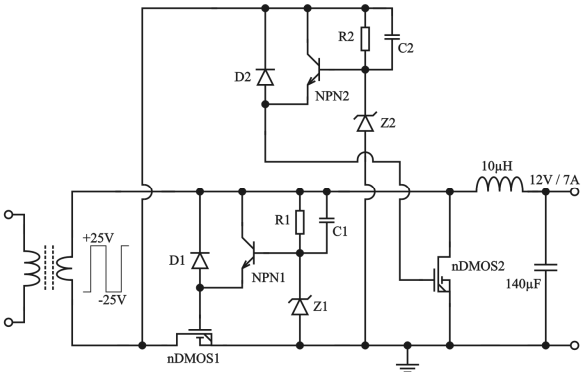

Fig.5: Basic synchronous rectifier circuit.

In an attempt to reduce the total size of the forward DC-DC converter and to improve the overall power efficiency of the system, we looked into the possibility of integrating the synchronous rectifier circuit of Fig.5 into a single silicon chip. In view of the rather high voltage levels at the output of the pulse transformer, a special high-voltage smart-power IC technology is needed. Based on precise

system requirements and constraints, we chose the I3T80 smart-power technology from ON Semiconductor, which is an 80V extension of a 0.35µm CMOS process.

As a starting point, several Spectre simulations were carried out on the circuit of Fig.5 in this I3T80 smart-power technology for different channel dimensions of the 2 main transistors nDMOS1 and nDMOS2. The graph of Fig.6 shows the simulated power efficiency of the basic synchronous rectifier at 7A@12V load conditions, for different chip sizes and different values of the switching frequency. Note that the active switches nDMOS1 and nDMOS2 are by far the dominant components in the total chip size.

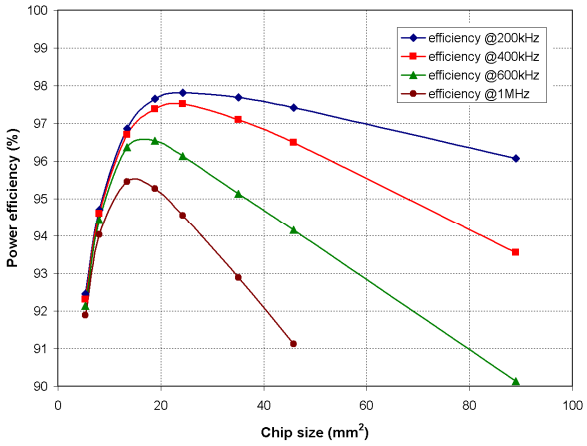

Fig.6: Simulated power efficiency of the basic synchronous rectifier for different chip sizes and switching frequencies.

The shape of the curves in Fig.6 is actually quite logical. Initially, the power efficiency rises steeply for increasing values of the nDMOS channel width because the channel resistance and hence also the static power dissipation in the nDMOS are inversely proportional to this channel width. However, as the channel width goes up, also the gate capacitance of the nDMOS increases, thereby requiring more power in the NPN bipolar transistors to periodically charge this gate capacitance at the switching rate. At a certain critical value of the channel width, this dynamic dissipation in the NPN devices becomes more important than the static dissipation in the nDMOS devices, and from that point on, the power efficiency begins to drop. The higher the switching frequency, the sooner this critical point is reached (because the dynamic losses in the NPN transistors are proportional to the switching frequency) and the steeper the curve will drop.

The contribution of the static dissipation in the nDMOS and dynamic dissipation in the NPN devices is also clear from Table 1, where the parameter M_nDMOS is a multiplier that defines the total effective channel width of the devices nDMOS1 and nDMOS2. Only for rather small values of the nDMOS channel width in combination with a moderate switching frequency, the static nDMOS dissipation is predominant. For very wide nDMOS channels and/or high switching frequencies, the dynamic NPN dissipation has the main impact on power efficiency.

This table leads to a very important conclusion: if we want to improve the power efficiency of the synchronous rectifier at high switching frequencies, we should find a way to reduce the dynamic power losses in the NPN transistors without deteriorating the static losses in the nDMOS devices. In other words, we should look for a circuit solution that reduces the energy needed to charge the gate capacitance of the nDMOS devices without actually reducing the size of these devices!

Component	Average power dissipation (mW)		
	M_nDMOS = 100 @ 200kHz	M_nDMOS = 800 @ 200kHz	M_nDMOS = 200 @ 1MHz
nDMOS1	**1120**	360	890
nDMOS2	**1130**	460	910
NPN1	70	**1240**	**1540**
NPN2	70	**1240**	**1530**

Table 1: Contribution of different transistors in the total power dissipation for different nDMOS sizes and switching frequencies.

4.2 Dynamic Power Loss Reduction

When looking at the way the gate capacitance of the nDMOS transistors is being charged by the NPN bipolar transistors in the circuit of Fig.5, it becomes clear that this is done very inefficiently. Indeed, the gate of the nDMOS devices is charged to about 3.3V, being the maximum allowed gate voltage in this 0.35µm I3T80 technology, but this is done through the NPN devices from a 25V power supply (the voltage across the secondary winding of the pulse transformer)! From an energetic point of view, this is a very bad strategy. To illustrate this and to show how we can improve things considerably, let's have a look at Fig.7.

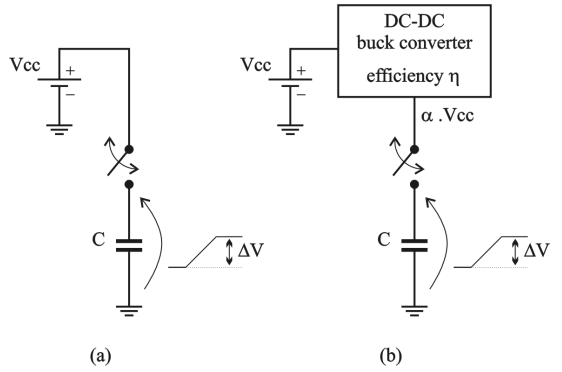

Fig.7: Principle of dynamic power loss reduction.

In circuit (a), the capacitor is charged an amount ΔV from a much higher supply voltage V_{cc} through some solid-state switch. In the circuit of Fig.5, ΔV would be 3.3V, V_{cc} would be 25V, and the switch the NPN bipolar transistor. A very simple calculation shows that the corresponding energy delivered by the supply voltage V_{cc} during the charging process is given by:

$$\Delta E = C \cdot V_{cc} \cdot \Delta V$$

In configuration (b), however, the supply voltage V_{cc} is first down-converted to a level $\alpha \cdot V_{cc}$ slightly above the needed range ΔV (in Fig.5, $\alpha \cdot V_{cc}$ could be e.g. 4V, leaving some margin), and this is done by means of a power-efficient switching DC-DC buck converter having a power efficiency η (e.g. 80%). In this case, the energy delivered by the source V_{cc} during the charging process becomes:

$$\Delta E = \frac{\alpha \cdot C \cdot V_{cc} \cdot \Delta V}{\eta}$$

When we substitute the above mentioned values that correspond to the circuit of Fig.5 into these formulas, we see that the energy consumption in configuration (b) is 5 times less than in the case of configuration (a)! This seems a very interesting approach for boosting the power efficiency of the synchronous rectifier at high switching frequencies and/or for large nDMOS devices. In this way, the original circuit from Fig.5 is transformed into the improved circuit of Fig.8. In this new version, the auxiliary supply voltage of 4V is not directly derived from the 25V transformer voltage, but from the 12V output voltage instead. During start-up, when the output is still far below the desired 12V, the DC-DC buck converter won't operate properly, and hence, the 2 nDMOS devices will entirely rely on their built-in drain-bulk diodes for rectifying the voltage from the pulse transformer. As the output voltage begins to rise, the DC-DC buck converter comes into action, and hence, the nDMOS devices get activated with a high degree of power efficiency.

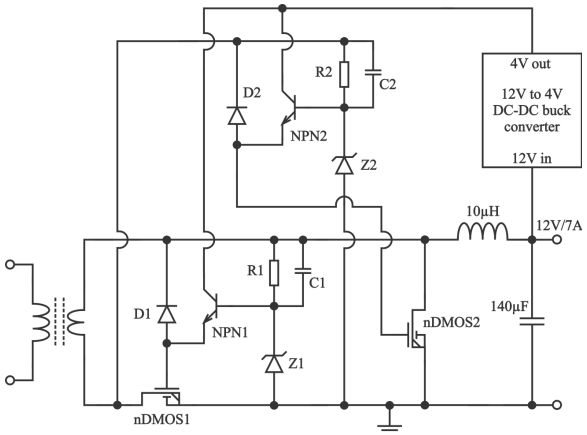

Fig.8: Synchronous rectifier with reduced dynamic power losses.

The impact of this technique to reduce the dynamic switching losses is really astonishing, as evidenced by the simulated data in Table 2. In those situations where the dynamic losses in the NPN devices were predominant in the power consumption of the original circuit (for very large nDMOS devices and/or high switching frequencies), the introduction of this new technique makes the dynamic losses in the NPN devices only marginal compared to the static losses in the nDMOS transistors! Note that the additional average power consumption of about 170mW in the active components of the 12V to 4V DC-DC buck converter are taken into account in the Spectre simulation of the efficiency in Table 2.

Component	Average power dissipation (mW)			
	M_nDMOS = 800 , @ 200kHz		M_nDMOS = 200 , @ 1MHz	
	Basic circuit	Improved circuit	Basic circuit	Improved circuit
nDMOS1	360	370	890	850
nDMOS2	460	510	910	860
NPN1	**1240**	**160**	**1540**	**180**
NPN2	**1240**	**160**	**1530**	**180**
Global power efficiency	**96,1%**	**98,1%**	**94,6%**	**97,0%**

Table 2: Impact of dynamic power loss reduction on transistor power dissipation and global power efficiency.

Fig.9 represents the simulated global power efficiency of the synchronous rectifier from Fig.8 (including also a novel technique for effective sub-threshold current suppression in the nDMOS transistors) for different chip sizes and switching frequencies, and compares it to the data that correspond to the original synchronous rectifier circuit from Fig.5.

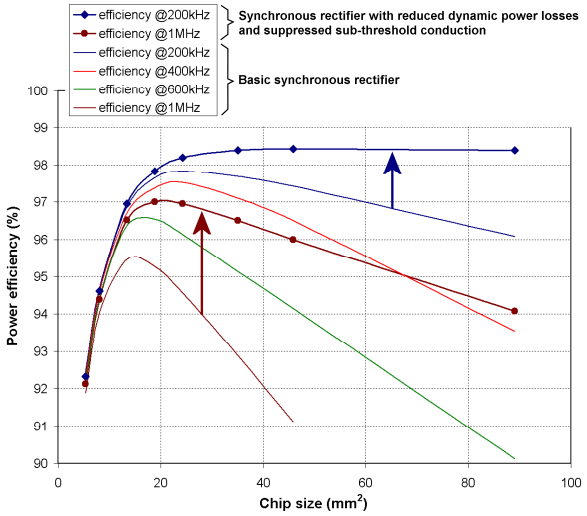

Fig.9: Simulated power efficiency of the synchronous rectifier with reduced dynamic power losses (plus comparison with basic synchronous rectifier) for different chip sizes and switching frequencies.

This comparison reveals the superior performance of the circuit from Fig.8. When looking at a switching frequency of 1MHz, the original circuit yielded a maximum efficiency of 95.5%, whereas the introduction of the technique for dynamic power loss reduction boosts the power efficiency to 97.0%! At frequencies above 1MHz, the efficiency increase would be even more pronounced.

4.3 Practical Implementation

The presented improved synchronous rectifier circuit from Fig.8 was integrated in a prototype IC employing the 80V 0.35µm I3T80 smart-power technology from ON Semiconductor. The die measures 24.5mm^2 and the IC was packaged in a 10x10mm^2 64-pins TQFP carrier. Experiments revealed satisfactory operation of the developed IC for output currents up to 8A.

5 Prototype DC-DC Converter

The presented prototype ICs with the new 4T active clamping circuit from Fig.3 and the improved synchronous rectifier circuit from Fig.8 were incorporated in several prototype DC-DC converter modules in order to evaluate their performance under real operating conditions and to assess their impact on the overall DC-DC converter performance. Fig.10 shows an example of a DC-DC converter PCB where the synchronous rectifier IC in its 64-pins TQFP package is clearly visisble in the centre of the photograph.

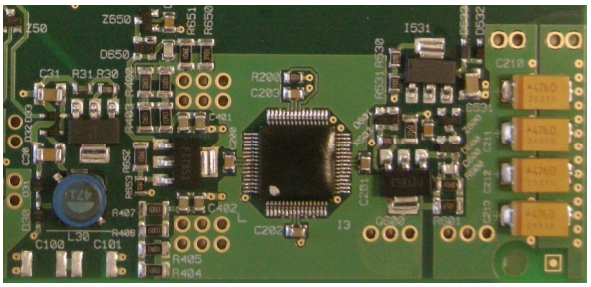

Fig.10: Photograph of a DC-DC converter PCB exhibiting the monolithically integrated synchronous rectifier IC in the centre.

One specific implementation concerns an isolated forward DC-DC converter for use in central-office DSL line access multiplexer cards. It converts a 48V DC input voltage into a 12V DC output voltage at 7A full-load output current (i.e. 84W full-load output power) for powering all electronics on such DSL line access multiplexer cards from the standard 48V DC bus. Thanks to the monolithic integration of the primary-side and secondary-side electronics and the use of a specifically designed planar pulse transformer, an ultra-compact 84W DC-DC converter module was achieved, measuring 55mm x 35mm x 10mm only.

Apart from the physical size, also the overall power efficiency is an extremely important figure of merit for power converter modules. Fig.11 shows the measured overall power efficiency of this 84W DC-DC converter module as a function of the load current (at constant 12V output voltage) and the DC input supply voltage, while using a switching frequency of 800kHz for driving the planar pulse transformer. Under full load conditions (7A load current at 12V DC output voltage) and employing the nominal 48V DC supply voltage, an excellent overall power efficiency of 90.8% is achieved, which is about 5% higher than state-of-the-art DC-DC converters that have similar electrical characteristics and employ discrete DMOS power devices at both sides of the pulse transformer rather than monolithically integrated electronics.

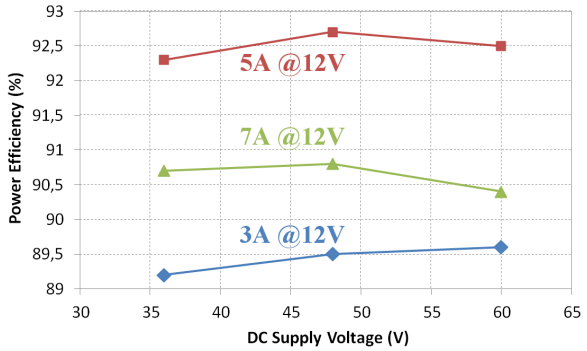

Fig.11: Measured overall power efficiency of the developed 84W DC-DC converter module as a function of load current and DC supply voltage, using an 800kHz switching frequency.

6 Conclusion

New circuit configurations for the monolithic integration of the driving and rectifying electronics in an isolated forward DC-DC converter were presented. At the primary side of the pulse transformer, a new 4-transistor active clamping H-bridge topology exhibits significantly reduced voltage requirements and allows monolithic integration in a junction-isolated smart-power IC technology. At the secondary side, a new synchronous rectifier circuit employing an additional DC-DC buck converter for driving the nDMOS transistors, is also compatible with a junction-isolated smart-power IC technology and reduces the dynamic switching losses, thereby boosting the power efficiency considerably.

The driving and rectifying electronics were both successfully integrated in the I3T80 junction-isolated smart-power technology from ON semiconductor, being an 80V high-voltage extension to a standard 0.35µm CMOS process. Based on these 2 chips and a specifically designed planar pulse transformer, a complete isolated forward DC-DC converter module was developed for application in central-office DSL line access multiplexer cards. It converts a 48V DC input voltage into a 12V DC output voltage at 7A load current with a 90.8% overall power efficiency, employing an 800kHz switching frequency, and it occupies a physical volume of 55mm x 35mm x 10mm only.

References:

[1] L. Bor-Ren et al., Analysis and implementation of an active clamp ZVS forward converter, *IEEE International Conference on Industrial Technology (ICIT)*, 2005, pp. 1427-1432.

[2] F. A. Himmelstoss et al., Comparison of a new combined four-diode forward-flyback converter with the classical forward converter, *International Symposium on Signals, Circuits and Systems (ISSCS)*, 2009, pp. 1-4.

[3] L. Bor-Ren et al., Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier, *IEEE Transactions on Circuits and Systems I,* 2006, Vol. 53, No. 6, pp. 1310-1319.