Neutral Point Potential Balance of Three Phase Three Level Diode Clamped Inverter

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Abstract: - This paper presents a simple method to control the neutral point potential (NPP) variations in three phase three level diode clamped multilevel inverters and also eliminate imbalance in the dc link. Phase Disposition (PD) PWM technique is used for generating the gate pulse for the switches. Two different controllers are used in this method. One for dc side control and the other is for load side control. The Performance parameters are analyzed for different controllers like PI and Fuzzy Logic controller and the results are summarized in the table. The Circuit is simulated in Matlab/Simulink and the effect of the Total Harmonic Distortion (THD) is analyzed. The simulation result confirms the effectiveness of this method to control the neutral point potential variation.

Key-Words: - Multilevel inverter, Phase Disposition (PD), Total Harmonic Distortion (THD), Pulse Width Modulation (PWM), Neutral Point Potential (NPP)

1 Introduction

Multilevel inverters are now well established technology for high voltage and high power applications [26]. Multilevel inverters are classified into three different types they are Diode Clamped, Cascaded H-Bridge and Flying Capacitor Multilevel inverter [1],[8],[9]. Diode Clamped Multilevel inverter has been widely used in industries because it has several benefits such as harmonic reduction, reduced stress across switching devices, and attain high-voltage and high-power capabilities without trouble in series–parallel connections of switching devices [3],[23]. Despite its several advantages it has frequent problem of DC link capacitor voltage imbalance due to the imbalance in the load [17].

Oscillations in the neutral point (NP) potential (NPP) is occurring due to the unbalance dc-link voltage and requires increased dc bus capacitance [4],[14]. It also distorts the inverter output voltage. To acquire full benefit of this uncomplicated structure the voltage across each dc-link capacitor should be restricted to half of the total dc-link voltage, therefore the NPP must be either strictly regulated or set to be zero [5],[6].

Several control techniques are proposed in the literature in order to control the neutral point potential and maintain the capacitor voltage balance with minimum ripples are discussed as follows [7].

SVPWM technique uses redundant switching states to control the NPP [11].But the relationship between NPP and the redundant switching state is very complicated [19]. Most of the other scheme requires load power factor angle, load voltage and load current measurements [22],[25].

Many carrier based PWM techniques like Phase shifted and Level shifted PWM are implemented to generate the waveforms of load voltage and load current with the reduction in THD [21]. But the issue of NPP is not discussed [16],[18],[20].

The analysis and design of NPP regulator is proposed [2] but it has the drawback of having high amount of lower order harmonics [10],[13].

Reduced Switching Loss technique based SPWM has been proposed in [24] which do not include the NPP variations [12],[15].

This paper proposes the simulation of three level diode clamped inverter employing a sine wave is compared with the carrier signal to generate pulses for the switches. Two controllers are used in this method. One for load voltage control and the other is for dc voltage control. From the load voltage control loop the three phase reference modulating signal is generated is added to the offset voltage generated by the DC-link voltage control loops to generate the three level waveform. This offset voltage not only eliminates the imbalance present in

the dc link and also eliminate the lower order harmonics.

Section 2 describes the structure and the operation of three level diode clamped inverter. Section 3 presents the block diagram and the operation of the controllers. Section 4 presents the simulation results. Results and discussions are presented in Section 5.

2 Structure of Three Level Diode Clamped Inverter

Three Level Diode Clamped inverter Consists of twelve switches and six fast recovery diodes with two DC-link capacitors are shown in figure1.

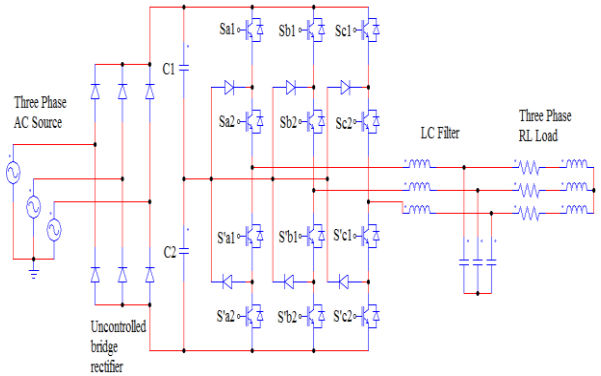

Figure 1. Three Level Diode Clamped Inverter

Sinusoidal PWM technique (SPWM) is used for generating the gate pulse for the twelve switches. For three level inverters, two carrier signals are used. In this SPWM technique sine wave is taken as the modulating signal (50Hz) and it is compared with the two high frequency carrier signals (2KHz) and the resultant gate pulse is produced which is given to the corresponding switches of the inverter to produce the three level waveform.

Table 1. Switching Sequence of Three Level Diode Clamped Inverter

S. No	Switching States				Switching States	Output Phase Voltage (Vao)
	Sa1	Sa2	S'a1	S'a2		
1	1	1	0	0	+	+(V/2)
2	0	1	1	0	0	0
3	0	0	1	1	-	-(V/2)

Passive LC Filter is connected between the inverter and the load to eliminate the higher order harmonics and the ripples present in the output voltage waveform.

3 Control Scheme of NPP Regulator

The Control scheme of the proposed regulator has been analyzed in both open loop and closed loop control system.

3.1 Open loop Control

The block diagram of the open loop control of three level diode clamped inverter is shown in Figure 2. It consists of three phase ac source it is connected to the uncontrolled six pulse bridge rectifier to obtain the pulsating dc voltage. The pulsating dc voltage is given as input to the three level diode clamped inverter which consists of 12 switches and the two dc link capacitors which is confined to the half of the dc voltage.

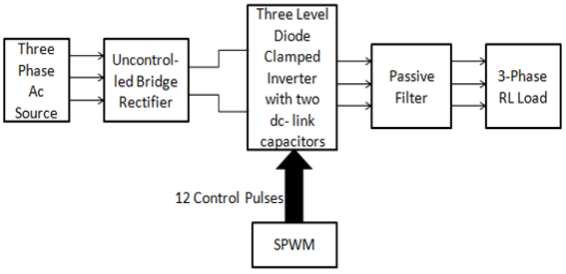

Figure 2. Block Diagram of Open loop Control

Normally in an open loop system there is no feedback is provided. If there is any disturbance occurred at the load side, it cannot be sensed by the source side. Therefore the system is not stable and we cannot control the neutral point potential in this method.

3.2 Closed loop Control

Closed loop control in three level diode clamped inverter is done by using three different methods which are discussed as follows.

3.2.1 Load Side PI Controller

The block diagram of Load side PI Controller is shown in Figure 3. Load side PI Controller aims to stabilize the load voltage control. Three phase voltage is sensed and converted into per unit quantities. These per unit quantities are converted to dqo transformations using three phase to two phase transformation. These dqo values are compared with reference values the error is generated which is processed through a controller then again the two phase values are converted into abc using two phase to three phase transformation then the reference

V*abc is given as input to the three level PWM generator which generates the pulses for the switches.

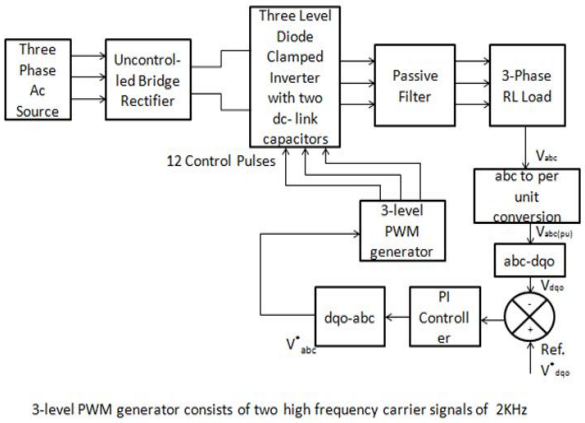

Figure 3. Block Diagram of Load side PI Controller

In load voltage control loop method PI controller is used which is used to control the load voltage only it does not able to control the neutral point potential.

3.2.2 DC Side PI Controller

The block diagram of three level diode clamped inverter with the dc-link voltage control loop is shown in figure 4. From the dc voltage loop, the difference between two dc-link voltages (i.e., Vnp = Vdc1−Vdc2) is calculated, and the error is processed through the PI controller. Then, the variable offset voltage signal Voff is generated.

A continuous variable offset Voff voltage regulates the midpoint potential of the dc bus and corrects any existing imbalance in the dc link. This offset voltage Voff is added to the three phase sinusoidal reference signal Vabc a new reference signal is generated.

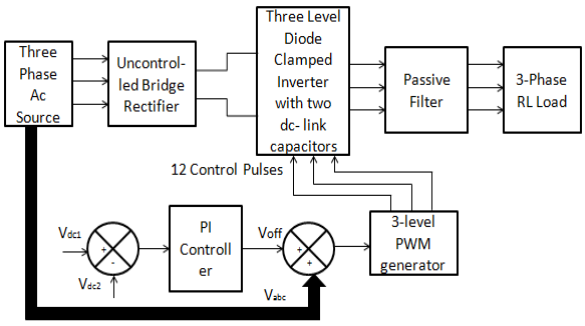

Figure 4. Block Diagram of DC side PI Controller

The new reference signal is given as input to the 3-level PWM generator which consists of two high frequency carrier signals 2 KHz. The reference signal is compared with the carrier signal and produces the gate pulses for the switches of the inverter to produce the three level output waveform.

In dc-link voltage control loop method the neutral point potential is minimized up to some extent by adding the offset voltage to reference signal.

But the drawback in this method only the input side is controlled and the load side voltage is not controlled. Due to these reasons, if any disturbance is occurring at the load side will make the system unstable.

3.2.3 Combined Load Side PI Controller and DC Side Fuzzy Controller

The block diagram of load side PI controller and the dc side fuzzy controller shown in figure 5.

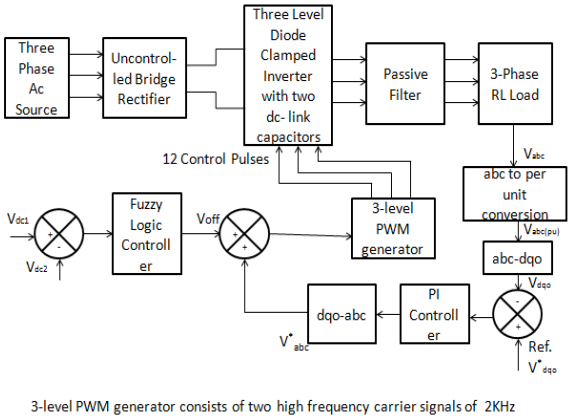

Figure 5. Block Diagram of Load side PI Controller and DC Side Fuzzy Logic Controller

The difference between the upper capacitor and the lower capacitor then the error is produced. It is processed through fuzzy controller. The fuzzy controller has two inputs error and change in error (ce) and has one output variable. The rules are framed to perform the desired operation. The error variable has five membership functions (NB,NS,ZE, PB,PS).The change in error has three variables (NB,ZE,PB).Therefore five rules are framed that is shown in table 2.

Table 2. Fuzzy rule base matrix

e / ce	NB	NS	ZE	PS	PB
NB	NB	NS	ZE	PS	PB
ZE	NB	ZE	ZE	ZE	PS
PB	NB	NS	ZE	PS	PB

$$F(n) = e(n) - ce(n) \quad (1)$$

F (n) =resultant matrix
e (n) =error
ce (n) =Change in error.

V*abc is generated from the load side, it is compared with the output from fuzzy logic controller then the new reference signal is generated which is given to the three level PWM generator which produce the desired switching pulses for the inverter. The NPP oscillation is very high in this method.

3.2.4 Combined Load Side PI Controller and DC Side PI Controller

The block diagram of load side PI controller and the dc side PI controller shown in figure 6.

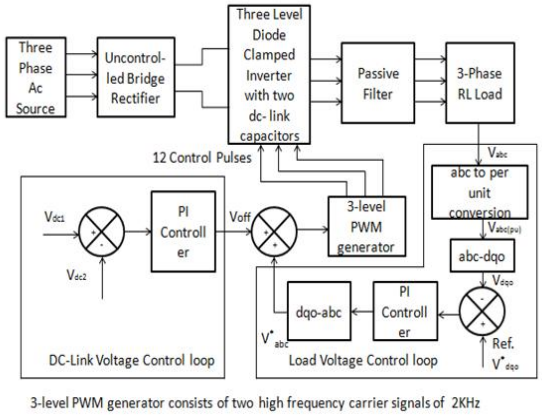

Figure 6. Block Diagram of Load side PI Controller and DC Side PI Controller

It is the combination of both load side PI Controller and DC Side Controller. In this method the reference modulating Signal V*abc is generated from load side is added to the offset voltage is generated from dc side and the new reference signal is produced which is given as input to 3-level PWM generator to generate the control pulses for the switches.

In this method the neutral point potential is well minimized compared to the above four methods and the voltage between the two capacitors is well balanced and the inverter voltage and current harmonics are minimized.

4 Simulation Results

The software simulation is conducted on Matlab simulation software, a widely used simulation for industrial applications. The PWM control unit, IGBT based diode clamped inverter unit as well as the LC filter will be constructed using Matlab to simulate and evaluate the proposed three level diode clamped inverter schemes on circuit level. The simulation parameters are listed in table 3.

Table 3. Simulation Parameters

S.No	Name of the Component	Rating
1	DC Link Voltage	680 V
2	DC Link Capacitance	2200µF
3	Filter Inductance	5.2 mH
4	Filter Capacitance	100 µF
5	Rated line-line Voltage	415 V
6	Frequency	50 Hz
7	Load Resistance	15 Ω
8	Load Inductance	24.2 mH
9	Carrier Frequency	2 KHz

After going through the necessary debugging process to correct various simulation problems or errors confronted during simulation, the simulation results waveform will be generated in the scope display window.

4.1 Open Loop Simulation Results

The outputs obtained from the open loop simulation are shown below.

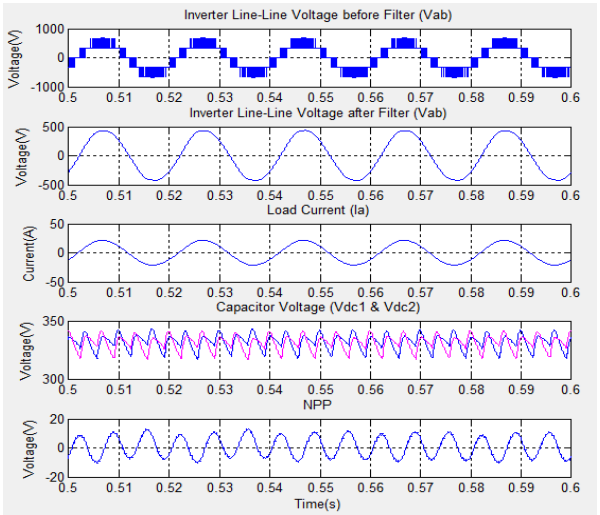

Figure 7. Output Waveforms in open loop

DC-link voltages (Vdc1 and Vdc2), NPP, load voltage, load current, in an open loop control are shown in Figure 7. It clearly indicates a non-zero average value of NPP with high switching density in the capacitor voltage profile and the capacitor voltage is not balanced in this method.

In open loop method even though we achieve the rated voltage and current .This method cannot be used because the feedback element is not provided

so if there is any deviation in the system it cannot be absorbed in this method

The harmonic analysis of the load voltage and the load current in an open loop system is done and the results are shown in figure 8 and figure 9 respectively.

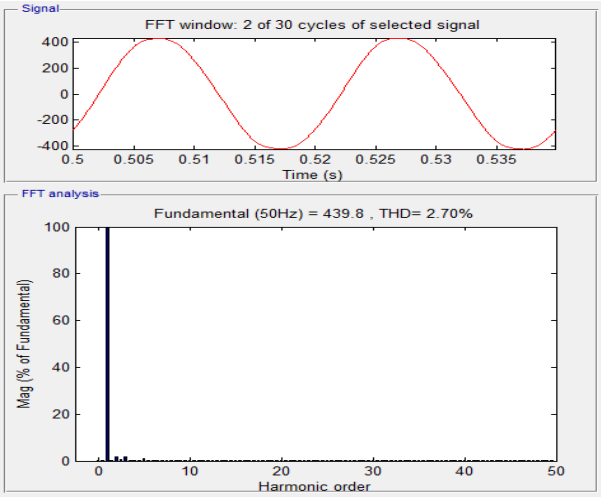

Figure 8. THD of Load Voltage

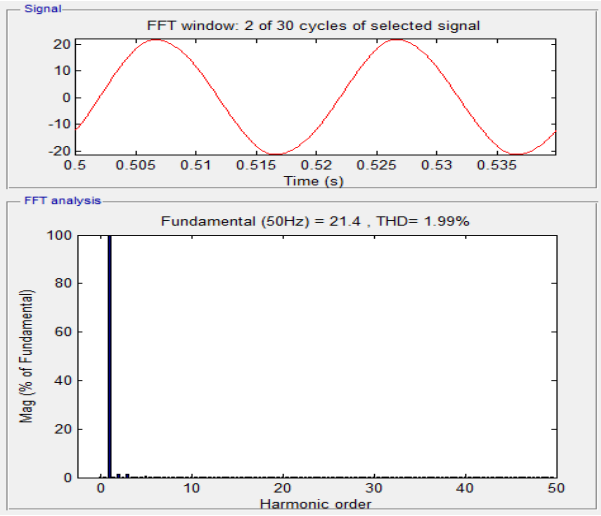

Figure 9. THD of Load Current

By using passive filters the higher order harmonics are eliminated. The THD of voltage and current are well below 5%, but the voltage between capacitors is not balanced.

4.2 Closed Loop Simulation Results

The simulations of closed loop system are done by using four different methods that are briefly discussed in section 3.

4.2.1 Simulation Results of Load Side PI Controller

Figure 10 shows the output waveforms of the load side PI Controller. In this method by using the controller the load voltage is stabilized, then also the capacitor voltage is not balanced.

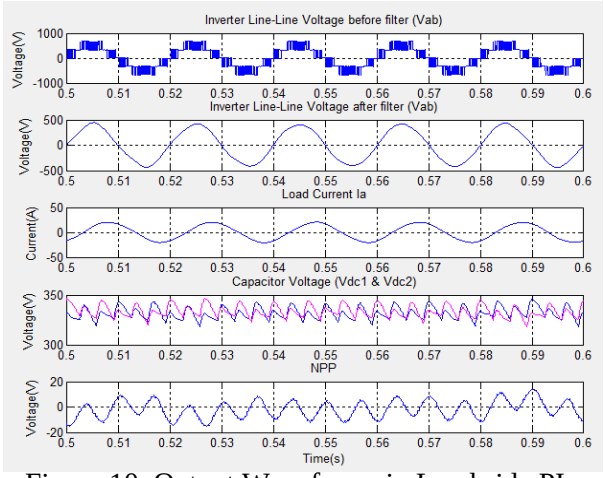

Figure 10. Output Waveforms in Load side PI Controller loop

Due to oscillations in the NPP waveform the voltage difference between the two dc-link capacitors is very high and this will create the imbalance in the dc-link.

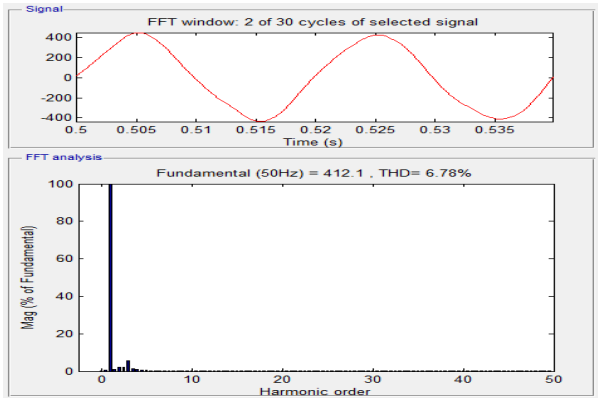

Figure 11. THD of Load Voltage

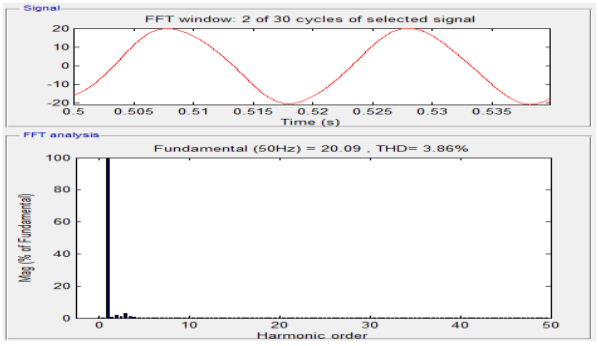

Figure 12. THD of Load Current

The THD of the load voltage and load current are shown in figure 11 and Figure 12 respectively. Higher order harmonics are eliminated, but the THD of load voltage is greater than 5%, which is not maintained as per IEEE 519-1992 standards.

4.2.2 Simulation Results of DC Side PI Controller

In this method the controller is used to control the neutral point potential by generating the offset voltage.

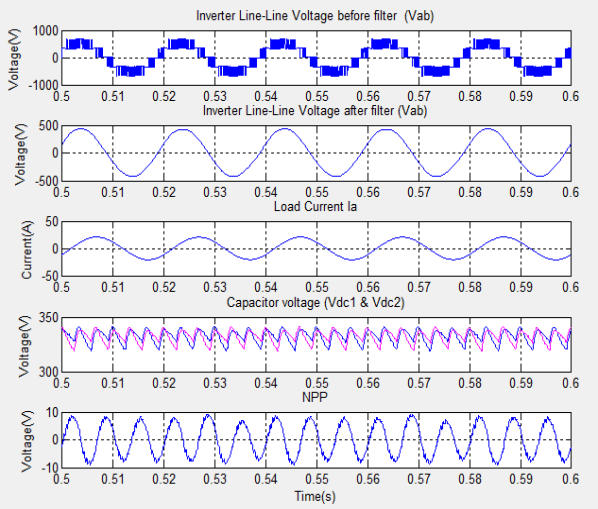

Figure 13.Output Waveforms in DC side PI Controller loop

The oscillations in NPP waveform are minimum compared to the above two methods due to that the voltage difference between the capacitors is very minimum is shown in figure 10. But the drawback in this method there is no feedback provided at the load side so the control of output voltage is very difficult.

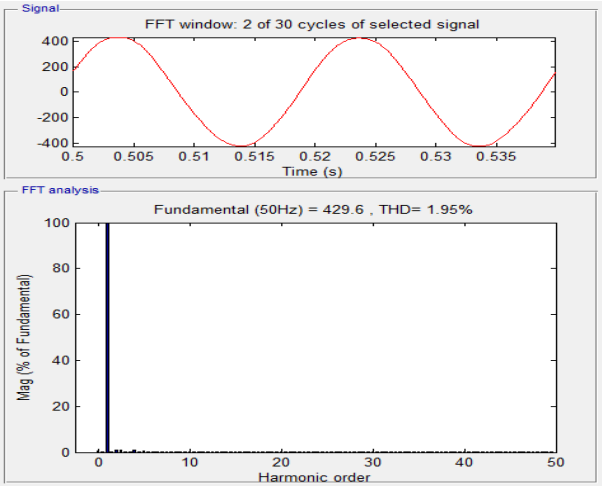

Figure 14.THD of Load Voltage

The THD of the load voltage and the load current is shown in Figure 14 and Figure 15 respectively.

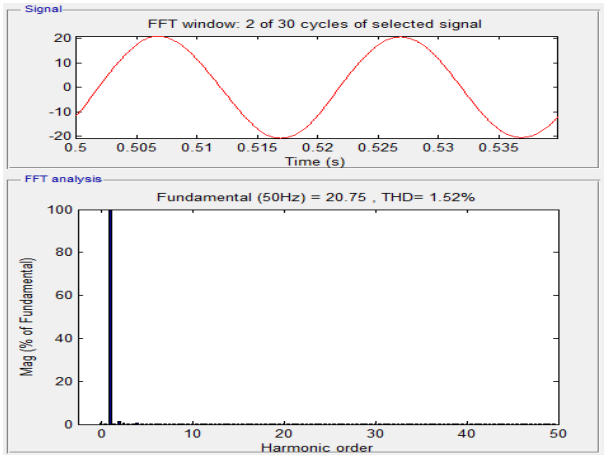

Figure 15.THD of Load Current

The THD of the load voltage and load current are well below 5%, but the drawback is capacitor voltage is not balanced.

4.2.3 Simulation Results of Load Side PI Controller and DC Side Fuzzy Controller

The output waveforms of the load side PI controller and DC side fuzzy logic controller are shown in figure 10.

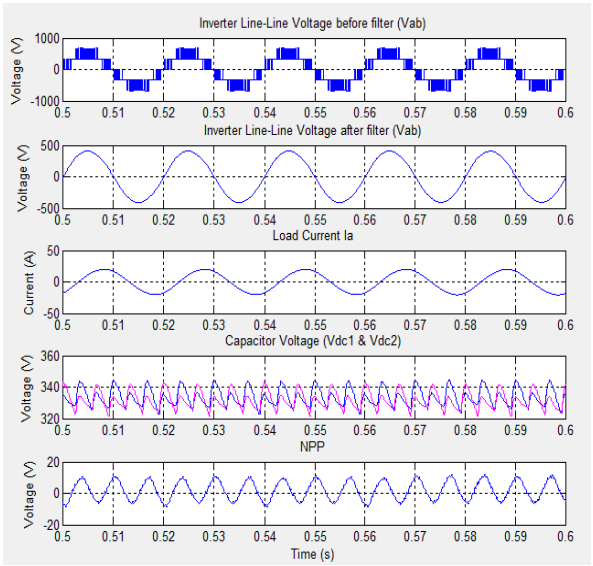

Figure 16. Output Waveforms in load side PI controller and DC side fuzzy controller

DC-link voltages (Vdc1 and Vdc2), NPP, load voltage, load current, without the NPP regulator are shown in Figure 16. It clearly indicates a nonzero average value of NPP with high switching density in the capacitor voltage profile and the capacitor voltage is not balanced in this method.

The harmonic analysis is done for voltage and current and the results are shown figure 17 and figure 18 respectively.

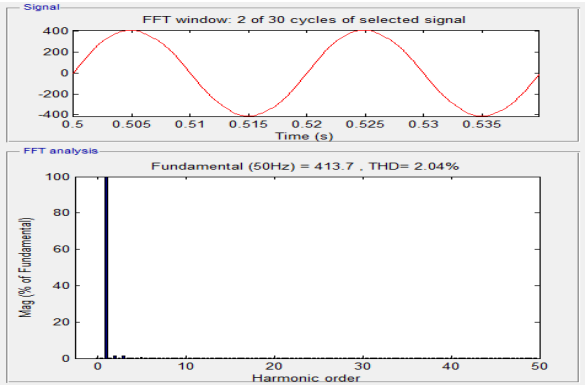

Figure 17.THD of Load Voltage

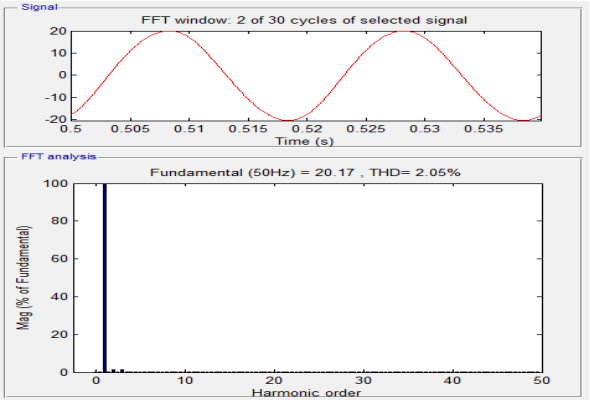

Figure 18.THD of Load Current

4.2.4 Simulation Results of Combined Load Side PI Controller and DC Side PI Controller

In this method two controllers are used to stabilize both the load voltage and dc-link voltage control.

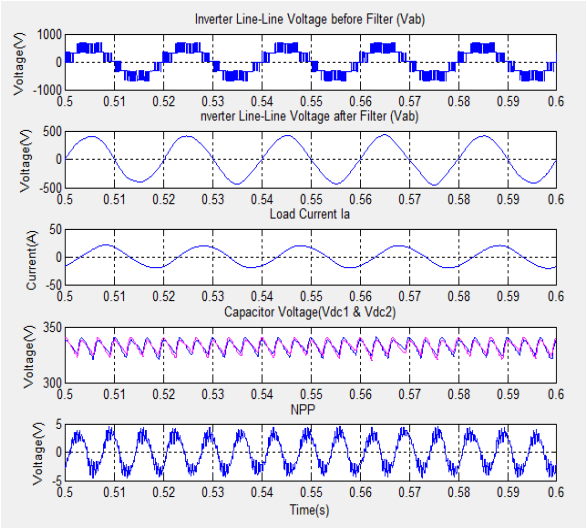

Figure 19.Output waveforms in combined load side PI controller and DC side PI Controller

Due to the average zero value of NPP and also the addition of the offset voltage to the three phase reference signal. The voltage between the two capacitors is almost same and the capacitor voltage is balanced, which eliminates the imbalance present in the dc-link and both the load voltage and the dc-link voltage is well controlled in this method.

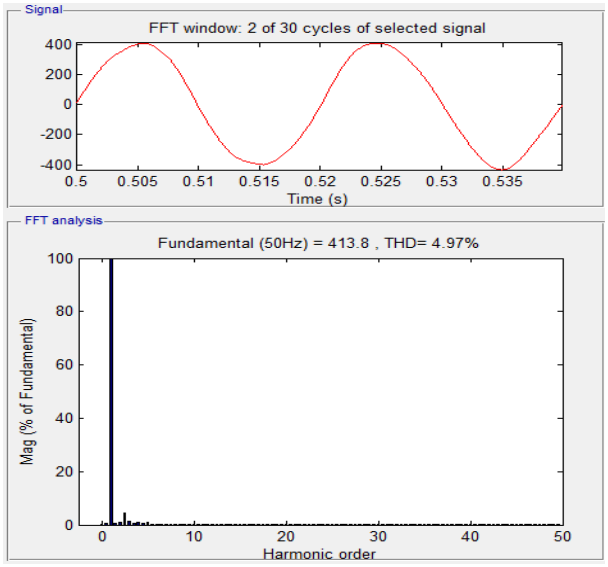

Figure 20.THD of Load Voltage

The harmonics present in the load voltage is shown in figure 20 and the THD is less than 5%.

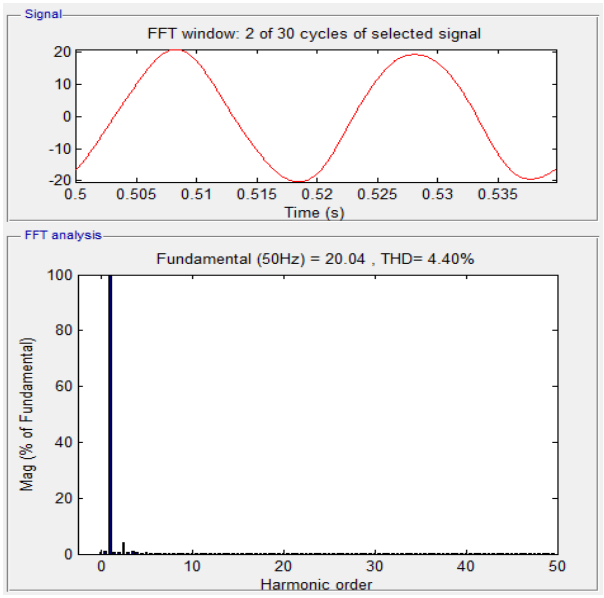

Figure 21.THD of Load Current

Figure 21 shows the line current is somewhat more distorted because of redistribution of charge among two DC link capacitors. Load voltage and current THD are still within the 5 % limit imposed by the IEEE 519-1992 standard.

Table 4. Comparison of Performance Parameters

S.No	Parameters	Different Control Methods				
		Open Loop Control	Load Side PI Controller	DC Side PI Controller	Combined Load Side PI Controller and DC Side Fuzzy Controller	Combined Load Side PI Controller and DC Side PI Controller
1	Fundamental Value of Vab (after filter)	439.8 V	412.1 V	429.6 V	413.7 V	413.8 V
2	Fundamental value of Ia	21.04 A	20.09 A	20.75 A	20.17 A	20.04 A
3	Rms Load Voltage Vab (after filter)	310.98 V	291.3 V	303.7 V	292.5 V	292.6 V
4	Rms load Current Ia	14.87 A	14.20 A	14.71 A	14.21 A	14.36 A
5	Average Neutral Point Potential (NPP)	2.815 V	2.605 V	0.833 V	2.306 V	0.392 V
6	THD of Load Voltage	2.70 %	6.78 %	1.96 %	2.04 %	4.97 %
7	THD of Load Current	1.99 %	3.86 %	1.52 %	2.05%	4.40 %

5 Results and Discussions

The parameters of the three level diode clamped inverter are analyzed with the different methods and the results are summarized in table 4. The open loop control, DC side PI Controller and the combined load side PI Controller and DC side fuzzy Controller are also maintained the voltage and current harmonics are less than 5 %. But the capacitor voltage is not balanced in these methods. Therefore, compared to the other methods Combined Load Side PI Controller and the DC side PI Controller produce better results because the average NPP is 0.392 V and the capacitor voltage is well balanced and THD is maintained as per IEEE 519-1992 Standards.

6 Conclusion

A simple method to control the neutral point potential for a three level diode clamped inverter has been presented in this paper. This method gives the improved inverter performance in terms of dc-link balance with almost zero average NPP. The control of NPP reduces the harmonic contents in inverter voltage and currents. Apart from maintaining the dc voltage balance it also reduces the distortions in the output voltage resulting in the reduction of dc-bus capacitance. The simulated results have been presented to validate the effectiveness of this method.

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