Method of elimination inrush current after connection of high input DC voltage

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Abstract: - This article deals with the problem of elimination inrush currents. The document proposes an active method for limiting the inrush currents during circuit switching when high inrush currents occur. The proposed system limits current in the circuit by means of a series connected Mosfet transistor. The Mosfet transistor is controlled in a linear resistive region. In the case of an inrush current in a circuit, the Mosfet transistor limits the magnitude of the current flowing into the circuit. The article also solves the problem of transistor power load. In the article there is a chapter that deals with the maximum magnitude of the limiting current that can flow through the transistor so as not to destroy it. In this new inrush current limiting configuration, the operator can directly define the amount of surge current that must not be exceeded after the circuit is closed. The proposed system is also complemented by other protective and control elements that are described in this article.

Key-Words: - Power Electronics, Inrush current, MOSFET transistor, limitation, converter

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1 Introduction

With increasing demands on the power of electric motors for various technical sectors (e.g. electric vehicles for traction purposes), the power of power semiconductor converters for connecting these motors is also increasing. As the power of the inverters increases, there is a problem with the inrush current. The problem of inrush current is compounded when using traction battery power used in cars.

The inrush current is the instantaneous input current of a high amplitude circuit that occurs when the circuit is switched on as a result of charging capacitors, inductors and transformers. This inrush current has a large amplitude and can reach currents of up to several tens of kilo-ampere [1] – [4].

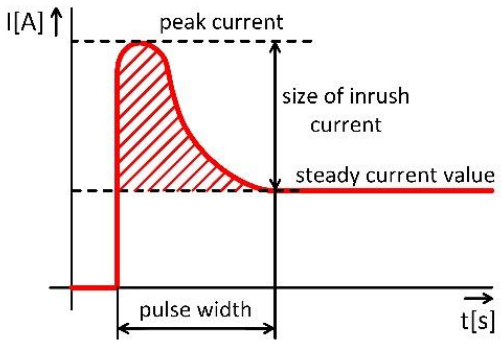

Fig. 1 Current curve when the circuit is switching on (inrush current)

Therefore, it is very undesirable in electrical circuits. In circuits where the inrush current occurs, the elimination of this undesirable phenomenon is solved by increasing the resistance in the circuit. In most cases, a resistor or an NTC thermistor is used to increase the resistance in the circuit. The duration of the inrush currents is of the order of milliseconds, the duration of this action being dependent on the size of the RC members in the circuit. Figure 1 shows an example of the current waveform when in the circuit the inrush current was generated [5] – [8].

The system designed by us solves the elimination of surge currents for the *9kW* inverter, which is used to power supply the asynchronous motor. Input voltage for the inverter is realized by traction batteries with nominal voltage *300V, DC*. The total charge capacity in the circuit is *5mF* and the parasitic resistance in the circuit is estimated at *50mΩ*. In this case, the inrush current would occur during the power on the I_{peak} = *6kA* circuit. This is confirmed by the simulation shown in Figure 2. Since the capacitor at the moment of switching on was a short circuit, the current was limited only by the resistance in the circuit:

$$I_{peak} = \frac{U_{IN}}{R} = \frac{300V}{50m\Omega} = 6[kA] \quad (1)$$

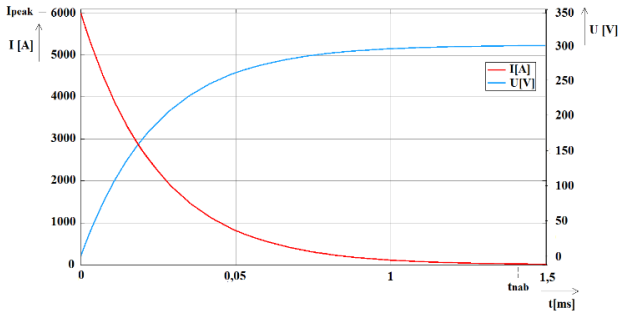

Fig. 2 Simulation of inrush current in the circuit, without limitation

Due to the high inrush current, it is not suitable to use a resistor or an NTC thermistor for limitation. Therefore, we decided to design a system that uses a controlled Mosfet transistor. The advantage of this system is that we can adjust the magnitude of the inrush current. This system can also be used for other circuits that have lower voltage and current parameters for which this system was designed [9].

2 Inrush current limitation with Mosfet transistor

As mentioned above, the inrush current during the initial start-up of the inverter that feeds the asynchronous motor can be limited by the Mosfet transistor. A schematic diagram of this circuit is shown in Figure 3.

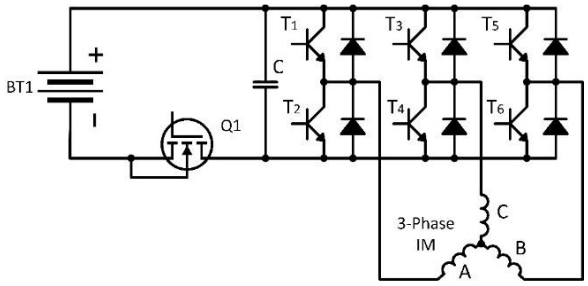

Fig. 3 A schematic diagram of the system

By controlling the transistor in its resistive area, we can reduce the magnitude of the inrush current generated by the charging of the capacitors of the inverter. This method is much more efficient and preferable than using a resistor or NTC thermistor. The advantages of this configuration are:

1.) Possibility to set maximum surge current. The user can set the amount of current which must not be exceeded. This feature allows the designed system to be used for other applications where inrush current limitation is required [10] – [12].
2.) System efficiency. Because it is a power semiconductor converter, we try to make the converter efficiency as high as possible. Therefore, the use of a resistor is not appropriate. We would reduce the efficiency of the inverter. But if we use a Mosfet transistor, we can effectively regulate the power supplied to the DC bus inverter [13].
We can set the amount of current that will be supplied to the circuit, according to the requirements of the application and cancel the restriction after charging. After charging, it will be bypassed. There are no unwanted losses.
3.) Power load of the limiting component. If we used a Resistor to limit the current, the power dissipation at the resistor would be too high.

Example of calculating instantaneous power on the limiting resistor ($P_{dissipation}$), for the proposed application: Supply voltage: $U_{IN} = 300V, DC$; Circuit Capacity: $C = 5mF$; Limiting resistance: $R = 20\Omega$. The effective value of the current in the circuit was: $I_{rms} = 5{,}9A$. Power dissipation is [14]:

$$P_{diss} = R * I^2 = 20 * 5{,}9^2 = 692{,}2[W] \qquad (2)$$

3 Power part design

Figure 4 shows a schematic of the power section of the inrush current limiting system. The power part of the proposed system consists of three main parts. These are active power semiconductor components. The main semiconductor component that provides the whole principle of inrush current limitation is Mosfet transistor. Its control ensures the limitation of the current flow in the circuit. The transistor is active in the case of over currents that occur during circuit switching on.

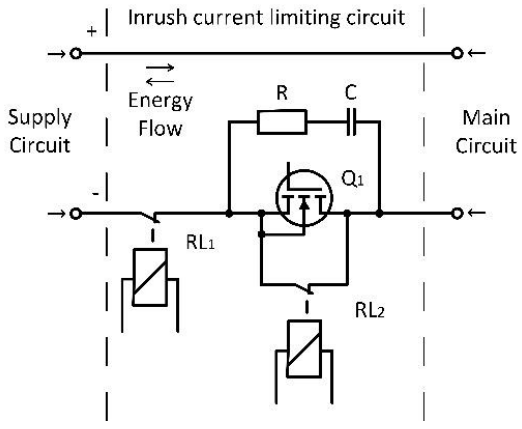

Fig. 4 Power part of the system

Another element in the circuit is relay 2, which serves as a bypass member. Relay 2 is connected in parallel to the transistor and at the moment the inrush current limitation is complete, relay 2 closes and the transistor is bypassed. The third active element in the power section is relay 1, which ensures the overall start and stop of the system. It also serves as a protective relay.

In the power section, an RC snubber is also contemplated to optimize the transistor to avoid failure during operation. The system can conduct current in both directions. Therefore, it is suitable for use in traction applications where we can measure and adjust the amount of current flow.

The power supply of the system is DC voltage. The negative pole of the supply voltage is separated by a relay with a quench chamber. Energy can flow in both directions. From the power supply to the load and from the load to the power supply. During the start of system startup, current flows into the circuit through the transistor. The transistor limits the current to prevent inrush current. Then relay 2 turns on and current flows into the circuit without restriction. Relay 1 is used for galvanic isolation of the system when the system is switched off.

4 Simulation results of the proposed system

The proposed system was simulated in Matlab / Simulink environment. The simulation is based on current limitation during the initial inverter switching on. At this point, high capacity is charging. Figure 5 shows the voltage on the main circuit and the current flowing into the circuit. Using a current limiting transistor, we regulated the current in the circuit to $I = 10A$. Current regulation is by means of a transistor, which is controlled by a PI regulator. Where we suppressed the current from *6kA* to *10A*.

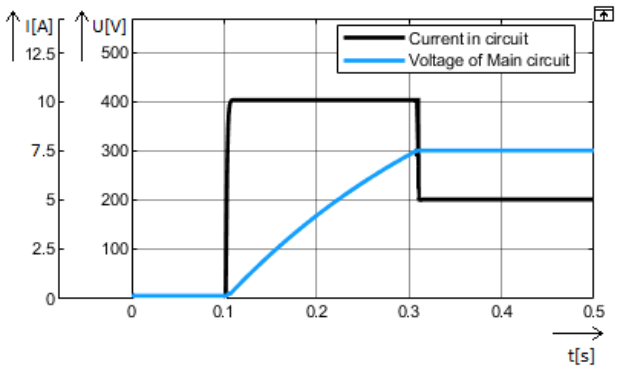

Fig. 5 Simulation of inrush current limitation

Current to the circuit flows only through the transistor. The inrush current was limited to the set value of 10A. This, however, greatly increased the delay time τ. The charging delay time was 0.2 seconds. At 0.31 seconds, the capacitor was charged to 300V and the charging current dropped to a load current of 5A.

Figure 6 shows the waveforms that determine the operation of the transistor and bypass relay.

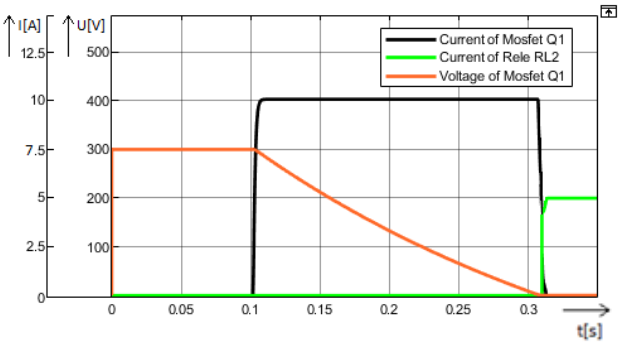

Fig. 6 Conductivity waveforms of transistor and bypass relay

The black waveform shows the current on the transistor that limits the inrush current to *10A*. The orange waveform represents the voltage across the transistor, which gradually decreases, while the voltage across the main circuit increases. The green curve represents the current through the bypass relay. We can see that if the voltage on the transistor drops to zero, the voltage on the main circuit will be equal to the supply voltage. Then the transistor turns off and the bypass relay is turned on, through which the load current flows into the circuit.

Initially, current flows through the transistor into the circuit and the bypass relay is open. During this cycle, the surge current is limited. The transistor limits its size. And the capacitor is gradually charging. After charging the capacitor, the inrush (charging) current disappears. The Mosfet transistor closes and the bypass relay turns on. Subsequently, only the load current flows into the circuit through the relay. The inrush current has been limited and the system continues to operate without restriction.

4.1 Simulation verification of transistor power load

This chapter shows the results of the transistor power load during the current limitation. In the simulation for the limitation, we detected the power losses on the Mosfet transistor at the time the

transistor was in operation using the "*Pe_getPowerLossSummary*" function [15] – [16].

Table 1 shows the Mosfet current through the transistor, the time delay, the power dissipation on the transistor, and the energy on the transistor. The simulation input voltage is $U_{IN} = 300V$. Main circuit capacity is $C = 5mF$.

Table 1. Transistor load simulation varication

I_{lim} [A]	τ [s]	P_D [W]	E[J]
20	0,0785	2853	235,5
10	0,17	1320	255
5	0,304	739	228
2	0,76	295	220
1	1,54	145	230

For the measured loads and time delays, we created a graph of the magnitude of the current through the Mosfet transistor, which can be seen in Figure 7. From the waveform we can see that with increasing current the delay time decreased but the power load of the transistor increased periodically.

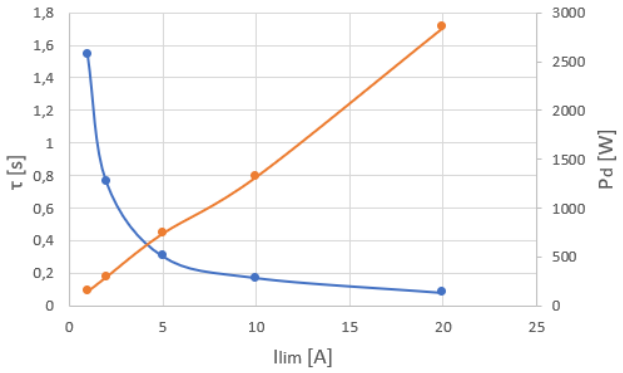

Fig. 7 A waveform to determine the maximum permissible current limiting through a transistor

Using this function, we can determine the maximum current limiting magnitude for a selected Mosfet transistor so that it does not exceed its maximum permissible power load. To prevent Mosfet transistor from straining.

5 System verification on real sample

The proposed system was verified on a real sample. Measurements were performed at reduced parameters. The prototype was created for the experimental verification of system functionality. The thickness of roads and conductive connections of real sample does not correspond to the power load for which the system was designed. Therefore, all experimental measurements were verified at reduced voltage. Figure 8 shows a prototype of the proposed system. The illustration shows the description of each part of the system. The designed system was controlled by a C2000 microcontroller from Texas Instrument TMS 320F28069.

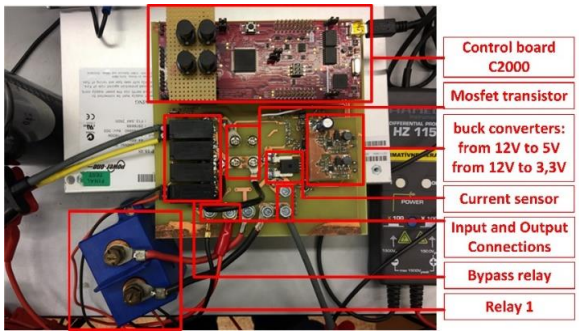

Fig. 8 Real sample of proposed system

Figure 9 shows the waveforms from the inrush current limitation measurement. The inrush current is limited to $I_{lim} = 3,6A$. The main circuit capacity is $C = 4,2\ mF$. Supply voltage is $U_{IN} = 37V$.

We can see from the waveform that the current in the circuit did not exceed the allowed current during charging.

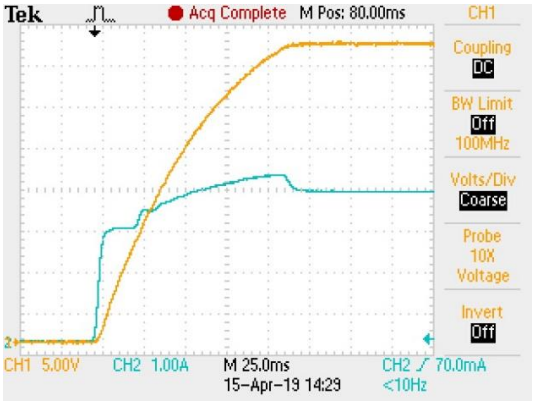

Fig. 9 Inrush current limitation measurement (U_{IN} = 37V)

The yellow waveform represents the voltage on the main circuit. The blue waveform represents the current in the circuit. The main circuit was gradually charged to the supply circuit voltage. After the capacitor was charged, the current in the circuit remained at $I = 4A$. Because the main circuit was loaded with a resistance $R = 9,2\Omega$. The time delay in the circuit was *120ms*.

Figure 10 shows the same measurement, to limit the inrush current as in Figure 9 but with different parameters. The charging capacity is $C = 4,2mF$. The charging current is set to $I_{lim} = 2,9A$ and supply voltage is $U_{IN} = 28V$. The result of this simulation is the same as the previous one. There was no inrush

current in the circuit. The capacitor was gradually charged to the value of the supply voltage.

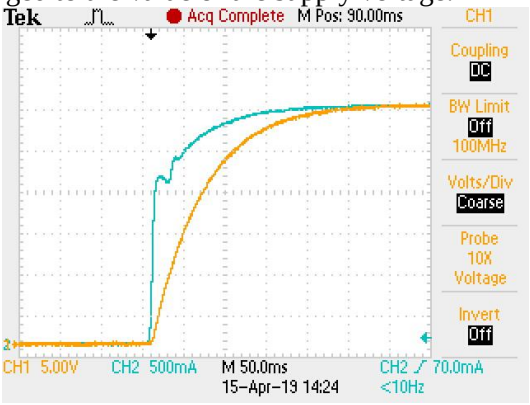

Fig. 10 Inrush current limitation measurement

Figure 11 shows the waveforms of inrush current limitation of a main circuit with the following parameters: $U_{IN} = 70,5V$; $R_{load} = 39\Omega$; $C = 2,2mF$. The yellow waveform represents the voltage on the main circuit, which gradually increased to the value of the supply voltage. The blue waveform represents the voltage on the transistor. This, in turn, drops to zero. The purple waveform is the current in the circuit. The current was limited to $I_{lim} = 1,8A$. The load current in the circuit is $I_{load} = 1,7A$. The green curve represents the current through the bypass relay. From this we can see that the transistor led the current during the inrush current limitation. Then the transistor and the relay led simultaneously. And then only the bypass relay conducts current to the load.

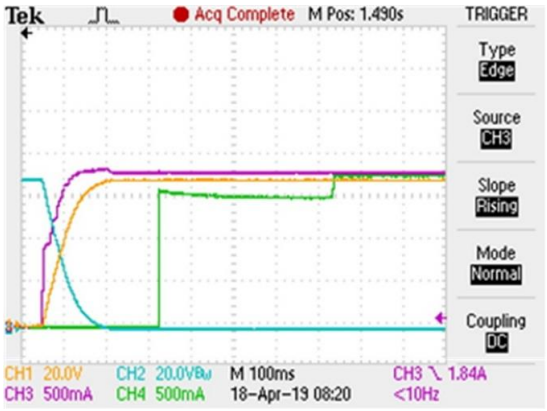

Fig. 11 Measurement of main circuit inrush current limitation

Figure 12 shows a measurement workstation consisting of a power supply, current probes, oscilloscope, multimeter, voltage probes, load resistance, load inductance, auxiliary power supplies and a notebook for communication with the microprocessor.

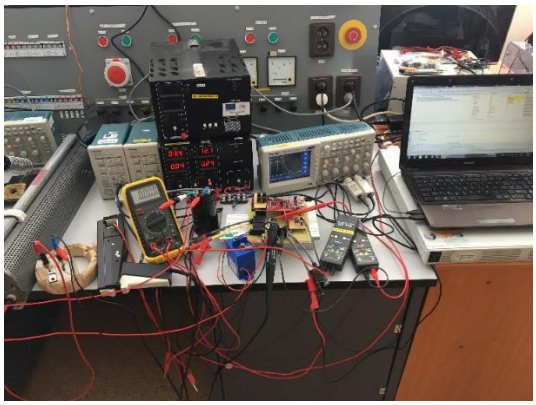

Fig. 12 Measuring workplace

5 Conclusion

This article presents a new design of the inrush current limiting system. It is an effective way of limiting. In the proposed system there is the possibility to specify the magnitude of the maximum inrush current. Therefore, the system can be used for various applications. Current limitation is solved with Mosfet transistor, which provides considerable advantages over conventional methods of limiting inrush current. The proposed system was verified by simulation and on a real sample. Results from simulations and measurements are presented in this article. From the results we can see that the proposed system successfully limits the magnitude of the inrush current during the initial switching on of the main circuit.

6 Acknowledgments

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