A Review of Carrier Based PWM Techniques for Multilevel Inverters' Control

DMITRY BAIMEL[1], SAAD TAPUCHI[1], NINA BAIMEL[2]
Department of Electrical Engineering
Shamoon College of Engineering[1], Sapir Academic College[2]
Beeer-Sheva[1], Hof Ashkelon[2]
ISRAEL
dmitrba@sce.ac.il

Abstract: - This paper presents a review of conventional and novel carrier-based PWM methods that are used for control of multilevel inverters. Among the discussed methods are Phase disposition (PD) PWM, Opposite Phase disposition (POD) PWM, Alternative Phase disposition (APOD) PWM, Phase Shifted PWM and Asymmetrical PWM. The paper shows the simulation results and comparison of these methods.

Key-Words: - Review, Pulse Width Modulation, Inverter, Multilevel, Carrier-based PWM

1 Introduction

There are several pulse width modulation (PWM) switching approaches. The PWM methods could be sinusoidal carrier-based that are applied separately for each inverter phase or space vector, where the switching algorithm is applied for all three phases of the inverter together [1]. The carrier-based PWM methods were the first to be implemented on Medium Volatge inverters (MVI). They were implemented on analog circuits but could also be implemented on digital ones as FPGA or DSP. The multi-level carrier-based modulation is implemented by defining carrier signals and switching rules for the intersection of these carriers with a reference voltage signal [2-5]. The comparison is performed separately for each phase of the inverter. The multi-level inverter of n levels would use n-1 carriers. For example, 12 carrier waves would be used with the present 13-level inverter. This approach works excellently when the carrier frequency is much higher than the modulation frequency, e.g., about fifty to one hundred times higher. However, such higher switching frequencies would also yield rather high switching losses, especially with high power MVI where the switched currents are kA and the switched voltages are kV. Therefore, continuous efforts are made to lower the carrier frequencies together with raising the number of levels in multi-level inverters [6-8].

The paper is organized as foloows: section 2 shows PD, POD and APOD methods and their simulation results; section 3 shows Phase shifted PWM; section 4 shows novel Asymmetrical PWM with simulation results.

2 PD, POD and APOD PWM

There most common carrier based PWMs are the Phase Disposition (PD) PWM, Phase Opposition Disposition (POD) PWM, and Alternative Phase Opposition Disposition (APOD) PWM [9-39]. In the PD PWM method, n-1 identical triangle carrier waves are placed one upon the other and compared to the modulation signal. Generally, the carrier frequency is calculated by:

$$f_{carrier} = 3 * (2k + 1) * f_{modulation} \quad (1)$$

where k is a positive integer.

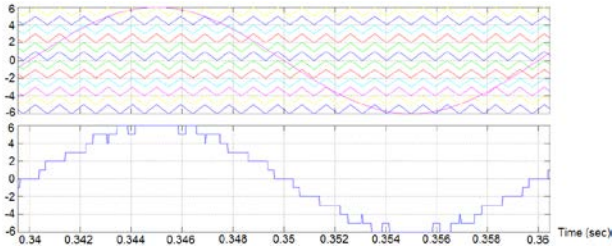


Fig. 1. 13-level carrier-based PD PWM. The modulation and the carrier waves are shown in the upper part of the figure; the obtained PD PWM signal is shown in the bottom of the figure.

It is recommended that the frequency index be an odd number [12]. Furthermore, the phase angle between the carrier and the modulation waves should be the same for all the three phases of the inverter. Therefore, the frequency index should be a multiple of three.

In the POD technique, the triangle carrier waves are placed one above another and there is a phase shift

of 180° between the carrier waves above zero to the ones below.

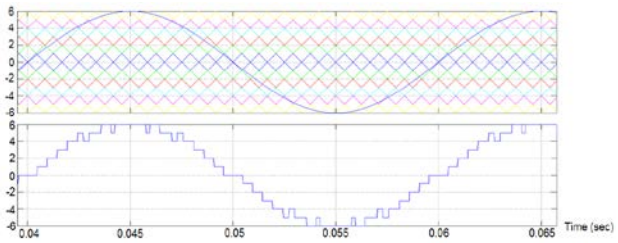


Fig. 2. 13-level carrier-based POD PWM. The modulation and carrier waves are shown in the upper part of the figure; the obtained POD PWM signal is shown in the bottom of the figure.

In the APOD PWM technique, the triangles are placed one above another and there is a phase shift of 180° between each triangle to another.

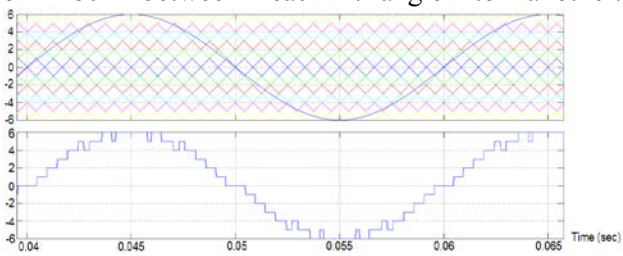


Fig. 3. 13-level carrier-based APOD PWM. The modulation and carrier waves are shown in the upper part of the figure; the obtained APOD PWM signal is shown in the bottom of the figure.

Table 1, 2, 3 show simulation results of PD, POD and POD PWM methods respectively, for different voltage levels. These methods are applied to 13-level cascaded Neutral Point Clamped (NPC) inverter (see Fig.4).The parameters of simulations are: $V_{DC} = 2000\,V$ (per 5-level H-bridge), NPC capacitors $C_1 = C_2 = 1e^{-2}$ F, the load parameters per phase are: $R = 0.019\,\Omega$, L=0.0024 H, and a sinusoidal back electro-motive force (EMF). The back EMF could be changed according to the desired power factor, frequency, and voltage. It is seen that the best results regarding the phase current THDs are obtained with the PD PWM method versus the POD and APOD PWM methods, although the PD carrier frequency (1050 Hz) was smaller than that of the POD and APOD (1200 Hz). It would be worth remembering that a lower carrier frequency means lower switching losses and cooling efforts. The phase and line voltage THD values are rather similar for all carrier based PWM methods.

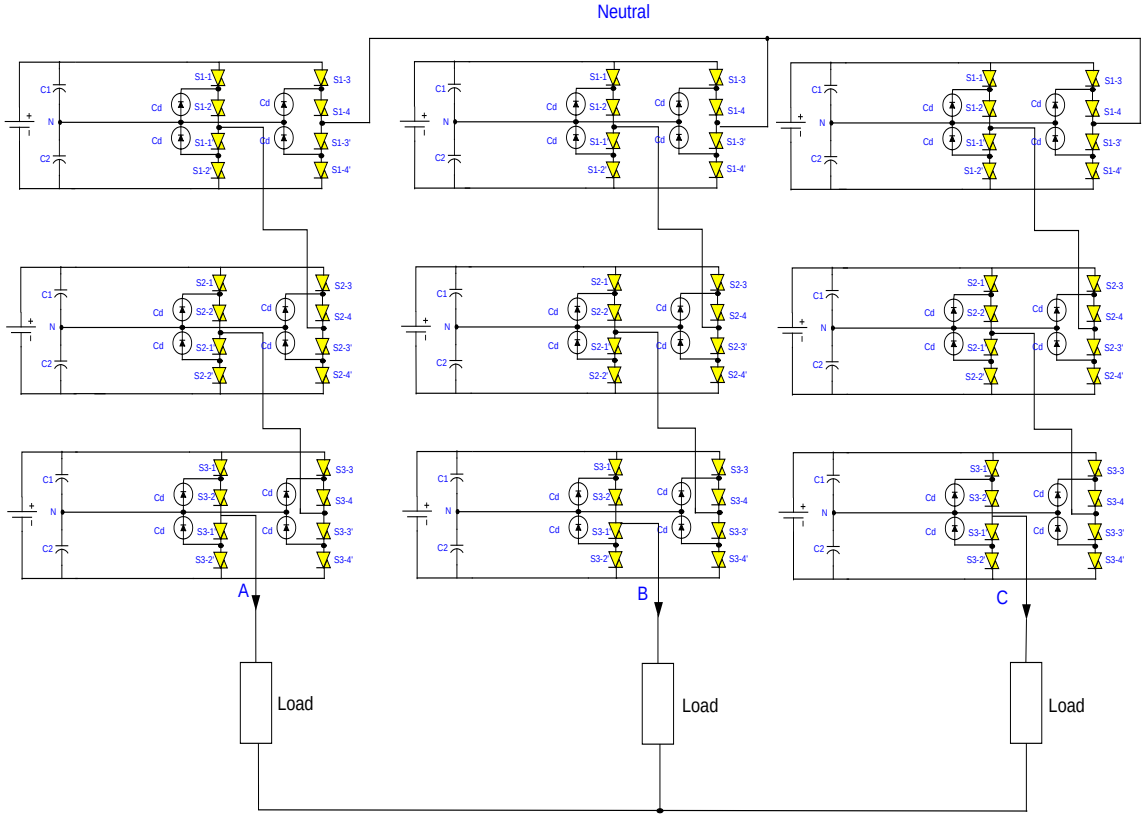


Fig. 4. The 13-level cascaded Neutral Point Clamped inverter.

Table 1. Output voltage and current THD versus the number of levels, modulation frequency is 50Hz, carrier frequency is 1050 Hz, PD PWM.

Modulation index	Inverter level	Phase current THD (%)	Phase voltage THD (%)	Line voltage THD (%)
1	13-level	1.49	8.74	5.1
0.83	11-level	1.25	10.49	6.15
0.67	9-level	1.06	13.27	7.33
0.5	7-level	1.24	17.68	9.97
0.333	5-level	0.88	25.75	15.83
0.167	3-level	0.93	51.41	34.11

Table 2. Simulated output voltage and current THD versus the modulation index, modulation frequency is 50Hz, carrier frequency is 1200 Hz, POD PWM.

Modulation index	Inverter level	Phase current THD (%)	Phase voltage THD (%)	Line voltage THD (%)
1	13-level	1.6	8.49	4.77
0.8	11-level	1.26	11.76	6.25
0.6	9-level	2.34	15.79	7.84
0.4	7-level	0.78	23.21	11.76
0.3	5-level	0.75	32.11	14.87
0.1	3-level	0.54	104.95	44.32

Table 3. Output voltage and current THD versus the modulation index, modulation frequency is 50Hz, carrier frequency is 1200 Hz, APOD PWM.

Modulation index	Inverter level	Phase current THD (%)	Phase voltage THD (%)	Line voltage THD (%)
1	13-level	2.49	8.97	7.17
0.8	11-level	1.97	11.27	8.58
0.6	9-level	1.92	16.07	12.9
0.4	7-level	1.5	22.03	18.15
0.3	5-level	1.96	31.57	25.11
0.1	3-level	2.31	105.5	81.55

3 Phase Shifted (PS) PWM

The conventional PS PWM method is usually used for cascaded H-bridge inverters, while each H-bridge cell is equivalent to a 3-level inverter. Two bipolar opposite triangular carriers are generated for each H-bridge cell. The four switches of the H-bridge are operated according to the comparison between the two triangular carrier waves and a modulation sinusoidal wave[13-14].

The carriers of different H-bridges in the same phase are phase shifted between them (see Fig. 5). The phase shift would be equal to:

$$\phi = \frac{180\circ}{n} \tag{2}$$

where n is the number of H-bridge cells in the inverter. By applying this method, n 3-level PWM signals are generated and summed. Their sum gives a (2n+1)-level PWM signal. The PWM method with two bipolar opposite carriers is equivalent to the POD PWM method but with a double frequency.

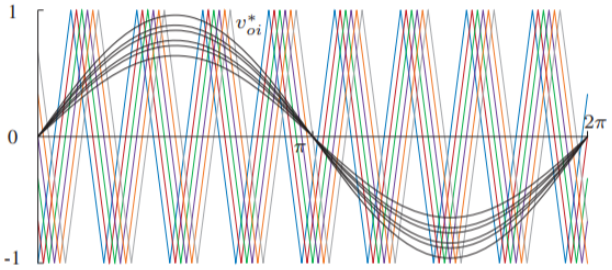


Fig. 5. PS PWM for the 7-level, cascaded H-bridge inverter and the generated output PWM signal.

The simulation results of PS PWM applied to the 13-level inverter are shown in Table 3.

Table 3. Output voltage and current THD versus the number of levels, modulation frequency is 50Hz, carrier frequency is 1050 Hz, PS PWM.

Modulation index	Inverter level	Phase current THD (%)	Phase voltage THD (%)	Line voltage THD (%)
1	13-level	1.23	9.2	5.5
0.83	11-level	1.1	11.1	7.1
0.67	9-level	0.95	15.2	8.22
0.5	7-level	0.93	16.3	11.12
0.333	5-level	0.8	24.5	15.34
0.167	3-level	0.9	49.3	37.2

4 Novel Asymmetrical PWM

The novel Asymmetrical PWM that is applied to 9-level cascaded NPC inverter and operates it as 13-level inverter. The asymmetrical 13-level PWM signal is obtained by summing two PWM signals: the 5-level hybrid PWM signal and 3-level pulsed PWM signal. The first 5-level hybrid PWM signal is constructed from combined parts of the standard 5-level PD PWM (see Fig. 6) according to the desired pattern as shown in Fig. 7 (PWM signal for 5-level bridge). The second 3-level pulsed PWM signal is constructed in coordination with the first 5-level hybrid PWM signal is such a manner that the sum of these two PWM signals will be the desired 13-level PWM. The desired 13-level PWM signal that is applied to the 9-level inverter is shown in Fig. 8. The frequency index should be a multiple of three.

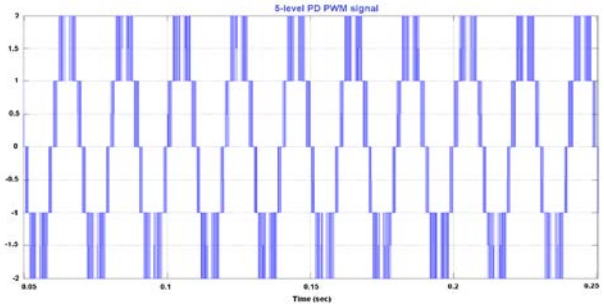


Fig. 6. The standard 5-level PD PWM signal.

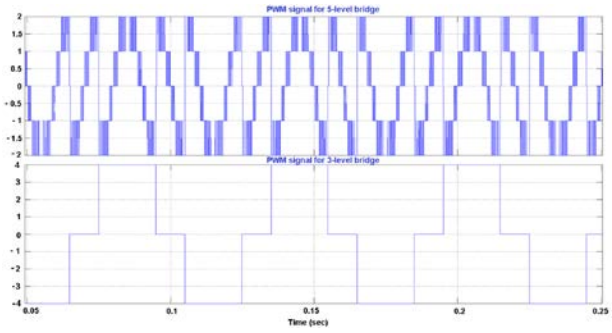


Fig. 7. The standard 5-level PD PWM signal.

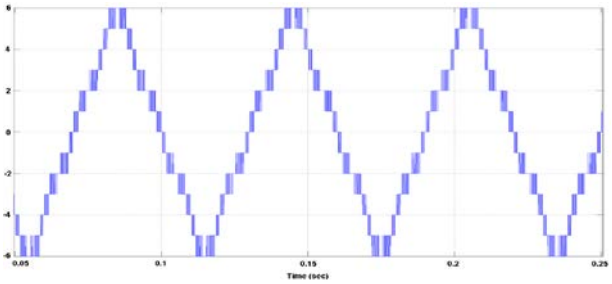


Fig. 8. The obtained 13-level PWM signal.

In order to verify the proposed PWM method, extensive simulations are performed. The simulation parameters are: DC=2000V, DC link capacitors C1=C2=10mF; the load of the inverter per phase are $R = 0.19\ \Omega$, L=0.24H. During the simulation of this 13-level PWM signal, the modulation frequency was set to 50Hz and the carrier frequency to 2100Hz. The obtained 13-level PWM signal is applied to the 9-level inverter presented in Fig. 9. If standard 13-level PD PWM was used, it would require additional cascaded bridge (see Fig. 4). This would result in additional costs and larger size and weight. The proposed PWM was also simulated for different modulation indexes. The simulation results are shown in Table 4.

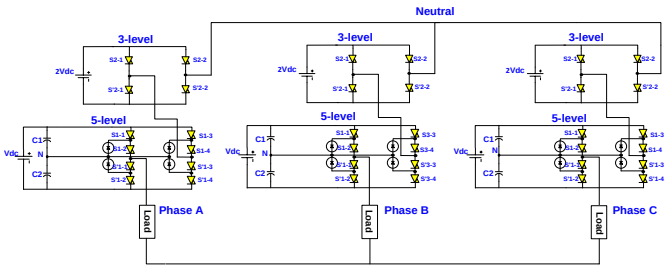
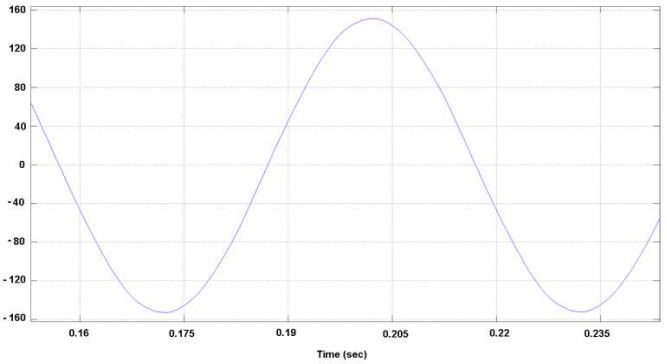
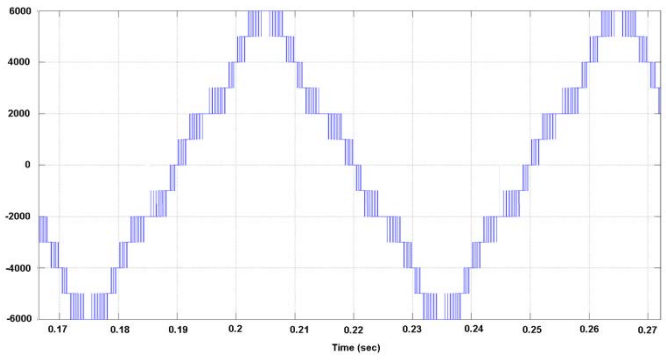


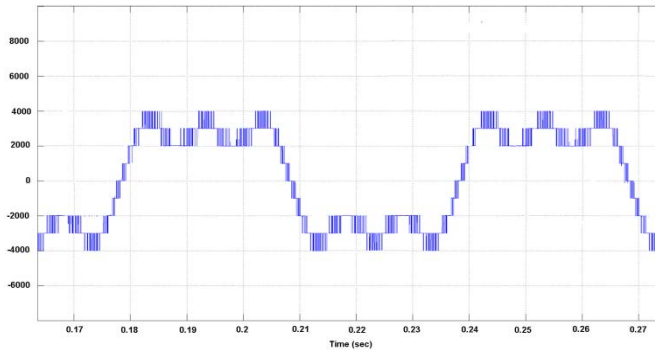
Fig. 9. The 9-level cascaded NPC inverter.



(a) Phase current, THD=0.9%



(b) Phase voltage, THD=16%



(c) Line voltage, THD=35%.

Table 4. Output voltage and current THD versus the level number. Modulation frequency 50Hz, carrier frequency 1050 Hz, Asymmetrical PWM

Modulation index	**Inverter levels (modulation index)**	**Phase current THD (%)**	**Phase voltage THD (%)**	**Line voltage THD (%)**
1	13-level (1)	0.9	16	35
0.83	11-level (1)	0.8	21	38
0.67	9-level (1)	1	27	44
0.5	7-level (1)	0.95	33	52
0.333	5-level (1)	0.8	47	61
0.167	3-level (1)	0.85	65	78

Table 4 shows that the decrease in the modulation index influences the number of the voltage levels in the output voltages, e.g., there are thirteen voltage levels in the phase voltage with modulation index 1, but only three voltage levels with modulation index 0.1.

It can be seen that the proposed PWM method provides good THD results of the currents and voltages. The phase current THDs are below 1% which is in full accordance with IEEE 519 standard. Therefore, the proposed method is practicable and it can be implemented also to other multilevel inverter topologies. This PWM method can be extended to higher number of levels.

Conclusions

The paper presents a review of standard and novel carrier-based PWM methods that are used for control of multilevel inverters. These PWM methods can be applied to different types of multilevel inverters. In this paper they were applied to the 13-level cascaded H-bridge NPC inverter (for PD, POD and APOD and PS PWM methods). The best results regarding the phase current THDs were obtained with the PD PWM method compared to the POD and APOD PWM methods. The PS PWM method is better suited for cascaded H-bridge inverters due to the parallel operation of all cascaded H-bridges.

The Asymmetrical PWM method was applied to the 9-level cascaded NPC inverter. The main advantage of this PWM method is that it allowed operation of the 9-level inverter as 13-level inverter. As a result, the number of components of the inverter was reduced compared to the standard topologies such as neutral point clamped or flying capacitor inverters. This results in smaller size, weight and cists of the inverter. However, the Asymmetrical PWM control is more complicated compared to the standard PWM methods such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and PS PWM. It can be seen that the Asymmetrical PWM method provides good THD results of the currents and voltages. The phase current THDs are below 1% which is in full accordance with IEEE 519 standard. Extensive simulation results validate the practicability of the Asymmetrical PWM method. The proposed method can be applied to any desired number of levels.

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