Parasitic Burden on the Performance of Coupled Inductor SEPIC Based Maximum Power Point Tracking in PV Systems

*NUR MOHAMMAD, MUHAMMAD QUAMRUZZAMAN, M. R. ALAM.

Department of Electrical & Electronic Engineering Chittagong University of Engineering & Technology, Chittagong-4349, Bangladesh *nureee_ruet@yahoo.com

Abstract: - This paper presents the effect of parasitic resistive burden in maximum power point tracking of photovoltaic (PV) systems using coupled inductor Single Ended Primary Inductance Converter (SEPIC). The energy storage elements incorporated in the coupled-SEPIC converter possess parasitic resistances. The particular effects of parasitics have been taken into concern for improving model accuracy, stability as well as the dynamic performance of the converter in MPPT applications. Detail model of coupled-SEPIC including inductive parasitic were developed. The performance of the converter in tracking MPP at different irradiance levels was analyzed for variation in parasitic resistance. The influence of converter as well as converter parameters on system behavior was investigated. It was found that the MPPT circuit reaches the maximum power point very fast followed by nearly free of start-up transient overshoot for reduced value of parasitic elements. For the similar load and at different weather conditions the MPPT efficiency was calculated. The maximum MPPT efficiency by using the coupled inductor SEPIC has been found 99.93%. The obtained simulation results validated the converter model in MPPT circuit.

Key-Words: - Photovoltaic (PV) energy systems, Parasitic burden, Maximum Power Point Tracking (MPPT), Single ended primary inductance converter (SEPIC), Magnetic coupling, Energy storage elements.

1 Introduction

Utilization of renewable energy resources is the most significant & prospective field to seek new energy sources to meet up the increasing power demand all over the world. Among the renewable resources, solar photovoltaic (PV) energy being the most accepted one due to its abundance, ease of accessibility and convertibility to the electricity. The output power versus voltage (P-V) curves of the PV array shows non-linear characteristic that depends on environmental conditions such as solar irradiance and temperature. The P-V curves (Fig. 1) udder different irradiance and temperature illustrate that, largest influence is the intensity of solar irradiation hitting the panel. The more solar radiation that comes into contact with the panel the higher the power, the less radiation the lower it becomes. As indicated, there is a unique point on the every P-V curve, where the maximum power is produced is called maximum power point (MPP). This is the point where the solar cell is most efficient in converting the solar energy into electrical energy. The MPP is not a fixed point, rather changes dynamically throughout the day depending on irradiance, G and temperature, T. Initiatively the derivative of power with respect to voltage of the PV source is zero at maximum power point.



Fig. 1 P-V Characteristics of solar PV module at different weather conditions.

As the maximum power points are not fixed as well as the observable voltage shifts where the MPP occurs. Therefore, the MPPs need to be tracked continuously in any weather conditions to maximize energy utilization of the PV source. The technique to extract maximum power by continuously adjusting the duty cycle of the DC/DC converter (which is placed between the PV source and load) with an appropriate algorithm is called maximum power point tracking (MPPT). The complete model of the standalone MPPT included PV system is presented in Fig. 2.



Fig. 2 PV system with maximum power point tracking circuit.

To track maximum power from PV array the different DC/DC converter topologies are frequently used, but most of the cases there is no clear criteria have been found for the suitable choice of converter. as well as properly tuning of the converter parameters. As a result maximum power point tracking performances degrades. For example, due to high input side current ripple of the some of the converter [1]-[4] used in MPPT circuit, the average value reduces and sensing this current leads to wrong decision for obtaining maximum power point. Moreover, the large ripple current may shorten the lifetimes of the low voltage PV sources [5]. Furthermore the large ripple current may create high voltage stresses of power semiconductor switches of the converter and electromagnetic interference (EMI) noises are significantly high [6]. The conversion efficiency is low due to higher conduction loss of the switches. Therefore, if the voltage stress is reduced by reducing input side current ripple, the efficiency of the MPPT could be improved. Due to the aforementioned problems frequently come with the conventional converter, the coupled inductor single ended primary inductance converter (SEPIC) has been proposed in MPPT circuit. Coupled inductor SEPIC provides the buck-boost conversion functionality without polarity reversal unlike the buck-boost and Cuk converter. The converter is capable of reducing the current ripple in the PV array side by properly coupling of the two inductors of the converter. It behaves as an automatic current shaper without any additional current control circuitry or input filter. The inductor used in the SEPIC has a certain amount of non-zero dc parasitic resistance, as it is usually a winding of several turns of long metallic wire. Similarly, the capacitor has also a small equivalent series resistance. But the parasitic resistance of capacitor may be neglected comparing to that of inductor [7]. Apart from adding ohmic losses, these parasitic resistances add current damping and affect the ripple attenuation [8]. Although considering ideal components significantly simplifies model development, but neglecting the parasitic in models may sometimes direct to failure in forecasting the fast-scale instabilities [9]. Therefore, it is important to take the effects of parasitics into consideration for exploring the dynamic performance, efficiency and robustness of the converter in MPPT. In case of SEPIC MPPT coupled inductor used for applications, a detail investigation is necessary to observe and analyze the effects of parasitics on the overall performance of the converter which is still not reported in the literature. In this paper, the effects of these parasitic resistances on the overall performance of these converters in MPPT are analyzed critically and the converter parameters are tuned to achieve quasi ripple free current in the PV side.

2 Maximum Power Point Tracking

After factoring in the attributes and deficiencies of several MPPT algorithms [10]-[13], the perturbation and observation (P&O) method is used in this work due to its fast tracking speed, less circuit complexity and its low computational demand. Flowchart of the method is presented in Fig. 3. The initial step in the algorithm is to sense the current and voltage presently being output by the PV array and use these values to calculate the power.



Fig. 3 Maximum power point tracking Technique

The algorithm then differences the existing power against the power from the previous iteration that has been stored in memory. The power difference is compared with zero, if it is found positive the algorithm will continue to perturb the voltage in the same direction. By contrary, if the power drops then the perturbation has moved the operating point away from the MPP. Hence, the method will reverse the direction of the next perturbation. The process is periodically repeated until the MPP is reached. In pulse width modulated (PWM) switching, the gate signals for MOSFET of the DC/DC converter are generated at a constant frequency of sawtooth wave modulated by the adjusted MPPT control signals. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width are shown in Fig. 4. The frequency of the repetitive waveform with a constant peak establishes the switching frequency. When the control signal, D which varies slowly with time relative to the switching frequency, is greater than the sawtooth waveform, the switch control signal becomes high, causing the switch to turn ON. Otherwise, the switch is OFF. In terms of $v_{control}$ and the peak of the sawtooth wave form V_{sw} , the switch duty ratio can be expressed as

$$D = \frac{t_{ON}}{T_s} = \frac{v_{control}}{\hat{V}_{st}} \tag{1}$$



Fig. 4 Pulse-width modulated waveforms.

The width of the gate pulses changes according to a MPPT control signal. When these PWM signal is applied to the gate of the MOSFET of the converter, it causes the turned ON and turns OFF intervals to change DC voltage level. The average DC output voltage must be controlled by adjusting the duty cycle of the converter so that the ratio of output voltage and current is same as the PV array at maximum power point.

2.1 MPPT Efficiency

Perturbation of the reference voltage to search maximum power oscillates the operating point around the MPP. The movement across the MPP is an unwanted oscillation that can be disrupting to exactly track maximum power. These oscillations reduce MPPT efficiency. MPPT efficiency is the ratio of the extracted power at standard test condition to the theoretical maximum power. The determination of dynamic MPPT performance is a challenging task as operating conditions can be changed in many ways. The behavior of the MPPT can be analyzed both in static and dynamic conditions; the static MPPT efficiency describes the ability of the MPPT to find and hold the MPP under constant environmental conditions (i.e. solar irradiance and cell-temperature) whereas the dynamic MPPT efficiency [14] describes the ability in tracking the MPPT in case of variable weather conditions. The MPPT efficiency is calculated as follows:

$$\eta_{MPPT}(t) = \frac{P_{in}(t)}{P_M(t)} \times 100\%$$
⁽²⁾

Where, $P_{in}(t)$ is the extracted maximum power from PV array $P_M(t)$ is the power at the MPP.

In case of discrete time calculations, the above variables are sampled, thus the MPPT efficiency at each sample is calculated as follows:

$$\eta_{MPPT}(k) = \frac{P_{in}(k)}{P_M(k)} \times 100\%$$
(3)

In static conditions, MPPT (t) is averaged over a specified period when the steady state is achieved and no further variations of $\eta_{MPPT}(t)$ occur; depending on the operating conditions, the transient can take several milliseconds. In dynamic conditions, when the MPP changes due to irradiance variations, the MPP tracking is usually analyzed using staircase or trapezoidal irradiance profiles [15] Knowing the values of $P_M(t)$ and $P_{in}(t)$ during the dynamic test, the efficiency can be calculated as follows [16]:

$$\eta_{MPPT} = \frac{\int_{0}^{T_o} P_{in}(\tau) d\tau}{\int_{0}^{T_o} P_M P(\tau) d\tau} \times 100\%$$
(4)

The oscillation around MPP can be minimized by decreasing the step size of the reference voltage However, a too small step size slows tracking the MPP considerably. To alleviate the aforementioned limitations it will be useful to use a small sampling rate which in turns speed up to reach maximum power point. So there has been made an optimization between accuracy and speed. In this research the switching frequency of the converter has been set to 25 kHz and the perturbation frequency of the reference voltage is one fifth of the switching frequency. As a result the sampling of the algorithm has been occurred in every .004 second.

3 Coupled inductor SEPIC

Circuit diagram of the coupled inductor SEPIC is presented in the Fig. 5, where the two separate inductors of the converter are physically placed on a common magnetic core. This reduces the component reckon, usually with slight or no penalty on the converter's character, rather enhancing its action.



Fig. 5 Coupling of inductors in coupled SEPIC is indicated by common core.

The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the inductance for a conventional SEPIC with two separate inductors. A first advantage of coupled inductors with respect to separate inductors is size and weight reduction [17]. An interesting characteristic of coupled inductors is that by proper design, unequal current ripple in the two windings can be obtained. Current ripple can be made even zero on one of the windings.



Fig. 6 Equivalent T model of coupled inductors.

To realize the input zero current ripple phenomena the equivalent transformer inserted T model of coupled inductor has been used. In order to investigate the zero ripple condition, accurate models of the leakage in series with the voltage sources and mutual inductances of the coupled inductor has been introduced. The problem has been made well-defined by including the parasitic resistance of inductors which are in series with the voltage. The equivalent circuit model using aforementioned considerations are expressed by following Eq.s (5) and (6).

$$v_1 = (L_{11} - M)\frac{di_1}{dt} + r_L i_1 + M\left(\frac{di_1}{dt} + \frac{di_2}{dt}\right)$$
(5)

$$v_1 = (L_{22} - M)\frac{di_2}{dt} + r_L i_2 + M\left(\frac{di_1}{dt} + \frac{di_2}{dt}\right)$$
(6)

3.1 Parasitics Burden on Conversion Ratio

The parasitic elements in a converter are due to the losses associated with the inductor, the capacitor, the switch, and the diode of the converter. The inductors used in the SEPIC have a certain amount of non-zero dc resistance, as it is usually a winding of several turns of long metallic wire. Similarly, the capacitor has also small equivalent series resistance (ESR). But the parasitic resistance of capacitor may be neglected comparing to that of inductor. The parasitic resistances of inductors become dominant at switching frequency than ESR of capacitors. Apart from adding ohmic losses, these parasitic add current damping and affect the ripple attenuation. Fig. 7 qualitatively shows the effect of parasitics (shown as dashed) against the duty ratio on the voltage conversion ratio of the converter. Sometime these parasitic elements have been ignored in the simplified analysis. However, these have been considered into the model of MPPT using SEPIC.



Fig. 7 Voltage conversion ratio is restricted by parasitic components.

If we consider that the converter operates in steadystate, the average current through the inductor is constant. The average voltage across the inductor including parasitic resistance r_L is:

$$V_L = L \frac{dI_L}{dt} + r_L I_L = r_L I_L \tag{7}$$

When the switch is in the ON-state, $V_Q = 0$ and when it is OFF, the diode is forward biased. Therefore, $V_Q = V_{in} + V_o$. So, the average voltage across the switch is:

$$V_O = (1 - D) \cdot \left(V_{in} + V_o \right) \tag{8}$$

The average inductor current [18], [19] in terms of average output current is:

$$I_L = \frac{D}{1 - D} I_o \tag{9}$$

Assuming the output current and voltage have negligible ripple. For the purely resistive load Eq. (9) becomes:

$$I_L = \frac{V_o D}{R \cdot (1 - D)} \tag{10}$$



Fig. 8 Normalized output voltage with the duty cycle variation for different parasitic resistances.

Using the previous Eq.s, the input voltage becomes:

$$V_{in} = r_L \frac{V_o D}{R \cdot (1 - D)} + (1 - D) \cdot (V_{in} + V_o)$$
(11)

$$\Rightarrow \frac{V_0}{V_{in}} = \frac{1}{\frac{r_L}{R} \frac{D}{(1-D)} + \frac{(1-D)}{D}}$$
(12)

Considering some practical value of parasitic resistance of the inductors, r_L Eq. (12) has been plotted. Normalized output voltages versus duty cycle are shown in Fig. 8. The figure illustrates that as the parasitic resistance increases the conversion ratio decreases and vice versa.

3.3. Converter Parameters Selection

Properly tuning the parameters of the converter is important. Let during the DT_s time, (*D* is the duty cycle and T_s is switching period of the PWM gate signals applied to the control switch) the switch is kept turned ON, the diode is turned OFF by the reverse voltage. The same input voltage imposed across both of the winding, as a result currents ramps up in the positive direction. In this time the load current is solely supplied from the output capacitor, C_2 . The pulsating current flowing through the control switch is the sum of the primary current (the average input current) plus the secondary current which flow through the coupling capacitor. The diode sees a reverse potential equal to $V_{in} + V_o$ during this period.

3.2. Duty Cycle Consideration

It is assume that the voltage drop V_D across the diode is usually 0.5V. The duty cycle D varies between 0 and 1. But too low or too large duty cycle is impracticable. Voltage conversion ratio is restricted by parasitic resistance of the energy storage elements of the converter. For the SEPIC converter operating in a continuous conduction mode, the value of duty cycle is given by

$$D = \frac{V_o + V_D}{V_{in} + V_o + V_D} \tag{13}$$

In case of minimum value of input voltage, the duty cycle would be maximum and vice versa. At first inductor L_1 has been selected. It is desired to have low ripple in i_{L1} to keep the solar panel operating at its MPP. At discharging phase of inductor, L_1 current ramp down at a slope of

$$\frac{di_{L1}}{dt} = \frac{-V_o}{L_1} \tag{14}$$

$$\Delta I_1 = \frac{V_o}{L_1} (1 - D)T \tag{15}$$

$$\frac{V_o(1-D)}{L_1 f} \tag{16}$$

One of the first steps in designing any PWM switching regulator is to decide how much inductor ripple current, ΔI_L , to allow. Too much, increases EMI, while too little may result in unstable PWM operation. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage [20]. The ripple current flowing in equal value inductors L_1 and L_2 is given by:

$$\Delta I_L = I_1 \times 40\% = I_o \times \frac{V_o}{V_{in}} \times 40\% \tag{17}$$

When the switch is turned ON, the value of the first inductor L_i is derived from the following fundamental relation of

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} \tag{18}$$

$$\Rightarrow L_1 = \frac{V_{in}}{\Delta i L_1 \cdot f} D \tag{19}$$

Similarly when the switch is turned OFF, the value of the inductor L_2 is derived from the following relation of

$$\frac{di_{L2}}{dt} = \frac{-V_o}{L_2} \tag{20}$$

$$\Rightarrow L_2 = \frac{-DV_{in}}{(1-D)} \frac{1}{\Delta i L_2} (1-D)T$$
(21)

$$\Rightarrow L_2 = \frac{-V_{in}}{\Delta i L_2 \cdot f} D \tag{22}$$

Ignoring the sign from the above equations and considering the magnitude of current ripple $\Delta I_{L1} = \Delta I_{L1}$, it can be said that, $L_1 = L_2$. That is, both the inductors have to have same level of inductance. It proves that they have induced same level of voltage with opposite polarity. Physically the windings are constructed with the same number of turns on the similar ferrite iron core. If L_1 and L_2 are wound on the same core, the value of inductance in the Eq. (22) is replaced by 2L due to mutual inductance. The coupled inductor value is calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{in}}{2 \times \Delta i L \times f_s} D \tag{23}$$

The MOSFET switch was selected with the minimum threshold voltage, the on-resistance, gatedrain charge, and the maximum drain to source voltage. MOSFETs should be used based on the gate drive voltage. The peak switch voltage is equal to $V_{in} + V_o$. The peak switch current is the sum of input and output current. The output diode was selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The minimum peak reverse voltage the diode must withstand is same as that of the MOSFET switch. The average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes were used in order to minimize the associated loss. The selection of coupling capacitor, C_1 , depends on the RMS current, which is given by:

$$I_{C_1(rms)} = I_o \times \sqrt{\frac{V_o + V_D}{V_{in}}}$$
(24)

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small. The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Ceramic capacitors are the best option due to having high RMS current ratings comparative to size. In a coupled inductor SEPIC converter, when the power switch Q is turned ON, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor sees large ripple currents. Thus the selected output capacitor must be capable of handling the maximum RMS current. In MPPT included PV system trapezoidal type solar irradiance model was considered to test the MPPT performances.

Table 1 Specification of PV array [21] and optimized converter parameters.

Parameters	Specification
Maximum power (P _m)	100 W
Open circuit voltage (Voc)	21.5 V
Short circuit current (I _{sc})	6.22 A
Voltage at maximum power (V _m)	17.30 V
Current at maximum power (I _m)	5.8 A
Short-circuit current temp	6.928 mA/ °C
Open-circuit voltage temp	-0.068 V/ °C
Module size	36 Cells
Inductor L ₁₁	0.1500mH
Inductor L ₂₂	0.1490 mH
Mutual Inductor M	0.1479 µH
Inductor parasitic resistance r_L	1.00Ω
Capacitor C ₁	47 µF
Capacitor C ₂	47 µF

4. **Results and Discussion**

The complete model of the PV system including MPPT algorithm using coupled SEPIC converter has been developed in Matlab/Simulink [22]. It presents unique capabilities for developing control algorithms, modeling power electronics and power systems. At first, the effectiveness of maximum power point tracking is illustrated in Fig. 9. From this figure it is clear that without MPPT circuit, usable power is largely reduced. For instance, the extracting power at 900 W/m² was found 90.06W, whereas it is reduced to only 50.09W only at same irradiance level without MPPT circuit. On an average about 45% power could be saved by using if MPPT is availed. It can be roughly said that, purchase of two solar PV panel is equivalent to purchase of only one solar panel, with an MPP tracker.



Fig. 9 MPPT performance improvement.

Maximum power point tracking operation can be better explained with reference to the array P-V curve of Fig. 10. Let the PV system was started at 1000 W/m^2 solar irradiance and 25°C temperature. For these weather conditions the possible maximum power from the PV array is 100.3W. The voltage at maximum power is 17.3V. The perturbation frequency of the MPPT algorithm is of 3.33 kHz and a step size of voltage is 0.4V.



Fig. 10 Maximum power point searching.

After nearly diminishing the start-up transient period the PV array power was measured at about 99 W with the system operating at the initial reference voltage (16.5 V) represented by point A. It is noteworthy that when it is said, the voltage level has been increases; it means the duty ratio of the converter has been rises by using P&O MPPT algorithm. When the algorithm reverses the perturbation direction by decreasing the duty ratio, then the voltage level also decreases. Fig. 10 illustrates that; the initial perturbation direction should be in positive direction, to increase the reference voltage. The reference voltage is increased by 0.4V (the step size) to 16.90 V moving the operating point to point B, where the available power is about 99.80W. Array power is measured after a perturbation period of 1.5 msec has passed. Now available power is 100.3, the maximum power for this irradiance. The voltage for this maximum power is 17.3V. As the power increases in previous step, hence algorithm continues to increase voltage level by perturbing in the same direction. Now the voltage level rises to 17.7V, power point is indicated by the point C. However after measurement, it was found 100.10W. As power decreases, the P&O algorithm reverses the perturbation direction to decrease the reference voltage, again back optimum power point, O. Due to the power increases, the algorithm continues to decrease the reference voltage to 16.9 V (point B) passing through the maximum power point (100.3 W at point O) located at 17.3 V. Because the power at point B is lower than that of at O, the P&O algorithm reverses the

direction of perturbation to increase the reference voltage to reach MPP. After next perturbation in the same direction, when power level will be decreases, the perturbation will be in the negative direction. The sequence is repeated until there is a change in solar irradiance and cell temperature. The fluctuation or oscillation of power around the maximum power point is only around 0.1% which sufficiently in acceptable limit. For any other irradiance level, the algorithm adjusts the duty cycle in similar manner as described before to deliver the corresponding maximum power. In similar fashion, for two different irradiance, the maximum power tracking is illustrated in Fig. 11. and Fig. 12.



Fig. 11 Maximum power point searching for two different irradiance.

A coupled inductor structure designed for zero ripple can have some residual current ripple due to the fact that the turns ratio used is not exactly equal to the one required for ideal zero ripple. But even if the exact turns ratio is used, the coupled-inductor structure will have some residual ripple when used in a switching converter due to the fact that the voltages applied by the converter to the two windings will not be exactly equal due to presence



Fig. 12 Maximum power points in P-V curves for two different irradiance.

of parasitic elements in the energy storage elements of the converter. Fig. 13 and 14 shows tracking performances for trapezoidal irradiance profile. From Fig. 13, it is seen that there is an observable deviation of tracking maximum power point due to consideration of inductive parasitic elements. But Fig. 14 best depicted the maximum power point with the similar input and output condition excluding parasitic components. Fig. 15 illustrates the maximum power for different irradiance level with time. The topmost curve indicates the extracted power at zero level parasitic. This is the maximum power. The subsequent curves illustrates that the available power from the PV sources reduces as the parasitic of the energy storage elements increases. It is also attributed that the power curves are being gradually affected by the ripple contents due to addition of resistive burden of the converter.











Fig. 15 Available power reduces as the parasitic of the energy storage elements increases.

5 Conclusion

Maximum power point tracking using coupled inductor SEPIC was presented in this paper. It was found that the converter is capable of reducing the current ripple in the PV array side by coupling two inductors of the converter. The converter with optimized coupling coefficient gives the steady operation of the converter in MPPT scheme with maximum system efficiency 99.44%, irrespective of weather conditions. The parasitic resistive burdens on the performance of MPPT using coupled inductor SEPIC have been analyzed. As the parasitic increases, quadric behavior of MPPT is observable. Oscillation arises due mismatch of induced voltage across the inductors of the converter. The possible voltage gain drops off sharply from the theoretical value, especially as the optimum duty cycle of around 93%. A fraction of the power managed by the converter was dissipated by these parasitic resistances. So Inductors with lower series resistance allow less energy to be dissipated as heat, resulting in greater efficiency and a larger portion of the input power being transferred to the load.

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