Design and performance analysis of 4-bit Nano-Processor design for low area, low power and minimum delay using 32nm FinFET technology

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Abstract: - The recent technologies in VLSI Chips have grown in terms of scaling of transistor and device parameters but still, there is challenging task for controlling current between the source and drain terminals. For effective control of device current, the FinFET transistors have come into VLSI chip, through which current can be controlled effectively. This paper is to address the issues present in CMOS technology and majorly concentrated on the proposed 4-bit Nano processor using FinFET 32nm technology by using the Cadence Virtuoso software tool. In the proposed Nano processor, the first part is to design using 4bit ALU which includes all basic and universal gates, efficient and high-speed adder, multiplier, and multiplexer. The Carry Save Adder (CSA) and multiplier are the major subcomponents which can optimize the power consumption and area reduction. The second part of the proposed Nano processor is 4-bit 6T SRAM and Encoder and decoder and also Artificial Neural Network (ANN). All these subcomponents are designed at analog transistors (Schematic level) through which the Graphic Data System (GDS-II) is generated through mask layout design. Finally, the verification and validation are done using DRC and LVS, at the last chip-level circuit is generated for chip fabrication. The ALU is designed by using CMOS inverters and the designed ALU schematic is simulated through 32nm FinFET technological library and compared with CMOS technology which is simulated through 32nm CMOS library (without FinFET). The power consumption of AND, OR, XOR, NOT, NAND gates, SRAM, Encoder, Decoder and ANN are 36.09nW, 64.970nW, 61.13nW, 33.31nW, 37.45nW, 32.5% optimization in power dissipation and 47% optimization in leakage current, 2.68uW, 1.98uW and 7.5% improvement in power consumption and 0.5% information loses compressed subsequently respectively. The basic gates and universal gates, CSA, subtraction, and MUX are integrated for 4-bit ALU design, and its delay, power consumption, and area are 0.104nsec, 314.4uW, and 56.8usqm respectively.

Key-Words: - FinFET Technology, CMOS, Gated Techniques, ANN, CSA, Nano Processors.

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1 Introduction

Rather than the dynamic force, static force from a transistor is devoured because of a little consistent release instrument, also called spillage. There are a few methods of spillage, however they can be extensively named sub-edge, entryway, and converse one-sided channel and-source substrate intersection band-to-band-burrowing (BTBT) [1, 2]. These spillage instruments have solid reliance with a few second request gadget parameters (e.g., oxide thickness, doping fixation, temperature), notwithstanding the flexibly and edge voltage of these gadgets. On account of these subsequent request impacts, it is all the more testing to precisely evaluate transistor level patterns in static force, and

its general commitment to the TDP. In any case, the general static force because of spillage has been consistently becoming in the course of the last a few innovation ages [3]. Sub-limit spillage, which has an exponential reliance with the edge voltage, expanded quickly with the scaling of edge voltage, and commonly overwhelmed the spillage flows [4]. All the more as of late, limit voltage has nearly quit scaling to counter this sub-limit spillage, yet the scaling of other gadget parameters (e.g., oxide thickness) caused an ascent in door spillage and BTBT. In this manner, both these two spillage instruments presently establish a considerable

division of the all-out spillage [1]. Regardless of this consistent ascent, a few methods have indicated huge potential in moderating the spillage (e.g., high-_ metal oxides, twofold door gadgets). Inside an innovation age, circuit planners pick the ideal methods for controlling the spillage vitality, dictated by the advancement of the general force execution of the framework [5]. The impact of door channel/source underlaps on a thin band LNA execution has been contemplated, in 30 nm FinFET utilizing the gadget and blended mode recreations. Studies are finished by keeping up and not keeping up the spillage current (I_{off}) and edge voltage (V_{th}) of the different gadgets. LNA circuit with two transistors in a course game plan is developed and the information impedance, increase, and commotion figure have been utilized as execution measurements. To show signs of improvement commotion execution and addition, Lun in the scope of 3-5nm is suggested [13].

The structure of a chip must conjoin two key innovation patterns: drifts in semiconductor industry that underlies the fundamental structure square of microchips, and patterns in programming that sudden spikes in demand for these microchips, directing their practical necessities. Behind a significant number of these innovation drifts, the market financial matters assumes a basic job and profoundly impacts their Evolution, including the state of microchips. The most significant pattern in the semiconductor innovation is the scaling of transistor gadgets, permitting to twofold the quantity of accessible transistors on a chip like clockwork [6]. Notwithstanding this exponential development in gadgets, the scaling additionally accompanies an improvement in the exhibition of every gadget, empowering all the more remarkable chip in progressive ages. Surely, no other industry in the history has seen the wonderful development that the chip business has shown in the previous a very long while [7]. This enormous improvement from the equipment incredibly affected the product, drastically expanding its decent variety and multifaceted nature in the interest to misuse the presentation help from the equipment, and improve the end-client fulfilment. While looking for execution improvement was the most prevailing necessity from a financial outlook before, more as of late, the market financial matters is progressively requesting vitality proficiency, while disallowing the ascent of multifaceted nature and related structure costs, significantly changing the plan contemplations of chip. Thus, the customary technique of abusing more transistor assets to construct progressively intricate, and power hungry solid processor centres, is offering route to the pattern of measured plans dependent on multicores where a solitary handling centre is reproduced on different occasions on a similar bite the dust. The development of multicore chips delivers numerous new difficulties and openings. Misusing the simultaneousness, and the calculation data transmission managed by these multicores is a significant plan challenge for the future frameworks, enveloping different layers of framework creators from the equipment modules to the application engineers [9]. Then again, the predominant correspondence transmission capacity and inactivity between on-chip centres motivate novel procedures to deal with the total centre assets, in order to fulfil the interest for execution and vitality proficiency. A large number of these strategies may have been altogether infeasible in multiprocessors worked from uniprocessor chips, and subsequently neglected to legitimize genuine contemplations previously. One more test rotates around guaranteeing solid execution, particularly when the characteristic unwavering quality from the equipment segments is required to fall with the innovation scaling [10, 11]. All these wide issue areas are significant and need considerable research, yet this work around the subsequent issue: abusing more assets to improve vitality productivity and execution, without putting extra weight on the force financial plan. A few current age multiprocessor chips are as of now working close to the building limit for power, in light of air cooling [12, 13]. With the exponential development of transistor gadgets, the capacity to put all the more handling centres on a chip is currently ready to effectively outpace the relating capacity to control up these centres at the same time.

The FinFET based microprocessor designs are fringe of two most fundamental trends in the latest technologies such as demand of semiconductor technology which is a group of basic building blocks such as ALU, registers, buffers, encoder and decoders, and software trends that simulates or compiles the microprocessors. Behind a considerable lot of these innovation patterns, the demand for semiconductors plays a basic job and profoundly impacts their development, including the state of microchips. The most significant pattern in semiconductor innovation is the scaling of transistors, permitting multiplying the quantity of accessible transistors on a chip for every ear. Notwithstanding this exponential development in

devices, the scaling likewise accompanies an improvement in the presentation of every transistor device, empowering all the more dominant microchips in progressive ages. For sure, no other industry in history has seen the wonderful development that the microchip business has exhibited in the previous a very long while. This huge improvement from the equipment incredibly affected the product, significantly expanding its assorted variety and multifaceted nature in the interest to abuse the presentation support from the equipment, and improve end-client fulfilment. FinFET has double Gate so it has better control of channel from transistor gates, reduced short channel effects, Better Ion/Ioff and improves the sub-threshold slopes. The power consumption in both dynamic mode and static mode are less as compared to traditional CMOS circuits. IC's designs are the most important domains, due to its low cost, low area and high speed process. For two decades, low force/vitality configuration has been a significant structure limitation. The blast in advanced interchanges and the craving to save battery lifetime, improve framework unwavering quality, and decrease cooling costs has pushed for broad research in low force/vitality computerized structure. In this paper low, vitality versus low force will be talked about. At that point the nuts and bolts of low force configuration patterns, significant methods, and ongoing difficulties will be exhibited and examined [14]. The static commotion edge of FinFET static random access memory (SRAM) cells working in the sub threshold district was explored utilizing an explanatory arrangement of 3-D Poisson's condition. A diagnostic SNM model for sub threshold FinFET SRAM was shown and approved by 3-D innovation PC helped structure blended mode re-enactments. When contrasted and mass SRAM, the standard 6T FinFET cell indicated bigger ostensible READ SNM (RSNM), better fluctuation insusceptibility, and lesser temperature affectability of cell dependability [15]. Since Moore's law-driven scaling of planar MOSFETs faces imposing difficulties in the nanometre system, FinFETs and Trigate FETs have risen as their replacements. Attributable to the nearness of numerous (two/three) entryways, FinFETs/Trigate FETs can tackle short-channel impacts (SCEs) better than traditional planar MOSFETs at profoundly scaled innovation hubs and in this manner empower proceeded with transistor scaling. In this paper, we audit inquire about on FinFETs from the bottommost gadget level to the highest design level. We review various kinds of FinFETs, different conceivable FinFET asymmetries and their effect, and novel rationale level and design level trade-offs offered by FinFETs. We likewise survey the investigation and enhancement apparatuses that are accessible for portraying FinFET gadgets, circuits, and models [16].

2 Problem Formulation

In existing research work pertaining to IC designs and fabrications in FinFET based analog circuits are suffering in terms of optimizations of power, area, leakage current, delay and reducing of transistors sizes (L/W ratio). The second challenging task in the existing work is that the controlling of current between source and drain terminals and it is not effective for high speed VLSI chips and for complex operations. The solutions of these two challenging tasks is the proposed 4-bit nano processor design using FinFET 32 nm technology in Cadence Virtuoso tool.

3 Proposed design of 4bit Nano processor

3.1 Analysis of power, area and delay optimizations for 4-bit Nano processor

This research work mainly concentrates on the optimization of area, power and delay, the area is mainly depending on the number transistors integrated to design a FinFET based processor using FinFET transistors and it can be expressed as $Area_{die} = \sum_{j=1}^{M} Size_j$, where $Area_{die}$ represents the silicon die area, M is the total number transistors are integrated on single processor, $Size_j$ is the size of the each and every transistor. The total area of the FinFET based processor is designed by considering the various factors like total area die expected, wafer size and cost after fabrication for the market place. Afterward the total area limitation or finalization of area for die, it should then be met by the total sizes of incorporated sizes of each transistors. As the condition shows, one can either decrease the size of every transistor or essentially expel the necessary number of devices to fulfill this requirement. After the minimum size of the device is obtained using FinFET technology, rectifications of the violation for the area constraints are possible and can be scale down the transistors count. In this work, the area optimization is done by using "**fingering**" concept. Fingering is to upgrade the resistance of the gate poly terminal along the width of the transistor. Since the gate poly is driven from one end and entryway poly is resistive, there might be motivation to have a rule that expresses the most

extreme width of a solitary finger. But the fingering requires more number of transistors but fingering concept is the most optimization techniques to optimize the area, not only area optimization, the active capacitance can also minimized because the drain region is bounded with gate poly instead of the electric field.

3.2 Technique to optimize the area by using Fingering Concept:

- Keep the transistor of fixed size so that the height remains constant but then put more number of transistors in parallel so as to deliver more current to the load.
- In this case join the sources and drains in chained fashion so that they act like taps in parallel. In general when say 2x and 4x drive strength buffers what exactly it means is that it could deliver 8 times more current than the normal 1x buffer by employing 8 fingers or even more.
- Another advantage of fingering is that resistance reduces drastically by fingering. Let us say you have a resistance of R from the given figure. Now when fingering is done, all these resistances come in parallel hence, the resistance reduces by a factor of N. This is another remarkable advantage of doing fingering.

The second most parameter is power consumption or dissipation of the proposed processor chip is measured as similar case of area discussed above. This power is mainly depending on the cost-effective capacity cooling of more number of transistors i.e more volume processor designs. In the recent research work, the energy in term of efficiency is optimizing in different ways on the silicon chip budget. The power measurement in general is $P_{dissipation_{die}}=\sum_{j=1}^{M} Power_j$, $P_{dissipation_{die}}$ is the power constraint on the chip design level, $Power_j$ is the power dissipated by the complete processor and M is the total number transistors used for the designing of the FinFET based processor. In this research work, the 4-bit Nano-Processor is designed, the one of the constraint of this processor is analytic model is that optimization of the power which is sum of the dynamic and static power. The dynamic power is mainly due to switching activity of the transistor which is due to charging and discharging of the capacitor load at the output of the each and every transistor and it can be expressed as $power_{dy} = C_l.V_{dd}^2.F_{signal}$. The static power is because of spillage has been consistently becoming in the course of the last a few innovation ages. Sub-edge spillage, which has an exponential reliance with the limit voltage, expanded quickly with the scaling of edge voltage, and commonly ruled the spillage flows. All the more as of late, limit voltage has nearly quit scaling to counter this sub-edge spillage; however the scaling of other gadget parameters (e.g., oxide thickness) caused an ascent in entryway spillage.

The quest for vitality productivity and better in progressive chip structures have constrained the architects to successfully arrangement more useful segments than those that are carefully vital for right execution. By definition, this technique prompts a decreased asset usage, with the degree of over-provisioning being contrarily relative to the use. In any case, there are a few instances of over-provisioning in the smaller scale design segments of current usage (e.g., the physical register document and guidance window passages). A FinFET based Nano-Multicore System (FinFET-NMS) is a class of multicores that by configuration arrangements more handling centre assets than that can be kept dynamic for its objective Thermal Design Power (TDP). The key differentiation between an ordinary multicore and a FinFET-NMS originates from the characteristic objectives in their framework structures, separately. Authoritative multicore considers a preparing centre as one of the most basic segments of the framework, and thus targets full use of its centre assets. As per the present innovation patterns, where the capacity to coordinate preparing centres on a solitary kick the bucket is outpacing the ability to control them up at the same time, a FinFET-NMS considers power and warm attributes more basic than the handling centres. Thusly, it arrangements more centre assets to offer a decision in allocating calculation on them, and improve framework attributes (e.g., vitality effectiveness, warm profile) by means of wise calculation task approaches. In this proposed wok, the design consists of transistor with two controlling gates is investigated as a circuit component utilized for the execution of various combinational basic components like gate, ALU, Multiplexers, Multipliers, CSA and encoder and decoders systems and utilizing these elements, the 4-bit Nano-Processor has been designed which depends on FinFET technology is designed from Schematic level to layout through GDS-II level. The verification is done through physical design to

validate the power, delay and area. With separately gates connected, series/parallel exhibits could be performed utilizing a solitary device, however with an immediate effect in the electrical presentation of gates used in processor. In this work, it is demonstrated the electrical investigation as far as signals delays passing and energy utilization of compacted transistor systems. Various topologies got from the different gates activity were tried through electrical re-enactments and the outcomes exhibit the current exchange off between these two parameters. Additionally, a diagnostic defer articulation was inferred for logic systems which use IG FinFETs, determining scientific articulations for the effect of diminishing varieties of arrangement transistors in logic gates. The investigative model for IG FINFET devices was tried in a coherent information way and contrasted with SPICE reproduction results, demonstrating its utility for the planning examination of computerized circuits. The major concerns of this chapter is to integrate the different designs discussed in the chapters 3, 4,5 and 6 using FinFET transistors. In the chapter 3 discussed about design of the ALU which includes all basic gates and athematic operation like multiplier, Carry Save Adder (CSA), MUX, 4-bit SRAM, Gilbert multiplier and buffers, through which the performance effects on the Nano-Processor is analysed as shown in Fig.1. The complete processor design could achieved the following

- The increase the source to drain current, the simulation of electrical environment has been set-up and it is capable of controlling the nature of FInFET devices and gate controlling or coupling capacity.
- All transient of electrical signals of different modules (discussed in the previous chapters) has been build using FinFET transistors and measured their performance metrics like delay and power dissipation.
- In order to Measure the different equations of delay and transitions of the different modules which are based on FinFET logic structures are designed and compared with the existing work.

The FinFET device is a symmetrical transistor having same gate function as CMOS gate function i.e $G_1=G_2=G_{FinFET}$ and their oxide thicknesses are same i.e $t_{ox1} = t_{ox2} = t_{FinFET\_ox}$. The gate and thickness oxides functions, the control of the current flowing between source and drain is very easy and can obtain the maximum current gain and voltage gain. In this research, the first part of design is 4 bit ALU using FINFET Technology. The CMOS Technology is dominant and widely used Technology for fabrication of VLSI chips but the major issues are scaling of short channel effects like DIBL, sub thresholding and GIDL, degradation of mobility and modulation of channel length. To address these issues with CMOS, the proposed design has been changed to mitigate technology formally called FINFET Technology.

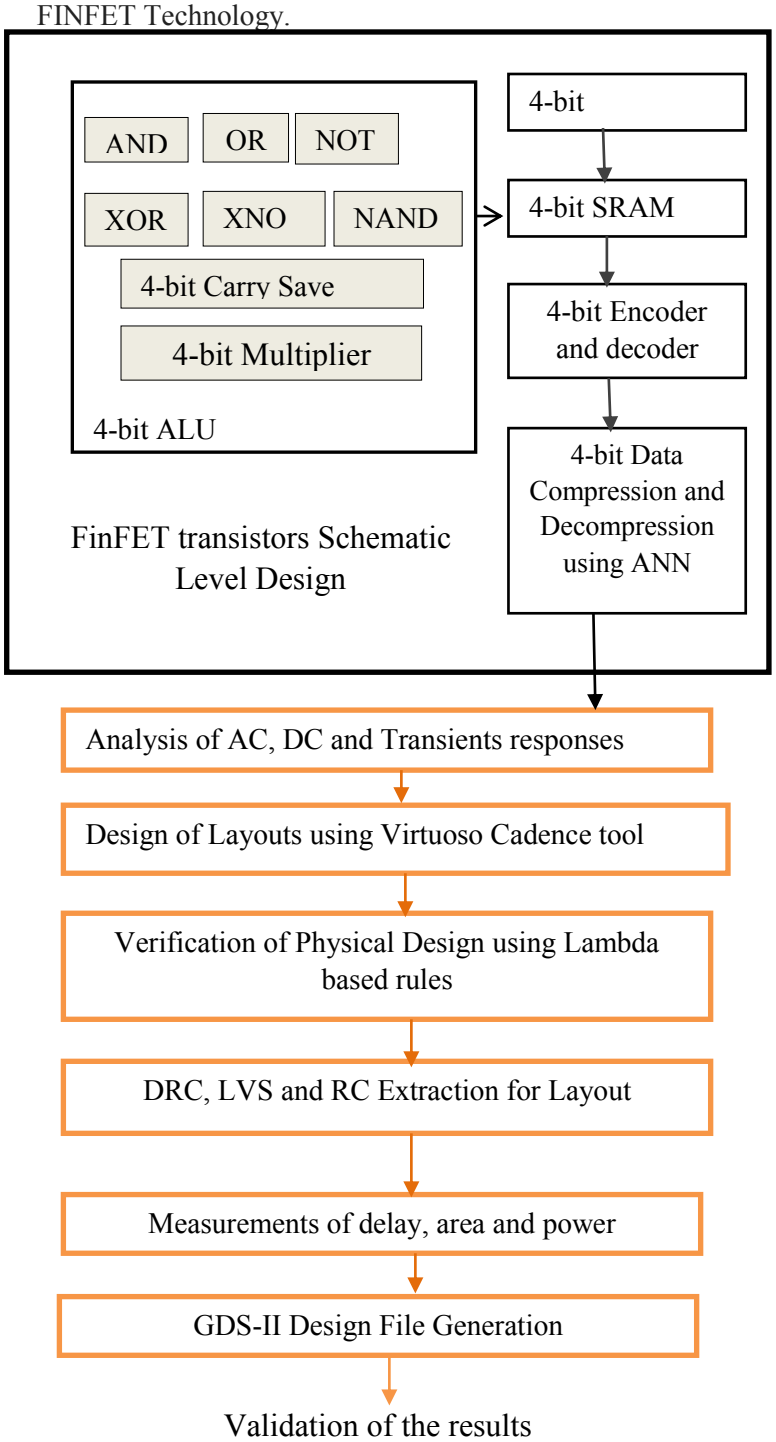

Fig.1. Proposed 4-bit Nano-Processor design using 32nm FinFET technology

The main advantage of it are controlling of current since it has two Gates, reduction of leakage current, reduction in delay of each transistor, minimum VT

and also FINFET transistors operates at a low power. The main concentration of 4 bit ALU design is to optimize the power delay, area, V_T and leakage currents.

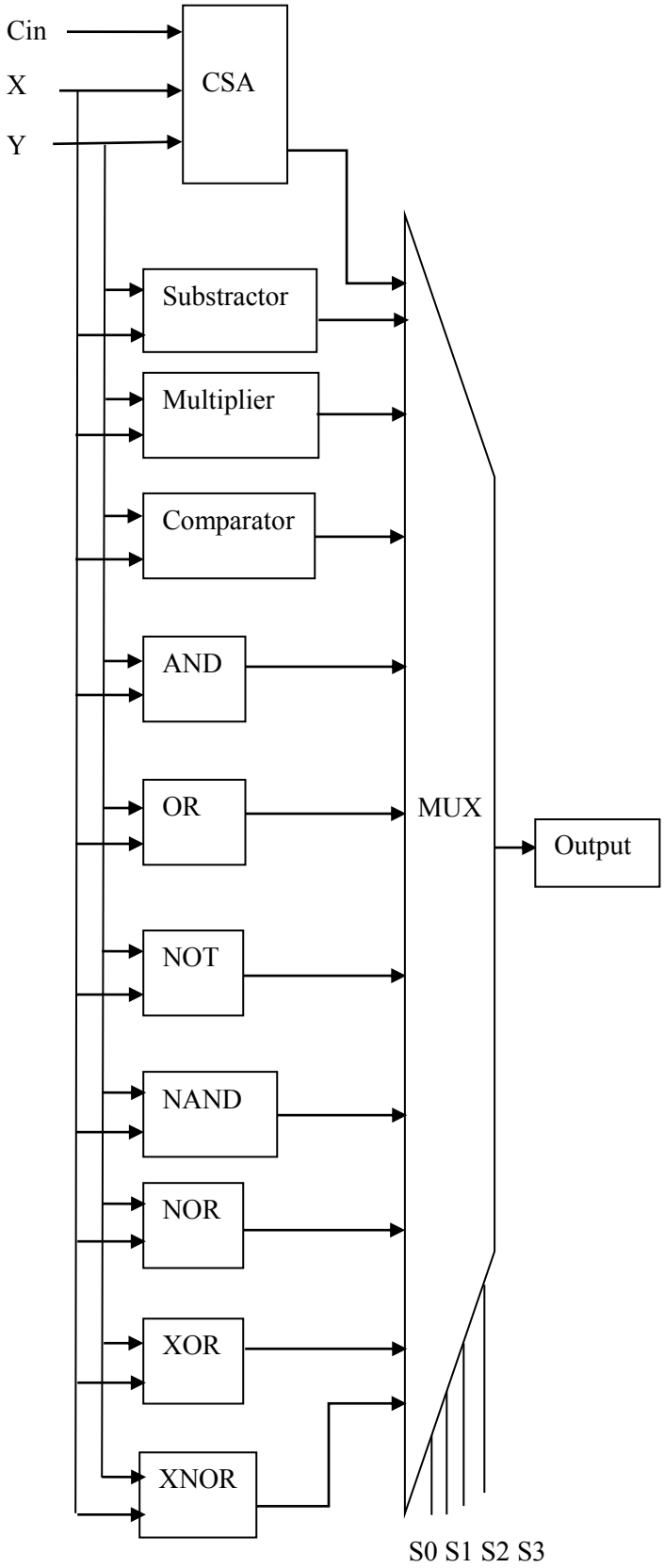

Fig.2: Architecture of 4bit ALU with 11 Input MUX

The ALU consists of complex multiplier, comparator, carry save adder (CSA), subtraction, are the Arithmetic operation and the seven logical Gates are designed by 32 by using 32nm FINFET Technology for 4 bit has shown in Fig.2 and The simulated results of 4 bit ALU is discussed in chapter 3. The design 4 bit ALU and its basic building block are used in the Nano processor. The 11 input multiplexer is designed to select one of the ALU outputs as MUX output as shown in Fig.2.

4. Results and Discussion

To meet power requirements, proposed Nano-processor must consolidate novel strategies for leakage current (LC) decrease, power decrease (PD), area optimization (AO) procedures and research how a decrease of LC, PR and AO impacts their significant level useful structures from the get-go in the plan stage. This work showed two explicit employments of LC, PR and AO contemplations utilizing scientific models in Nano-Processor plan. In the first place, this work broadened the past work talked about in presentation, and joined LC, PR and AO for unequivocally displaying power limitations in different Nano-Processors structures. Strangely, this work found that with the expanding power imperative, demonstrated utilizing various degrees of LC, PR and AO, the uneven multicore moved toward the exhibition of the dynamic multicore. All structures of 4-bit Nano-processor cells of CMOS and FinFET were verified, validated and analyzed in term of simulation waveforms in Cadence Virtuoso tool to investigations its metric exhibitions, like, different delays, normalized power consumption/dissipation, power-delay-product (PDP), and energy and delay product (EDP). In light of the discoveries, the 4-bit FinFET-based Nano-processor is demonstrated to be the most minimal and ideal tradeoff in every single metric execution contrasted with the CMOS-based existing processor. This demonstrated, by utilizing FinFET innovation in 4-bit processor chip level circuitry, it will improved in terms of power, area and delay. In any case, the cell configuration likewise adds to how great the nano-processor performs, as examined prior. The 4-piece FinFET-based nano-processor has a decreased propagation delay and normal energy dissipation, PDP, and EDP, along these lines giving FinFET innovation incredible points of interest in vitality effectiveness and exhibitions for 32 nm innovation. It was likewise confirmed that the 4-bit

conventional pass-transistor logic (CPL) FinFET based nano processor performed very well with a decreased measure of PDP and EDP contrasted with other cell plans on account of its fast execution and full swing activity. The complete Nano-processor design which includes ALU, Multiplexer, encoder, decoder and ANN schematic in terms of analog transistors are shown in Fig.3. The results are validated through simulation of each and every sub components as shown in Fig.4. The Fig.5 is ANN design, its includes both compression and decompression and their input and output ports.

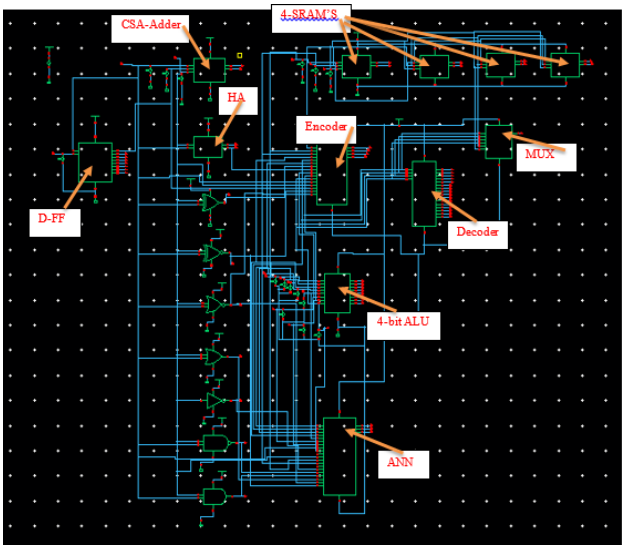

Fig.4. Overall proposed Nano-Processor design using FinFET 32nm technology and subcomponents

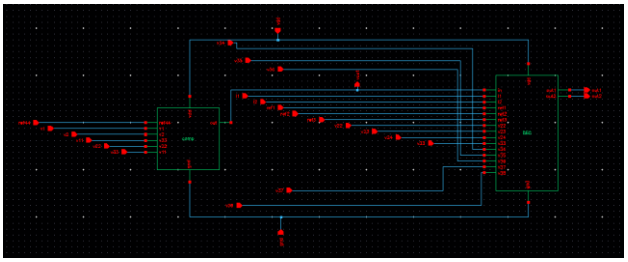

Fig.5. Top level schematic circuit of ANN

5 Conclusion

In this paper, the dual gate transistor is presented to design the all basic operations, ALU, multipliers and using these basic elements, the 4-bit Nano-Processor is designed. This processor design, shown the interested feature of FinFET devices for controlling of the current flowing between source and drain and controlling of the transistor operations to obtain maximum gain, low power, low delay and low area. Through dual gate operation, it is observed that, the threshold voltage (V_t) is minimum as compared the case in the CMOS technology. The complex multipliers and other complex logical functions are simulated using Virtuoso back-end Cadence tool, it include the 32nm FinFET technology. The simulated results using different topologies have shown that reduction in the number of transistors, low area and optimized power. Lastly, delay and power simulations of the designed Nano-Processor were performed to prove that 32nm FinFET transistors would be helpful to minimize the leakage currents and area optimization using Fingering concepts. From the obtained results, it is observed that, there is reduction power of about 48%, reduction in delay is about 51% and 29% of power reduction as compared to existing works.

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