A 1GHz low-cost, ultra low-noise preamplifier

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Abstract: - A high quality, compact 1GHz preamplifier suitable for operation in conjunction with micro channel plates (MCP) and silicon Photomultipliers (SiPM), that is comprised of two integrated circuits is described in this paper. The amplifier requires no adjustment and has a flat response from low frequencies and adequate bandwidth for high speed measurement systems.

Key-Words: - ultra low-noise preamplifier, MCP, SiPM

Received: February 22, 2020. Revised: August 31, 2020. Accepted: September 25, 2020. Published: October 18, 2020.

1 Introduction

There are numerous detection systems such as neutron time-of-flight [1], photon counting [2] and charged particles detection [3] where the signal level is sufficiently low that amplification with low noise and high time resolution is required to measure the radiation signal. When the signal level is low, there is a requirement for a low noise and low distortion amplifier to make the measurement feasible. Proposed designs of amplification modules [3, 4] can be found in literature that can attain very low noise spectrum densities but they may use DC coupling and lack the ability to reach an adequate high frequency cut-off close to 1GHz. DC coupling also amplifies DC errors and low frequency noise. Typically, low frequencies do not contain useful information for these types of applications and the suppression of these frequencies is preferred. AC coupling, however, can reduce the total output noise and eliminate the requirement for adjustment of the amplifier. Another advantage of AC coupling is that it eliminates the need to use a symmetrical supply to the amplifier and this simplifies the amplifier design.

In this paper a low cost, ultra low-noise preamplifier is described, with a flexible design that can be modified and adapted to any specific need. The final design is compact and adjustment free. A typical equivalent input noise voltage density of about 1.6nV/Hz1/2 and a high cut-off frequency (-3dB) better than 1GHz is achieved.

2 Design Considerations

There are three requirements that are difficult to satisfy in a preamplifier that is used in instrumentation. These are low noise, high gain and high bandwidth. For the attainment of low noise, the noise of the first amplification stage is a significant consideration. The contribution to the equivalent input noise of the following stages is divided by the gain of their previous stages so that generally the following stages do not contribute significantly to the equivalent input noise [5]. To achieve high gain, it is possible to connect several stages in series, however, this makes it difficult to achieve a high bandwidth as each stage must have a much higher bandwidth than the series combination.

For the first amplification stage, there are solutions that have an input voltage noise density less than 1nV/Hz1/2 for example the Texas Instruments LMH6554 [6]. However, such a device needs a lot of external components and for this reason the final design objective may not be achieved. The gain of such a device and its bandwidth are also marginal. Currently, the input stage of choice has become the Analog Devices ADL5566 [7]. Each stage of this device has a typical input voltage noise density about 1.3nV/Hz1/2 at a voltage gain greater than 3 for single end operation and a bandwidth of

4.5GHz under these conditions. Most of the passive components are inside the device and this enables easy construction. The quality of the external passive components can easily affect the characteristics of the device close to the 1GHz design specification. The minimization of the external components in addition to the dual construction in a single package (there are two identical stages in a single package) allows for an efficient printed circuit board (PCB) design.

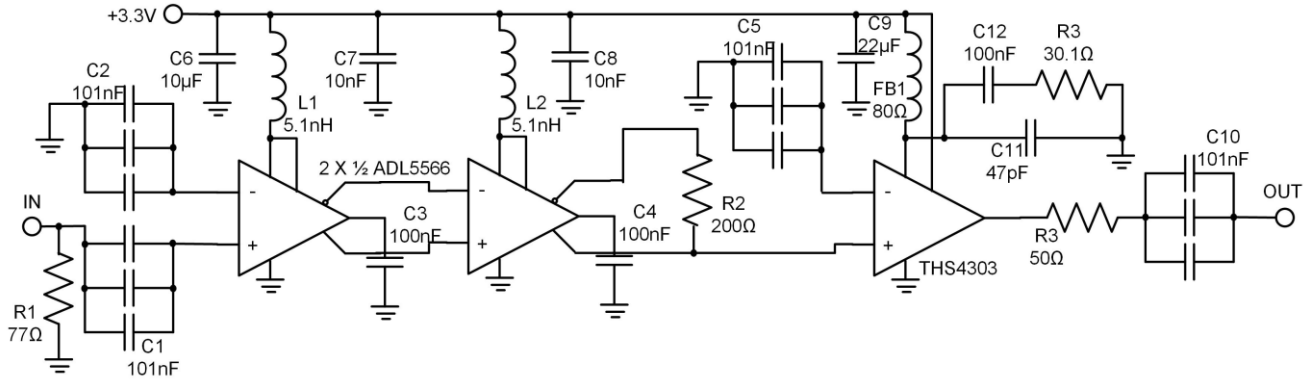

Fig. 1. The proposed preamplifier circuit.

Fig. 1 shows the preamplifier circuit design. To make an AC coupling from some 10's of kHz up to GHz frequencies special RF capacitors are required. Regular low frequency capacitors have a low resonance frequency that affects the response of the amplifier to frequencies close to 1 GHz. To overcome this problem, a parallel combination of a 100nF X7R dielectric, a 1nF C0G and a 47pF C0G, all 0402 footprint (Murata GRM155R71C104KA88D, GRM1555C1H102JA01 and GRM1555C1H470JA1D) is formed as a 101nF equivalent capacitor. This combination has low impedance at high frequencies. In this case, the low cut-off frequency of the amplifier is close to 50KHz. If a lower cut-off frequency is desirable another capacitance can be connected in parallel with this combination.

The Input stage is single-ended and asymmetrical. Although this type of design is not supported from the ADL5566 datasheet and application notes, it is used as it is expected to deliver higher voltage gain and lower noise. There is also an input impedance change with this topology but it is likely to be insignificant. The no-load voltage gain of the first stage is expected to be x6.25 (15.9dB). Between the first and second stage there is a direct (without the use of other components) DC coupling. The DC errors are insignificant and are unlikely to saturate the second stage output. This in turn minimizes the number of components used. In addition, the termination resistance of the first stage is only 160 Ω when compared to the 200 Ω that is specified. It is known that compensation and the high cut-off frequency are affected by this asymmetrical operation and the non-specified load. In this case it is not a problem as this stage has a much higher bandwidth than that required and thus the operation within the useful bandwidth is not affected. The second stage is normally terminated on a 200 Ω resistor. At the second stage's output a total voltage gain of x35 is expected.

According to the ADL5566 datasheet RG=80Ω and RF=500Ω. The input internal resistance (Ri) of the first stage is given [8,9]:

$$R_i = \frac{R_G}{1-\frac{R_F}{2\left(R_G+R_F\right)}} \Rightarrow$$

$$R_i = \frac{80\Omega}{1-\frac{500\Omega}{2\left(80\Omega+500\Omega\right)}} = 140.6\Omega \quad (1)$$

The lower cut-off frequency of the input formed RC can be calculated:

$$f_{-3dB} = \frac{1}{2\pi RC} \sim 11.5kHz \quad (2)$$

More than one high-pass RC are formed and determine the amplifier lower cut-off frequency. The actual amplifier lower cut-off frequency is always higher than the one from this calculation. To match the amplifier input internal resistance to 50Ω an external 77Ω resistor (R1) is placed in parallel to the input resistance Ri (140.6Ω||77Ω=49.75Ω). The first stage gain without load can also be found in respect to the differential output:

$$G_1 = \frac{R_F}{R_G} = \frac{500\Omega}{80\Omega} = 6.25 \quad (3)$$

The 5Ω output internal resistor of the ADL5566 forms a voltage divider with the 80Ω (RG) input resistance of the second stage. The divider ratio can be found equal to 0.941. The no-load voltage gain to

the ADL5566 second stage output can be calculated to 6.252·0.941=36.76. The second stage output formed voltage divider rounds the total ADL5566 voltage gain to 35.

For the final stage the fixed gain amplifier THS4303 (Texas Instruments) was chosen. This amplifier forms the final frequency response and provides a single-ended gain of 10. As only the one half of the previous stage signal is used (one end only) the amplification on this amplifier output is expected to be 175. Because this amplifier is specified to operate at 100Ω output load, a 50Ω resistor is placed in series with its output. This resistor forms a voltage divider with the 50 Ω output load and the final voltage gain will be 87.5. A resistor network can be used at the THS4303 output, as is show in Fig. 2, if a round value of amplification about 50 is desirable. Resistors R5 and R6 can be rounded in a higher value without a significant performance change.

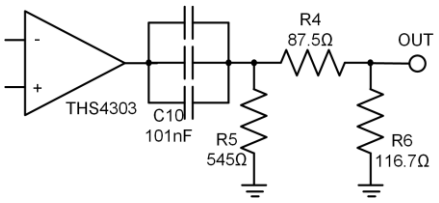

Fig. 2. Resistive network rounding voltage gain at x50 on 50 Ohm load.

3 Construction tips and operation

Some experimental prototypes were constructed in order to verify the operation and to ascertain the construction demands. The Printed Circuit Board (PCB) was designed to use two layers for easy construction. The signal path tracks that connect the output of the input stage with the input of the second stage (the connection between the two parts of the ADL5566) are paralleled with cables to reduce the tracks' inductance. One of the most difficult construction issues is to solder the 0402 size capacitors for the signal paths. 0402 size capacitors perform better than the 0603 at high frequencies and their use simplifies the circuit. All the resistors must be thin film. Small size is also preferred for the resistors. To supply power to the circuit, a mini USB connector was used. The supply voltage can be applied from a 5V mobile phone charger with a mini USB output plug. An AMS1117 low drop out (LDO) regulator was used to convert the input voltage to 3.3V that is required for a low noise circuit operation. A prototype circuit photograph is shown in Fig.3, where the dimensions of the final construction can be seen. The bottom layer "L" shape track is the heat sink of THS4303 that is connected to its inverting input (pin 14). It is likely that the thermal pad of this integrated Circuit (IC) can be connected to the negative plane, but this is not stated anywhere in the datasheet or the application notes.

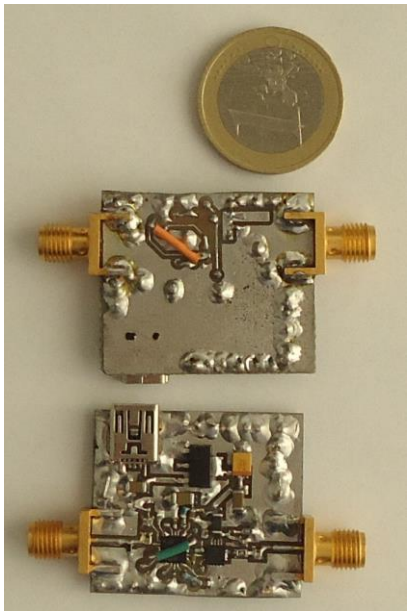

Fig. 3. Prototype circuit photograph

Some measurements of the prototype circuit frequency response are shown in Fig. 4 and a frequency response curve has been draw based on the measurements that were taken. The frequency response (-3dB) exceeds 1GHz when the preamplifier is terminated on a 50 Ohm load.

4 Simulation Results

In order to prove the proper operation of the proposed amplifier, and have a connection between theoretical calculations and experimental results the circuit should be modeled and simulated. This simulation is somewhat challenging. The proposed amplifier uses two integrated circuits from two different manufacturers. Thus the simulation is difficult in a single simulation environment. ADL5566 has no Spice [10] model, but THS4303 has PSpice and Spice for TINA-TI models. TINA-TI is a Spice-based simulator and for this reason is capable of simulating complex circuits. In order to use a Spice-based simulator the ADL5566 must be modeled. The datasheet of the ADL5566 contains an equivalent circuit and a frequency response that shows an increment of amplification before the upper cut-off frequency. Usually this type of amplifiers have low loop-gain and their frequency

response is affected from two poles that are relatively close to each-other. The simulation model for the ADL5566 that was used is shown in Figure 4.

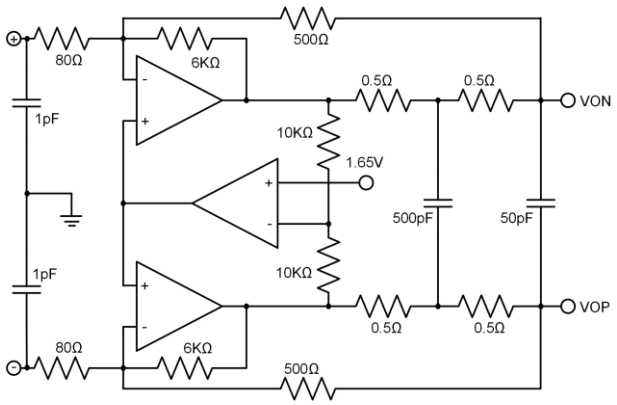

Fig. 4. The ADL5566 approximated Spice model.

The frequency response and the behavior of the ADL5566 equivalent circuit is close to those described in the ADL5566 datasheet. The simulation, using the TINA-TI, frequency response of the ADL5566 is shown in Figure 5.

Using the previously described Spice model for the ADL5566 the circuit can be modeled and simulated without problems using the TINA-TI. Each one of the capacitors that form the 101nF capacitor is modeled as a series RLC circuit. This is not accurate as the resistive part is not constant vs frequency, because it is depends on the dielectric losses. The R and L values were approximately extracted from their datasheet frequency characteristics. These values are shown on Table 1.

	GRM155R71C 104KA88D	GRM1555C1 H102JA01	GRM1555C1 H470JA1D
C	100nF	1nF	47pF
R	20mΩ	600mΩ	200mΩ
L	0.4nH	0.238nH	0.024nH

Table 1. Capacitors RLC model values

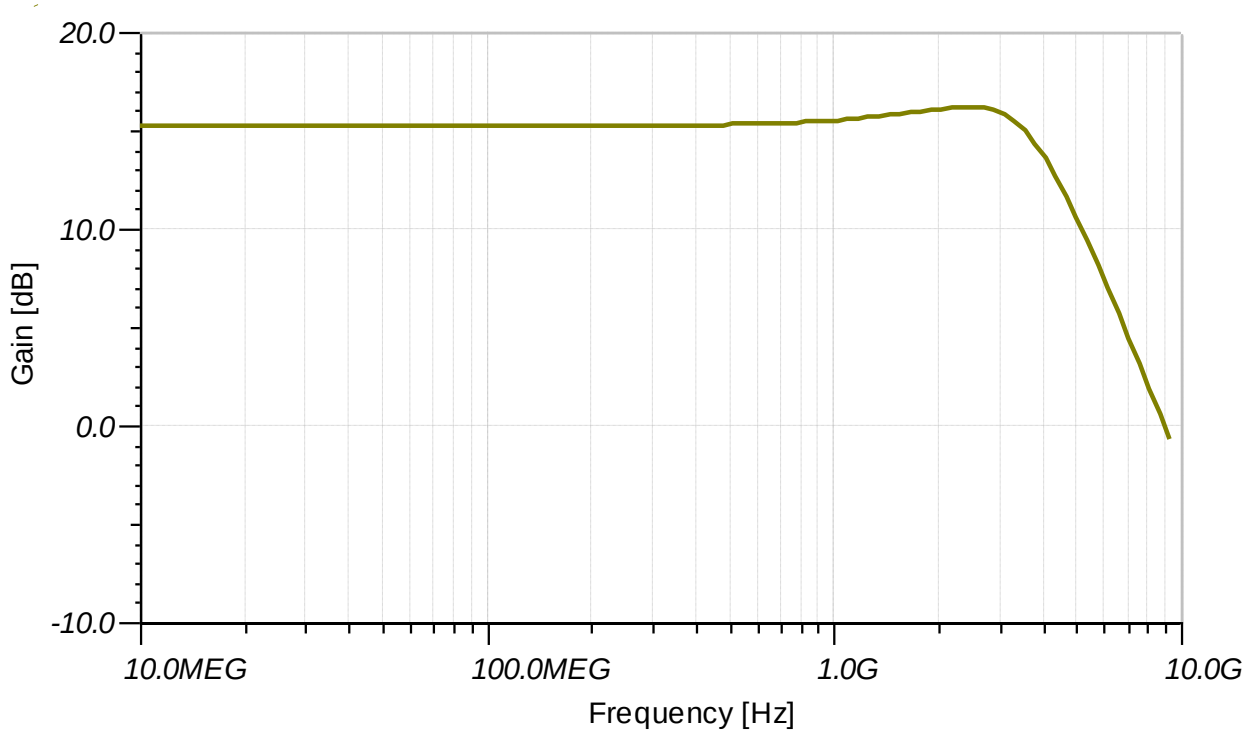

Fig. 5. The ADL5566 Spice model frequency response.

Using the models and parameters and the default TINA-TI model for the THS4303 several simulations of the proposed amplifier circuit were performed. The frequency response resulted from the simulation is shown in Figure 6:

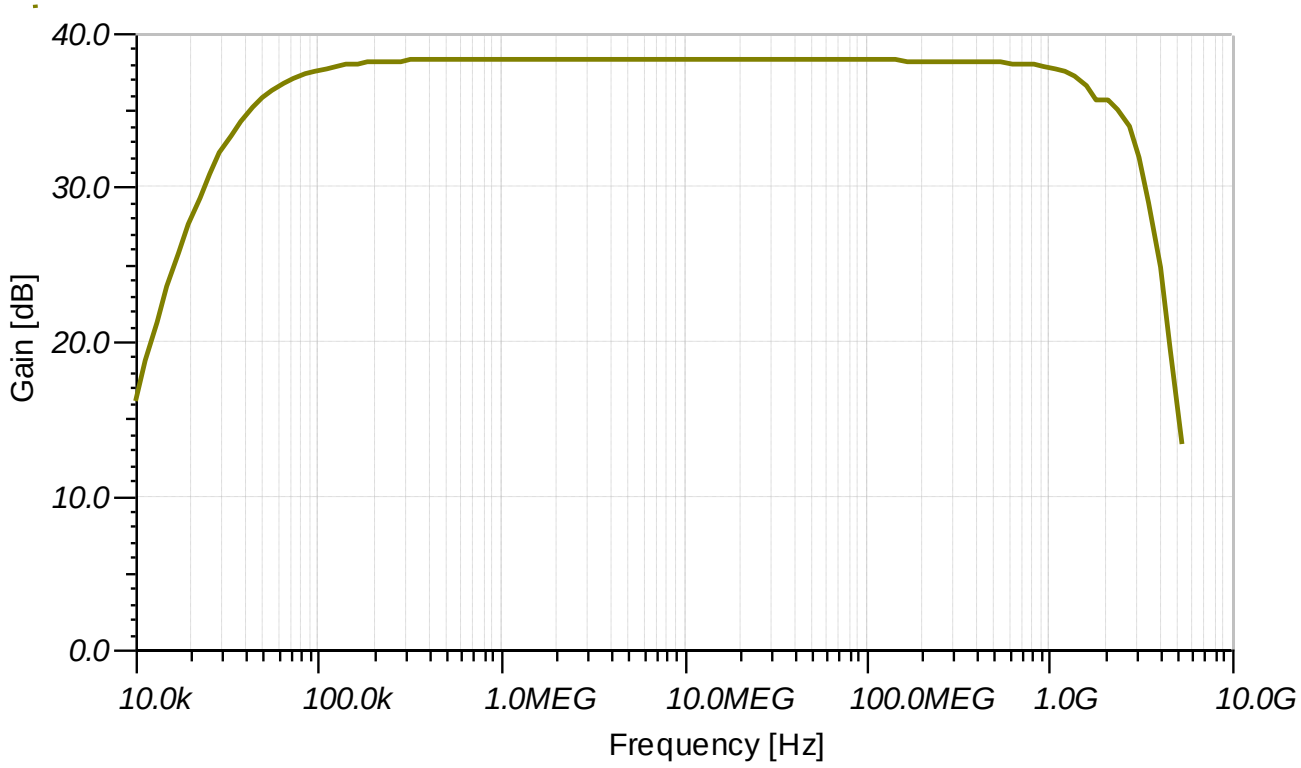

Fig. 6. The proposed amplifier simulated frequency response.

The frequency response curve that flattens exactly before the upper cut-off frequency was determined after several trials to originate from the parallel combination of capacitors that form the 101nF capacitor. In simulations this capacitor combination extends the upper cut-off frequency about 100MHz compared to the single 100nF capacitor. The simulated upper cut-off frequency is about 2.4GHz. Although THS4303 bandwidth is only 1GHz, the increment of the amplification close to 1GHz caused by the ADL5566 extends the upper cut-off frequency in simulations.

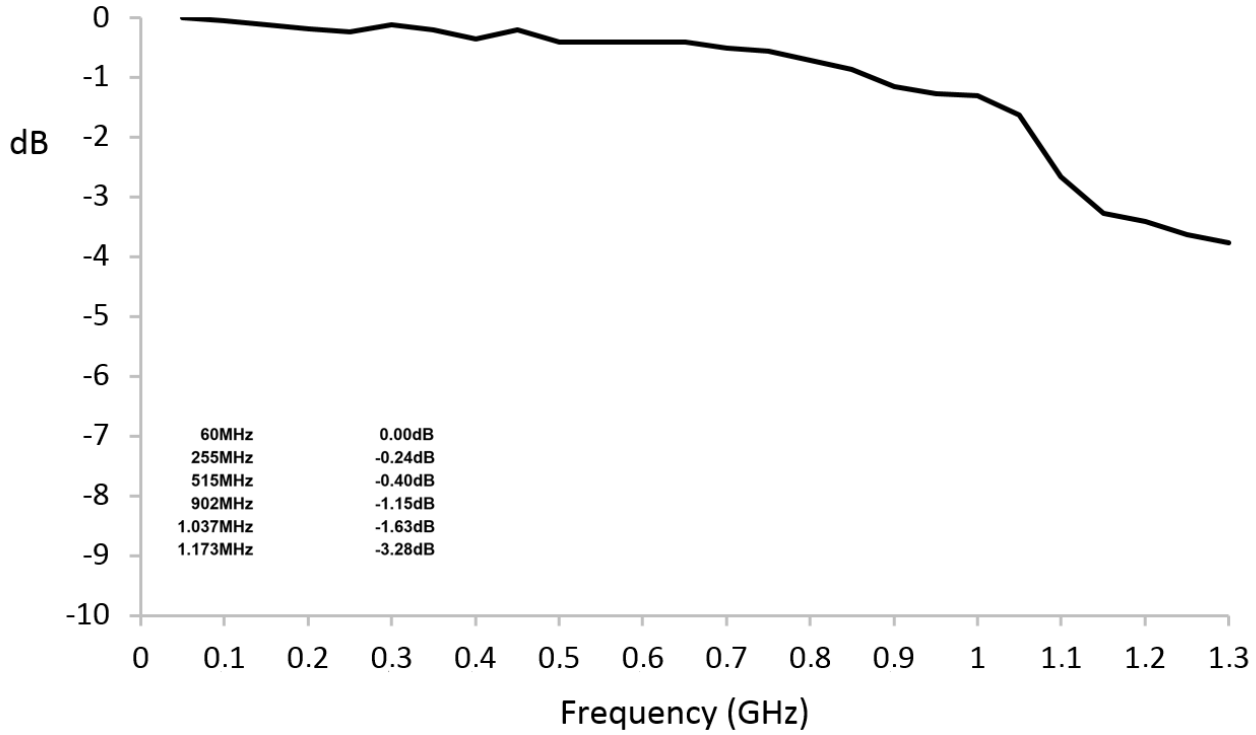

Fig. 7. Prototype circuit frequency response.

Some measurements of the prototype circuit frequency response are shown in Fig. 7 and a frequency response curve has been plotted based on the measurements performed. The upper cut-off frequency (-3dB) slightly exceeds 1GHz when the preamplifier is terminated on a 50 Ohm load. In comparison to the simulated frequency response we observe a small amplification decrement as the

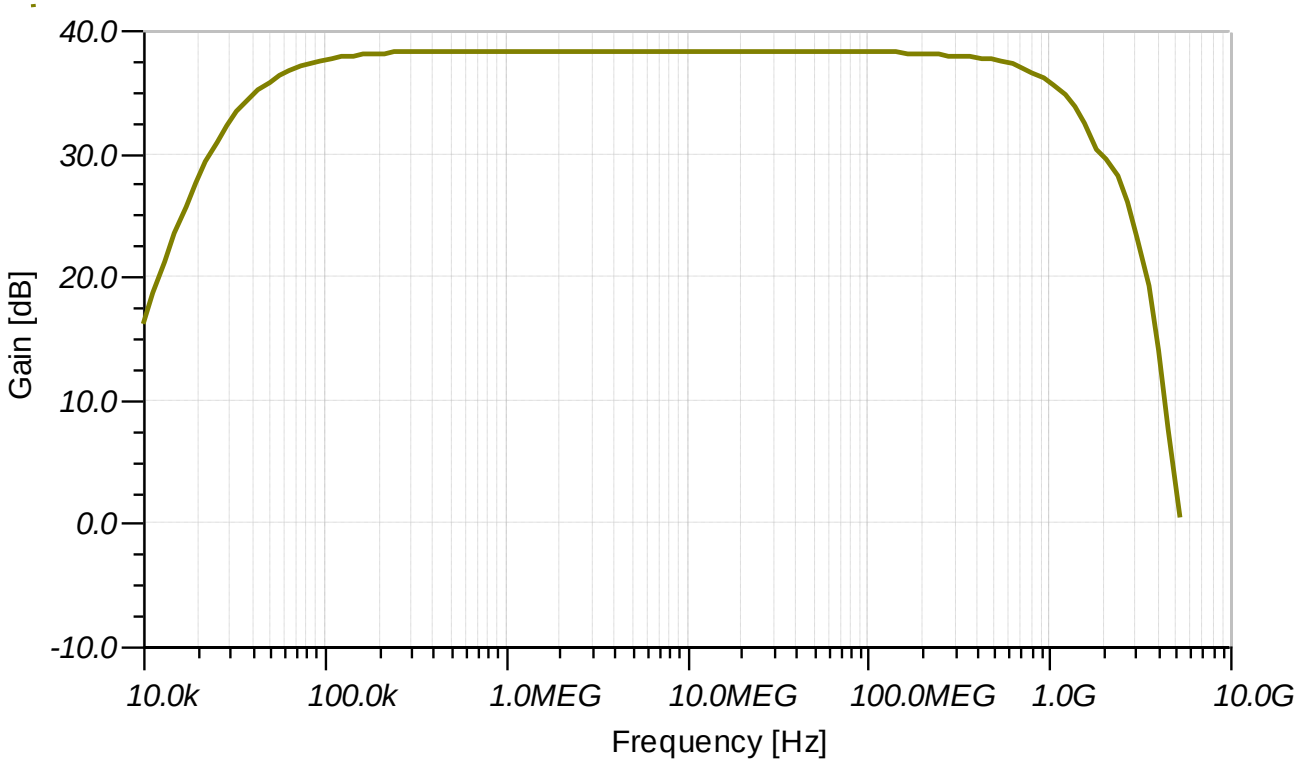

Fig. 8. The proposed amplifier simulated frequency response using a 50Ω||5pF load.

frequency increases. In practice this is normal and it is difficult effect to be modeled in a simulation in these types of high frequency circuits. This is affected by several factors such as capacitances on the PCB, inductances of the tracks, inaccurate models of the passive components and poles that are missing in integrated circuits default models. These factors are significant at high frequencies. In practice the circuit upper cut-off frequency exceeds the 1GHz and the circuit satisfies the purpose that it was designed for.

Several simulation trials were made to determine the cause of the simulated and measured frequency response curves. It was found that the series 50Ω resistor with the THS4303 output, limits the amplifier frequency response forming an RL low pass filter with the load capacitance. A small track over a ground plane on a common double layer FR4 PCB forms a capacitance of about 0.6pF/cm. As shown in Fig. 8, a 5pF of load capacitance limits the simulated frequency response close to the frequency response curve has been plotted based on the measurements performed. This capacitance is close to the measurement used setup.

5 Conclusion

The design of a high quality, compact 1GHz preamplifier suitable for operation in conjunction with micro channel plates (MCP) and silicon Photomultipliers (SiPM) is described in this paper. The 1GHz preamplifier comprised of two integrated circuits. The minimization of the external components ensures the ultra-low-noise operation and the low-cost design.

References:

[1] Mauri G., Mariotti M., Casinini F., Sacchetti F., C.Petrillo, "Development of pulse shape analysis for noise reduction in Si-based neutron detectors", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, Vol.910, 2018, pp. 184-193.

[2] Tosi A., Scarcella C., Boso G., Acerbi F. "Gate-Free InGaAs/InP Single-Photon Detector Working at Up to 100 Mcount/s", *IEEE Photonics Journal* ,Vol. 5, Issue 4, 2013, DOI: 10.1109/JPHOT.2013.2278526.
[3] Domienikan C., Costa P., Genezini F. and Zahn G. "Low-cost Amplifier for Alpha Detection with Photodiode", *International Nuclear Atlantic Conference - INAC 2017*, October 22-27, 2017.
[4] Flaxer, E., "A low-cost, ultra-fast and low-noise preamplifier for micro channel plates", *Measurement Science and Technology*, Vol.17, No.8, 2006, pp. N37-N40
[5] "Noise Specs Confusing?", *National Semiconductor Application Note 104*, May 1974
[6] lmh6554.pdf, "LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier", *datasheet, www.ti.com*
[7] ADL5566.pdf, "4.5 GHz Ultrahigh Dynamic Range, Dual Differential Amplifier", *datasheet, www.analog.com*
[8] MT-076.pdf, "Differential Driver Analysis", *Tutorial*, *www.analog.com*.
[9] AN-0990, "Terminating a Differential Amplifier in Single-Ended Input Applications", *Application Note, www.analog.com*.
[10] , *https://en.wikipedia.org/wiki/SPICE*.