Low Power Checks in Multi Voltage Designs

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Abstract: —Leakage power consumption has been almost a serious problem these days in semiconductor industry. Many low power techniques like multi-voltage, power gating etc. are deployed to improve power saving. Power aware verification hence has become a critical issue now. Static low power verification has been developed to verify that low power architectures are designed in correct approach meeting all electrical rules in SoC. The UPF(Unified Power Format) is the standardized format that has all power intent information and can be used throughout the design flow to ensure that the power specification is intact. Firstly, this paper describes the special cells and its operation used in low power techniques. Secondly it describes the major checks examined at each stage using Synopsys VCLP tool and finally debugging with the tool and conclusion.

Key-words – Power domain, UPF, low power cells, electrical connectivity, VCLP, missing special cells, multi-voltage.

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1. Introduction

While wireless devices are rapidly making their way to the consumer electronics market, a key design constraint for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries. So the most important factor to consider while designing SoC for portable devices is 'low power design'.

Growing need for portable communication devices and computing system has increased the need for optimization of power consumption in a chip. Another motivation: some major cells are idle for most of the operating time and some when active might not be critical in terms of timing. Optimization of power should be done at all different stages of VLSI design. While implementing low power techniques at logic synthesis and physical design, several problems arise in implementation. Low power SoC need several implementation level adaptions which uses industry level power format specification known as UPF (Unified Power Format)

Addresing the dynamic or leakage based power consumption using above methods required the use of standard which was different from traditional methods. This lead to development of UPF (Unified Power format), an open standard that allows designers to describe the power design intent. Implementation of design with UPF will cause different issues related to timing, congestion, placement etc. and are dependent on functionality, tech nodes, supply vol etc. Solving this implementation problems requires different methodology to solve each of them

2. Literature Survey

2.1 Power domains and Switching

In multi voltage designs, some domains has switchable supply which are called switchable domains. Power Management Unit is one of the units that controls power up and power down sequences. It toggles the control signals according to power sequence and allows current to the relevant power domains with help of power switches. Main idea of this is turnoff massive unused parts of the design and gain low current consumption.

2.2 Special low power cells

This section explains the working of six special cells used in implementing low power techniques in the design.

2.2.1 Isolation cell

The outputs of powered off domains will be floating as they don’t be active. These floating outputs cannot be the inputs of domains which are active. In order to solve this problem, a logic which is used to isolate two power domains is placed when one of them is switching OFF while the other is ON and the signal is going from OFF to ON domains. This isolation cell sends the actual signal to be sent to the ON domain that supposed to go from OFF domain and make sure active domains are no affected. Lack of isolation cell passes unknown signal (X) and causes leakage of power. If the signal passed is to be 1, then OR gate with one input as ‘1’ acts as isolation here. Similarly if ‘0’ to passed, then AND gate acts as isolation. There is one more type of isolation cell which is of latch type. Latch stores the outputs of power off domains and

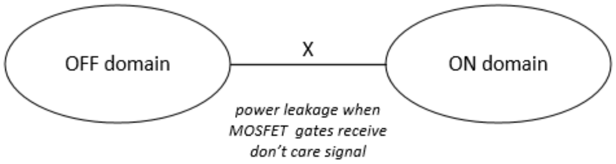


Fig 2.1 Signal transmission without isolation cell

The above figure depicts that when a signal goes from domain which is OFF, that cannot be a proper signal (0/1) but don't care. Now when an unknown signal reaches to any gate of a transistor in ON domain, operation of transistor may go abnormal and there can be chance of leakage from VDD to VSS

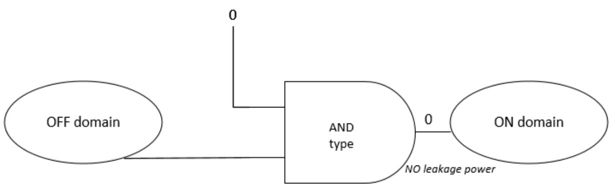


Fig 2.2 Signal transmission with isolation cell

The above scenario can be solved by placing isolation cell which allows a proper signal(0/1) to the ON domain.

2.2.2 Retention cell

When the power domain goes OFF, the state present in the flip flops will also be erased. Some IPs will need to retain their values for fast wake up. For the previous state to be preserved, this logic isi used. This has a flip flop and a state saving latch. The latch associated with it will retain the prior state when its power is off. The retention mode consumes little more current than power off mode but always allow fast recovery of the IP after waking up from sleep mode.

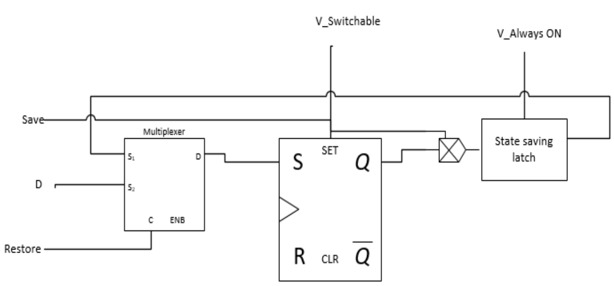


Fig 2.3 Retention cell

The retention is nothing but a flip-flop with restoring latch. The logic stored in flip-flop will also be saved in latch. The only difference is supply of flip-flop is switchable and latch is always on. The multiplexer allows us to save and restore the logic in latch.

2.2.3 Level Shifter

When the logic goes from higher voltage power domain to lower voltage power domain or vice versa, this logic should be used. This functions as a buffer while it shifts the power levels. Generally for HIGH to LOW type, as input is overdriven there is no need of level shifter in this case. But in LOW to HIGH type, as the input is under driven, the following domain which is operating at higher levels may not consider the signal value as it is in preceding lower voltage domain.

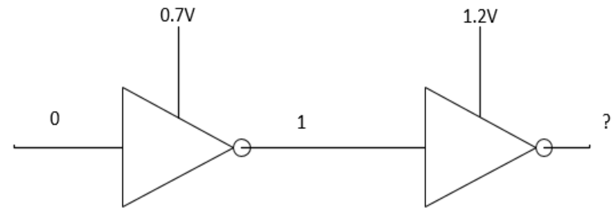


Fig 2.4 Showing need of LS from low to high voltage levels

From the above fig, first inverter has converted logic from 0 to 1 and the voltage level of this is 0.7V but, when it goes to higher voltage domains, this 0.7V may not be considered as logic high. Therefore, in this case LS is essential

2.2.4 Enable Level shifter

This performs dual function of both level shifter and isolation signal. So when the logic tranfers between two voltage levels and one is going to switch off, this has to be used.

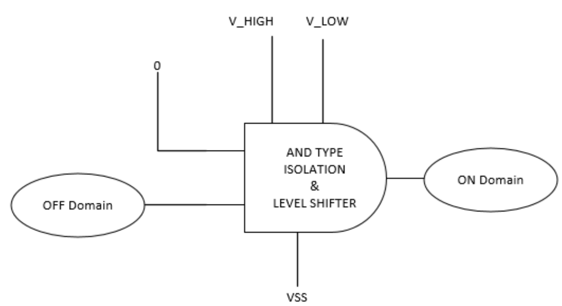


Fig 2.5 Enable LS

The voltage level of OFF domain is high (V_HIGH) and ON domain is low (V_LOW) in the fig.

2.2.5 Always ON cell

The logic used when a signal transfers through OFF domain while source and sink domains are switched ON

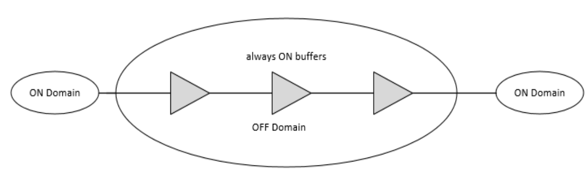


Fig 2.6 AON buffers placed in OFF domain to allow communication between two ON domains

These buffers are powered ON always irrespective of switchable supply of that domain.

2.2.6 Power Switch

Logic which is used to connect and disconnect the supply from MOSFET gates to make a power domain switchable.

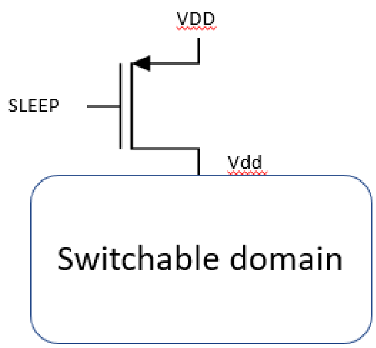


Fig 2.7 Header power switch

As shown in the figure, PMOS transistor acts as gating element in header switch. Whenever the swicthable domain need to work, then the supply for that is given by sleep signal of PMOS transistor.

2.3 Verification on of power intent

Steps involved in low power flow:

i. Define and capture the design intent for SoC in RTL and power intent by creating a UPF file. power options can be explored using UPF file, while maintaining the integrity of design as captured in golden RTL.

ii. Verify the contents of the UPF file using quality checks, which ensure that UPF is syntactically correct, power intent is complete, design and power intent are aligned properly. For example, identifying isolation or level shifter definitions in upf. Finding missing these definitions by using formal techniques will save simulation and synthesis debugging later.

iii. Next step is to verify the correct functionality of the design with low power behavior superimposed on top of functional behavior, RTL, through simulation.

iv. Continuing the above, Power Shut Off is effectively simulated to ensure that the chip functions correctly with few portions turned off and the same portions can recover after powering them up. The control signals specified in the strategies of isolation, level shifter etc. are generated from power management unit (PMU). Low power behavior is triggered when these control signals are asserted.

v. Just before shut off, isolation enable signal is asserted. But between isolation insertion and power off, retention signal is asserted by PMU, which causes the simulator to store the current values of all retention flops specified in UPF.

vi. Conversely, on power up, retention flops restore the retained values and isolation values forced on outputs will be removed.

2.4 UPF file structure

create_power_domain
set_domain_supply_net

create_supply_ports
create_supply_net
connect_supply_net

add_port_state
add_pst
create_pst

create_power_switch
map_power_switch

set_isolation
set_isolation_control
map_isolation

set_level_shifter
map_level_shifter

set_retention
map_retention

Fig 2.8 UPF file structure

3. Stages of running VCLP checks

VCLP involves three separate stages while performing checks. These are organized as below:

a. Design/UPF creation:
As the implementation of the design is not yet done, checking for insertion of special cells & PG related issues doesn't make any sense. Checks at this stage predicts any further problems which can be encountered in later stages. Example problems detected at this stage can be:

- Inconsistency between UPF parts where the source is OFF and sink is ON, but isolation strategy is not defined in UPF file.

b. Post-synthesis:
Here all the previous stage checks must be performed. Although the UPF may be stable at this point but design changes may cause new UPF consistencies. In that case, UPF need to be changed accordingly. Example problems at this stage are:

- Missing level shifter at the crossing in the design where it is needed

- Isolation is present where it should be, but the isolation enable signal is not connected to the port which is mentioned in UPF.

c. Post-route:
Again all the previous checks must be performed. In addition whole power and ground checks need to be done for electrical correctness and whether consistent with UPF.
Example problems:
- A level shifter's primary supply doesn't match with the driver's supply of it
- A macro power pin's supply doesn't match with that of UPF's

4. VCLP Design flow

Following shows the design flow of the tool used for low-power verification. UPF file is used in various stages in the design flow. UPF check is done before synthesis to ensure the consistency. It is then passed to perform low power synthesis using design compiler. DC will write all other low power information in incremental UPF. Both golden UPF and incremental UPF are used to perform UPF check and design check to verify the low power insertions during synthesis. After PNR, in addition to the above checks, PG check is also performed using UPF and physical netlist.

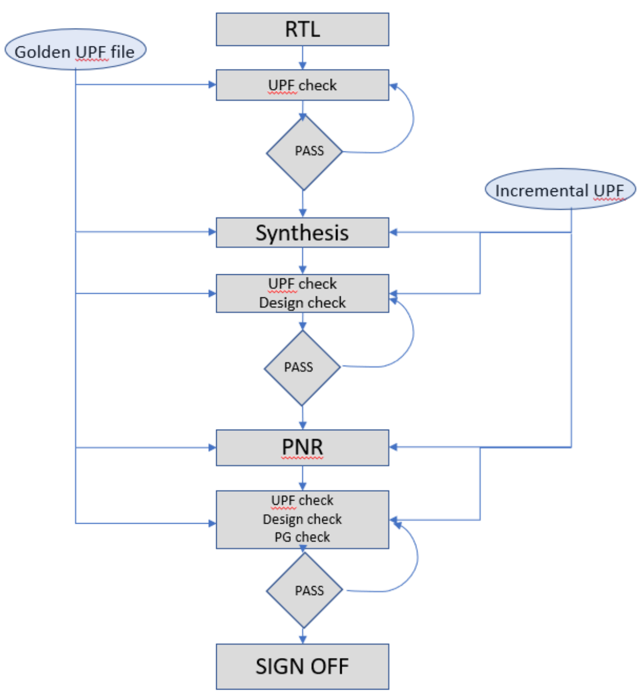


Fig 4.1 VCLP design flow

5. VCLP Checks

5.1 Signal corruption checks

Detects the violating low power architecture at gate level netlist

5.2 Structural checks

Formal verification in low power implemented designs validates two factors. (i) Low power verification (ii) logical equivalency.

For low power verification, the focus is to ensure that the design is electrically correct and has less leakage power in view of low power. The flow verifies whether the special cells are implemented correctly in the design as defined in UPF file. And also checks the state retention and isolation control signals are driven correctly by domains that are powered up and tests for power control functionality.

5.3 Power and Ground checks

Checks the PG consistency against UPF for power network routing on physical netlists.

5.4 Functional Checks

Validates the correct functionality of special cells like isolation cells, power switches, etc.

6 Major Checks

In our design we found the following are the major violations need to be fixed. Mentioned below here are the rule name of the violation in VCLP tool.

6.1 Isolation Strategy missing: Isolation cell is required at the crossing according to PST states set in UPF, but the strategy is not defined. For this we have to verify the PST states whether they are defined appropriately. If it is correct, then have to protect that cross-over by writing the strategy.

6.2 Isolation buffering issue: This error flags out when source supply where the signal is coming from is OFF and instance in between is ON or instance is ON and sink supply where it is going to is OFF.

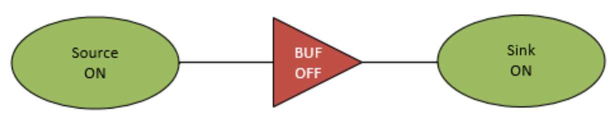
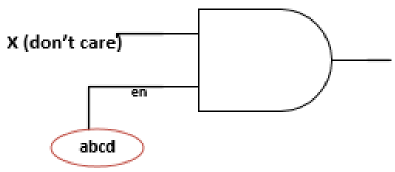


Fig 6.1 example of ISO_BUFINV_STATE

With this we get not only electrical violation but also functionality of the design gets corrupted. This causes the design to consume excess leakage power and function improperly. This can be fixed by either inserting isolation cells or swapping the type of cells to AON and provide the secondary supply as needed accordingly after ensuring the PST defined is correct.

6.3 Control pin of isolation connection: An isolation signal has two inputs, one is the clamp value which should be sent to sink side and the other is enable signal which tells the cell to work as isolation or just buffer. Now that enable signal will already be defined in UPF. But while implementing if the design hooks up to other port which is different from that of UPF's then we get this error. Here we need to check why is connected wrongly and if it is not ignorable then we have to hack the UPF or correct in the design.

```
set_isolation_control isolatio_policy
-domain <power_domain>
-isolation_signal abc
-location self
-isolation_sense low
```



As shown above the isolation signal mentioned in the UPF is different from the design

6.4 Isolation strategy supply: According to the PST states, the isolation cell is seated at the crossover but the supply of it can be less ON than source and sink. So here we have to make sure that the power of it is ON at least as long as the sink supply is ON. Sometimes we get this error when isolation is working as buffer (where data is some constant not don't care). In that cases we ignore it.

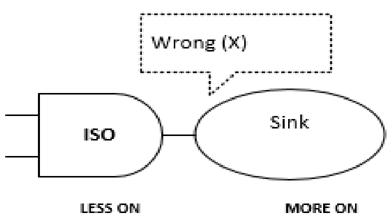
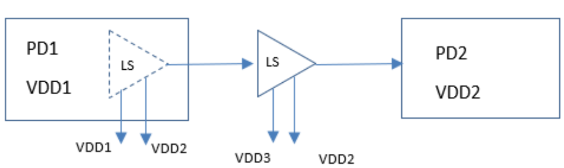


Fig 6.2 ISO should be ON as long as sink is ON

6.5 Standard cell mail rail connection of level shifter: Generally level shifter should be placed in the domain where it gets the rail voltage (primary supply). SCMR stands for standard_cell_mail_rail. This attribute is present on LS input & output pins. Input supply should match the primary power and output supply should match secondary power. Now we get this error when LS is placed in the domain where it gets wrong source/sink supply. If this is the actual issue, then we have to fix this by running synthesis again making sure that LS sits in right place.



In the figure shown above, LS is shifting voltage from VDD1 to VDD2. According to the strategy written in UPF, LS supposed to be placed in power domain PD1 and get the supply VDD1 but as it is outside, it is getting some other supply (VDD3) which is not intended. Normally, the LS will be placed automatically by tool. We need to fix this by giving some procedure to the tool and run synthesis.

6.6 Supply short: If PG pins of the instances are connected to same UPF supply, this error flags out. The supply shorts are serious electrical violations if shorts are found between ground and power pins. But most of the time we see the redundancy of power pins and hence the short will be between two power pins i.e., primary & secondary. In this case it doesn't make any serious problem but the instances having two power rails (Always ON) consumes a lot of area. If this instances are more in number, then we increasing the area of an IP. So it is always better to swap the AON cell to normal type.

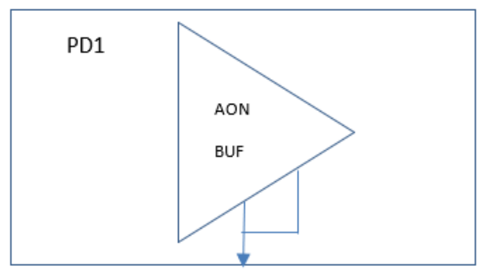


Fig 6.3 AON dual supplies are shorted

In the above figure, primary & secondary supply are shorted. This cell can be replaced with single power rail cell.

6.7 Heterogeneous strategy of level shifter: If there are heterogeneous sinks of different supply which needs LS from source, then LS strategy should be defined at inputs of two sinks separately. If it is defined only at source then this error flags out. Also in multiple mixed fan-out scenarios, LS strategy written at source cannot be valid for multiple fan outs at the same time. In this case, we should ensure that there is no strategy written at source side but at each sink separately.

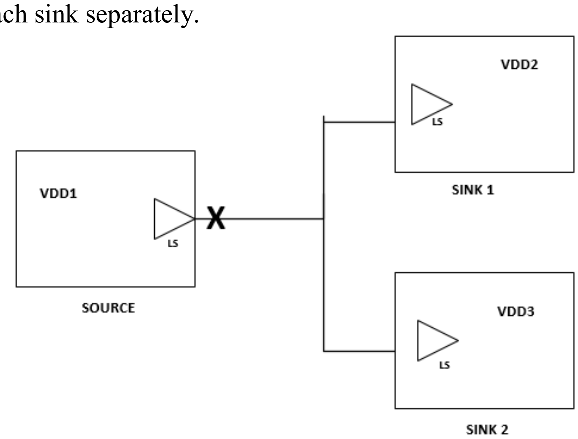


Fig 6.4 placing LS in hetero sinks

In the figure shown above, LS sitting at source side ios wrong as it shift the power levels to either of the sinks but not for both. Therefore it should be inserted at the inputs of each sink.

6.8 Power/ground data supply: Design methodology prescribes that logic pins should not be directly connected to the supply in the design. It is suggested that they should be tied to TIE LOW or TIE HIGH cells. These cells avoid the direct connection to the power/ground network. Why are these required? To avoid ESD (Electro-Static discharge) into gate. Gate oxide in a transistor is thin and sensitive to voltage surges.

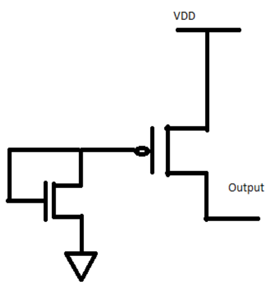


Fig 6.7 Tie high cell

6.9 Power/Ground logical connection: UPF supply net doesn't match with actual design supply net of instance. In UPF, supply of a pin is explicitly defined with *connect_supply_net* command.

connect_supply_net VDD1 -ports abc/vcc (UPF definition)

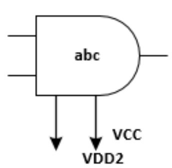


Fig 6.6 Instance supply(vcc) connected to VDD2

As shown above, in UPF the supply given to vcc pin of abc instance is VDD1 but in design it is connected to VDD2. So we have to review the logic path and confirm which supply must be hooked to and either change UPF or correct design such that they correlate properly. In early stages, we don't do power connections and at that stage it can be ignored

6.10 Power switch ack port driven : Acknowledge port of a power switch should not have any driver because that will be eventually driven by ack pin of power switch instances once they are implemented in the design. Other than this ack pin, if any buffers or other cells are found in fan-in they are considered as invalid drivers and this tag flags out. In this case, need to modify UPF in RTL and logical stages and make sure that we leave the ack port undriven.

7 Challenges in low-power verification

7.1 Isolation instances missing at insert dft stage

Design compiler tool inserts the isolation instances in synthesis before compile stage where there is a crossover. But there is one more stage after compile called insert_dft, where new scan flops and other logic gets added. Then tool doesn't automatically place isolation cells. Then tool flags out an error ISO_INST_MISSING in thousands. This can be solved by writing the isolation strategies in incremental UPF at that stage taking reference with already existing strategies in UPF.

7.2 Buffer insertions in timing ECOs

During timing ECOs, lots of buffers gets added in setup/hold fixes. However, ICC2 doesn't handle the power domain aware placement very well. So it places those buffers in wrong domain while implementing ECOs. Sometimes there will be more back to back buffers placed in wrong domain. Manually getting all these buffers might go wrong or can take many iterations. So we managed this by scripting in TCL language and made it easier for debugging with less manual effort.

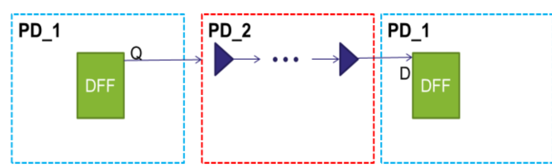


Fig 6.7 Adding setup/hold buffers

8 Results

This power aware simulation gives us simple report that can be easily understood and makes debugging uncomplicated. We can run and get reports from starting stage which lessens the burden at final stage of the design. Not only that if partition owner wants to change the design, these reports can be used as guidance and modify the design accordingly. The two inputs required for the tool are *power aware gate level netlist* which contains power aware design physically connected and *UPF file* containing logical connectivity.

As discussed in this paper, our multi voltage design consists of all the six special cells that are needed for low power design. Following is the low power intent present in our design.

```
vc_static_shell> report_upf
Design top                    : ,
Isolation instances           : 19988
Level shifter instances       : 238
Retention instances           : 4136
Power switch instances        : 3990
Multirail macro instances : 1
Total instances               : 2177750
Crossovers                    : 298383
Merged power states           : 131078
```

Schematic - Debugging in VCLP

With VCLP tool, we can easily trace the driver and load information when violations show up the at the domain boundary, in addition all low power related information is shown in the interface. The connectivity information is shown on the left side and low power property of the violation on right side.

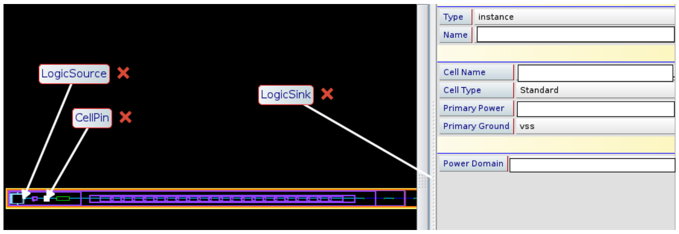


Fig 8.1 Debugging in VCLP

The violations flagged out in our deisgn are as follows. We debugged each violation and tried to lessen the electrical violations in the design.

Management Summary

Stage	Family	Errors	Warnings	Infos	Waived
UPF	Isolation	117	2	0	0
UPF	LevelShifter	29	3	20	0
UPF	UpfConsistency	4	0	0	12
Design	Isolation	91	2	0	0
Design	LevelShifter	186	8	0	0
Total		427	15	20	12

Fig 8.2 Management summary - list violations of all special cells

Tree Summary

Severity	Stage	Tag	Count	Waived
error	UPF	ISO_STRATEGY_IGNORED	110	0
error	UPF	ISO_STRATEGY_MISSING	7	0
error	UPF	LS_STRATEGY_MISSING	29	0
error	UPF	LS_SUPPLY_UNAVAIL	4	0
error	UPF	UPF_SUPPLY_NOSTATE	0	12
error	Design	ISO_BUFINV_STATE	79	0
error	Design	ISO_INST_MISSING	7	0
error	Design	ISO_SINK_STATE	5	0
error	Design	LS_INST_MISSING	186	0
warning	UPF	ISO_STRATCONTROL_GLITCH	2	0
warning	UPF	LS_SCMR_MIXED	3	0
warning	Design	ISO_CONTROL_GLITCH	2	0
warning	Design	LS_LOCATION_WRONG	8	0
info	UPF	LS_MAP_MISSING	20	0
Total			462	12

Fig 8.3 Tree summary – detail each violation

```
Tag             : RAIL_BUFINV_STATE
Description     : Supply off for buffer/inverter [Instance], but sink
                  [LogicSink] supplies on
Violation       : LP:3446
Instance        : BUF_inst_4
Cell            : M10S31_BUFX4
CellPin         : o
EndOfChain      : BUF_inst_1/o
LengthOfChain   : 1
LogicSource
  PinName       : AON_reg_387/q
LogicSink       : AON_phy_top_inst/i_standby
```

Fig 8.4 Detail information about the violation

9 Conclusion

Power aware verification is very well necessary for today's designs. Working and usage of special cells in low power design are explained. And also how the VCLP tool carry out the checks are illustrated. With the help of Synopsys VCLP, we have performed the low power checks in our design and mentioned the challenges we faced with design.

10 References

[1] Synopsys VC LP User guide, Version L-2016.06, June 2016

[2] Practical guide to low power design - https://projects.si2.org/events_dir/2009/PowerForward/LowPowerGuide09232009/pfi_lpg_chapters/lpg_sect1_06052009.pdf

[3] Liang, Chao. "Mixed-signal verification methods for multi-power mixed-signal System-on-Chip (SoC) design." 2013 IEEE 10th International Conference on ASIC. IEEE, 2013.

[4] Bembaron, Freddy, et al. "Low power verification methodology using UPF." Proc. DVCon (2009): 228-233.

[5] G. Gokulakrishnan, V. Ramesh, MFFA based Optimal Location and Capacity of UPFC for Improving the Loadability of Power Systems, WSEAS Transactions on Power Systems, Volume 13, 2018, pp. 399-413