Digitally Controlled AGC with Programmable-Gain Amplifier for DVB-T/H

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Abstract. This paper describes a digitally controlled automatic gain control (AGC) subsystem for the analog front-end (AFE) supporting the digital video broadcasting in DZIF (double conversion with zero second IF) architecture. The receive path contains a programmable-gain amplifier (PGA) with self-tuning gain circuit. The dynamic range of the PGA is 51 dB controlled by a digital loop to form a first order control system. The third-harmonic distortion is less than -60 dB for differential input signal up to 160 mVpp. The supply voltage used is 1.8 V and the power consumption of designed chip is 13 mW. The nonlinearity of the proposed design verified by HSPICE post-layout simulation is better than -60 dB at every MOS corner, which is suffcient for the system specification. This chip is fabricated on TSMC's standard 0.18 m 1P6M CMOS technology.

Keywords: Programmable-Gain Amplifier, Video Broadcasting, Multimedia Technology

1 Introduction

With the advance of the multimedia technology and the network universalizing, the audio and video information can be transmitted in the binary data. The advances in digital transmission for mobile video-casting are now widespread thanks to the solutions for digital video broadcast to hand-held devices (DVB-H) and video streaming. Hence the Cell phone with TV receivers can catch the latest news, sports, view your favorite comedy show, or watch cartoons with high quality entertainment even that there is no network access. The DVB-H standard was formally adopted as an European Telecommunications Standards Institute (ETSI) standard in November 2004 [3]. Furthermore, DVB-H is officially endorsed by the European Union as the "preferred technology for terrestrial mobile broadcasting from March 2008 [4].

The concept of the single-chip tuner presented in this paper is based on attempting to capture the advantages and eliminate the disadvantages of some existing architectures. Fig. 1 shows a typical architecture of the double conversion system with zero second IF (DZIF). As its name suggests, the DZIF system is a combination of a double conversion superheterodyne and a zero-IF tuner. It is similar in structure to that proposed in [1] and [2], with a high rather than a low first IF. The interest RF channel is translated to higher IF using a tunable LO. Table 1 summarizes the baseband channel requirements for the DVB-T COFDM modulation scheme and the main requirements for this tuner. This receiver RF signal is translated to an 8MHz signal bandwidth for the required ADC.

The COFDM (Coded Orthogonal Frequency Division Multiplexing) modulation scheme used in DVB-T is well suited to the difficulties of a terrestrial transmission channel. OFDM is a multi-carrier modulation, with the digital bitstream to be transmitted being broken down from one high-rate stream into many lower rate streams. Each lower rate stream is transmitted on a separate OFDM subcarrier; using QPSK, 16-QAM, or 64-QAM constellations. The required signal to noise ratio (SNR) at the receiver depends on the constellation size of QAM. For a bit error rate (BER) of 10^{-7} in ADSL system, for example, 64-QAM requires about 27.7 dB whereas 16-QAM only requires 21.5 dB on an additive white gaussian noise (AWGN) channel. The dynamic range and linearity of the ADC (analog to digital converter) can be briefly defined according to the PAPR (peak to average power ratio) and the averaged signal strength. Unfortunately the PAPR is especially large in multi-carrier systems and hard to calculate precisely in

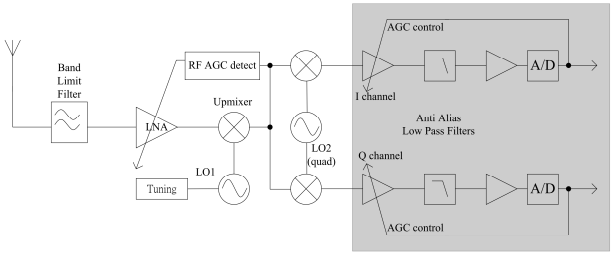


Figure 1. A typical architecture of wideband IF receiver with double conversion.

Table 1. DVB-T/H baseband channel requirement [1][2].

RF input Frequency Range	45~862 MHz (approx..)
Channel Bandwidth	6~8 MHz
COFDM bandwidth	5.5~7.5 MHz (approx..)
C/N Requirement	5.6 dB (QPSK 1/2 code rate)
	24.8 dB (64-QAM 3/4 code rate)
Dynamic gain rage	0~53 dB
Total harmonic distortion	< -60 dBm
Cut-off Frequency	4 MHz

wireless system. While the AGC adjusts the averaged signal strength to a constant level, what importance is to determine the reference power level. The paper is relevant to reduce the gain error and minimize the converged time with the high linearity AGC.

2 Digital Feedback Loop AGC

Typically, there are two types of AGC scheme, which are feed-forward AGC and feedback AGC. The feedback type AGC has the more advantages such as more precise performance and lower frequency noise. However, the acquisition time is rather long because the loop bandwidth is much smaller than the frequency of signal proceeded. In a wired communication system with time-invariant channel, it is popular that the feedback type AGC is considered [5][6][7][8][9]. For wireless systems, the feedback AGC is still employed in spite of the fact that the wireless channel is time-variant [10][11][12][13].

2.1 VLSI AGC Architecture

A traditional analog gain control structure is less flexible than digital one. Fig. 2 show the proposed control architecture to combine the digital gain control loop with narrow bandwidth and the wide bandwidth analog signal path. Notably, the former need a DAC (digital to analog converter) to convert the digital feedback signal from the DSP into analog signal. A decoder is used here instead .

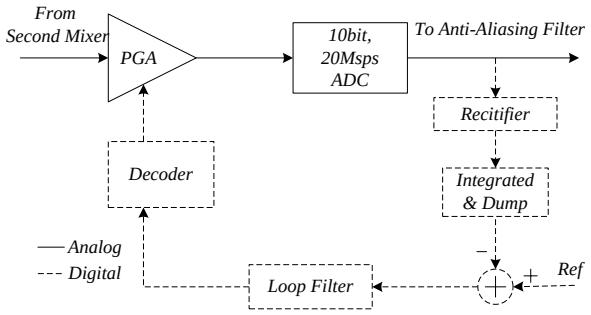


Figure 2. Block diagram of the proposed AGC

2.2 First Order Approximation Analysis

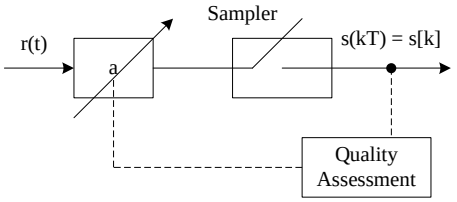


Figure 3. Brief diagram of the of AGC

Is there an adaptive element that can accomplish task? In the past, almost all AGC structures have been constructed as a first-order loop [5]. Since it can eliminate the overshot which might cause gain error and power waste. In the beginning of iteration and optimization shown in Fig.3, one reasonable goal is to minimize a simple function of the difference between the power of the sampled signal $s[k]$ and the desired power d^2 [14]. For instance, it is a popular cost function to minimize the averaged squared error in the powers of s and d, defined as follows:

$$\begin{aligned} & J_{LS}(a) \\ & = avg\{\frac{1}{4}(s^2[k] - d^2)^2\} \\ & = \frac{1}{4}avg\{(e^{\beta a(k)} \cdot r(k))^2 - d^2)^2\} \end{aligned} \quad (1)$$

The output signal level of PGA is function of its control signal. The exponential model for PGA is adopted in the design since the small signal PGA gain a is proportional to the control signal only and independent on the input signal $r(t)$. Applying the steepest descent strategy yields

$$a[k+1] = a[k] - \mu \frac{dJ_{LS}(a)}{da}|_{a=a[k]} \quad (2)$$

According to Equ. (2) and (3), the following algorithm is obtained:

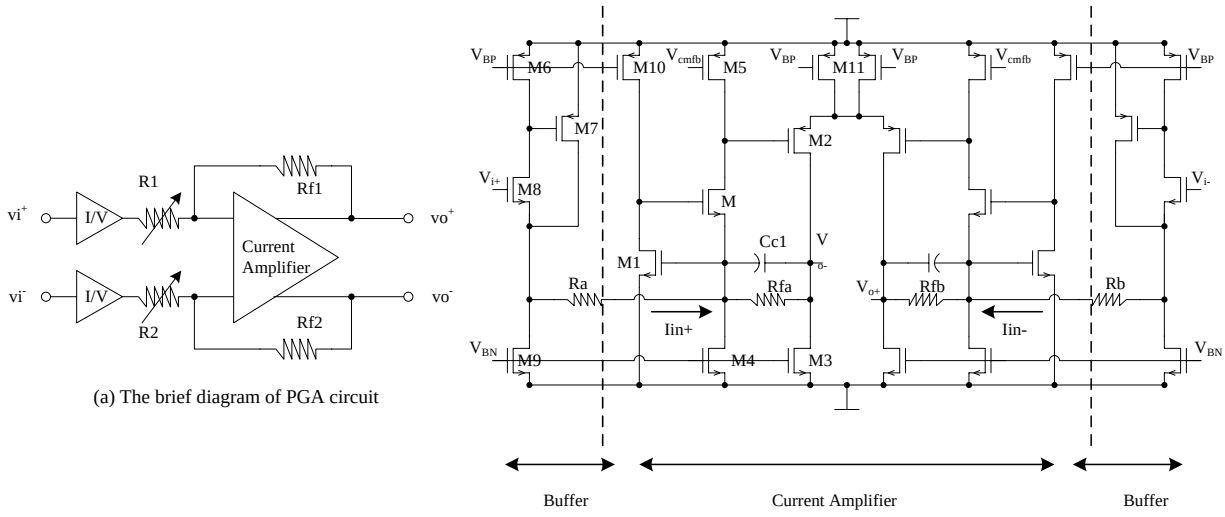
$$a[k+1] = a[k] - \mu \cdot avg\{s^2[k] - d^2\} \quad (3)$$

3 PGA in AGC Loop

As mentioned before, the main function of the AGC is to limit the dynamic range of the A/D converter. The requirement of the AGC is to have a large dynamic range. It's tough to use a single VGA to realize a wide dynamic range (DR) of tuning. The three stages of individual PGAs to attain the required 51dB gain range is proposed. While some dynamic range is alleviative in the RF-AGC of RF front-end, the rest DR design in baseband is shown in Fig. 5. The priority of the gain partition is considered about the low noise enhancement, but it is also a trade-off between SNR and NF (noise figure).

3.1 Schematic of PGA

The PGA cell shown in Fig.4 has a current feedback topology of the circuit [6]. For the system consideration, the variable gain amplifier with constant bandwidth is what we want. The shunt-shunt structure can provide the immutable bandwidth while changing the resistor network Ra, and the overall voltage gain is ratio of Rfa/Ra. The input stage, M6-M9, is the super-source follower providing low output impedance. The variable resistors, Ra and Rb, are two digitally-controlled switched resistor networks as shown in Fig. 6. These resistors are weighted to obtain a linear-dB gain step with a step size of 1dB. Two resistors networks are been designed for 6 dB of coarse tuning and 1dB of fine tuning. The required resistor values are shown in Table 2. It's not important to confirm neither the absolute nor the relative value of the resistors, since the gain of mismatch which is caused by the process variation can be fixed by the digital feedback loop.



(a) The brief diagram of PGA circuit

(b) The schematic circuit of PGA

Figure 4. The Programmable-Gain Amplifier circuit

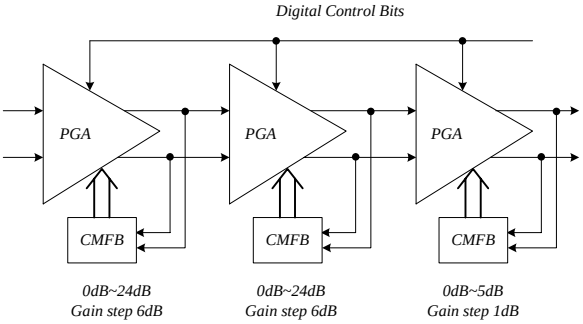


Figure 5. Gain Partition of Proposed AGC

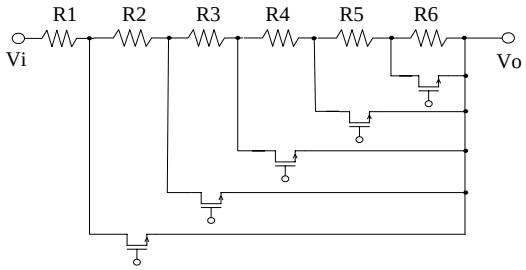


Figure 6. Schematic of Variable Input Resistors

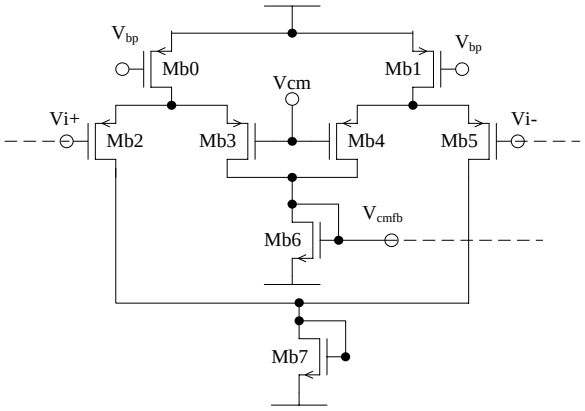


Figure 7. Common mode feedback circuitry

The high-gain current amplifier has low input impedance and high output impedance with the gain-boosting scheme. To enable the capability of common-mode rejection, the second gain stage is implemented using source-coupled pair. Fig. 7 shows the continuous-time common-mode feedback which is employed to stabilize the common-mode voltage. The transfer characteristic of the current amplifier is linearized by two fixed resistors, Rfa and Rfb. The open loop gain of the current amplifier is summarized as follows:

$$A_{iv} = \frac{g_m R_f}{1 + g_m R_f} \cdot R_L \cdot (g_m r_o) \cdot A_{2nd} \tag{4}$$

$$A_{close\_loop} = \frac{A_{iv}}{1 + A_{iv}\beta_g} \tag{5}$$

where A_{2nd} is the gain of M2 and M3. From Eq. (5), $A_{iv}\beta_g$ should be large enough to assure that the ideal formula of feedback topology is correct. A high A_{iv} and large feedback resistor Rfa is what the commentary cites above.

Table 2. Common mode feedback circuitry

Required Resistor Value		
Resistor	Coarse Tune	Fine Tune
R1	500Ω	4kΩ
R2	500Ω	500Ω
R3	1kΩ	550Ω
R4	2kΩ	610Ω
R5	4kΩ	695Ω
R6		775Ω

3.2 Linearity of PGA

The primary issue of this design is the noise analysis of the PGA. There are two part of the noise source, one is

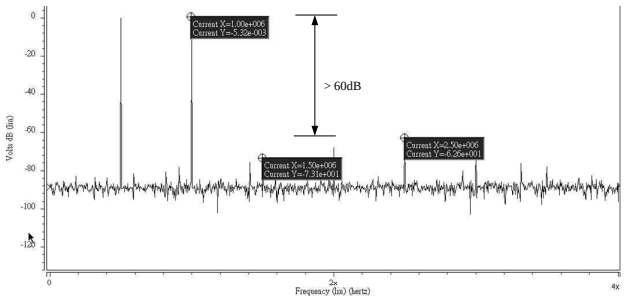
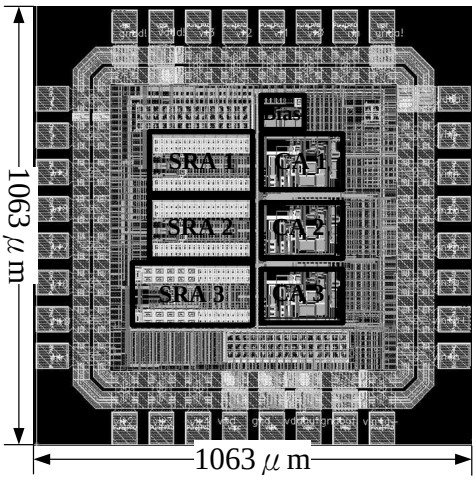


Figure 8. Simulation PGA's output two-tone spectrum at 1 Mhz; 500 kHz and 80 mV_{pp} output. The third order intermodulation is less the 60 dB.

the electronic noise source, and another is generated by the circuit nonlinearity which is also called interference noise. Some examples of inherent noise are thermal, shot, and flicker noise. While total harmonic distortion is often used to describe nonlinearities of analog circuits, it is also popular to define third harmonic as the measures of nonlinear behavior. The main PGA circuit is the key component of the distortion source, but the resistors and the output buffers which connect two stages are also important. It is not allowed in spite of one of them does not match the specification. The third-order intermodulation simulation of fundamental circuit is shown Fig. 8. It may be a more appropriate parameter to verify the workability of an communication integrated circuit since the signal is averagely spread on the frequency spectrum in a multi-carrier system.

4 Simulation Result

The analog forward path of AGC is fabricated in a TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.18 μm 1$P6m$ CMOS process through the CIC advanced service; Fig. 9. shows the chip layout where all the I/O pads are protected by the ESD circuit which is provided by ITRI. Active silicon area for the analog circuit was about 0.25 mm. Fig. 10. shows the AGC output waveform when the input level is 0.22 mV_{pp}. As expected, the output magnitudes are maintained at a constant level of 1 V_{pp}, and the converge speed is about 14 symbol periods. Using 20 Mhz ADC sampling rate, it needs one more symbol periods (one symbol period plus cyclic prefix) as the integrated and dump to make sure that it has the invariable gain in one symbol. The minimum voltage input needs the longest settling time and the critical converge speed is 14 symbol periods. It still can make the digital circuit work ordinarily. The four-corner ($FF/0^oC$, FS, SF and $SS/80^oC$ transistors model) post-layout simulations of bandwidth and the maximum gain are revealed in Fig. 11. Table 3 shows the simulation performance of PGA. The proposed design preserves the high linearity and high dynamic gain range with fast settling time.



CA -- Current Amplifier
SRA – Switch Resistors Array

Figure 9. Layout of Programmable-Gain Amplifier

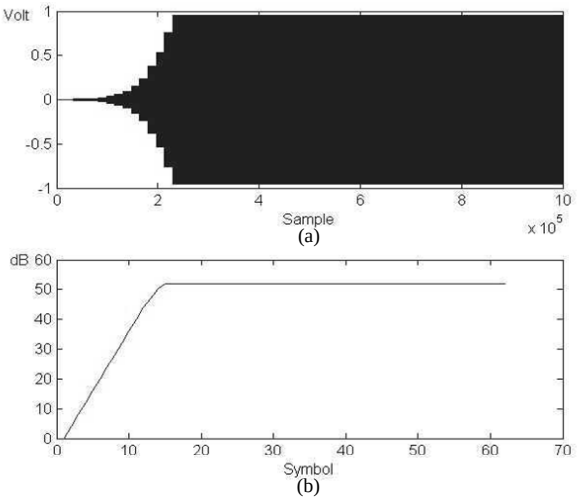


Figure 10. AGC close-loop simulation with settling time using Matlab

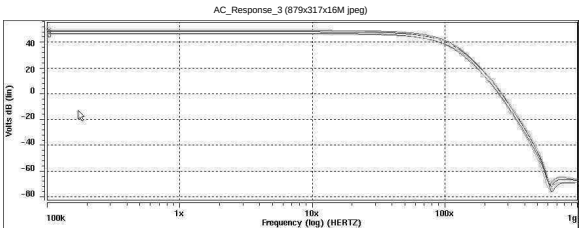


Figure 11. AC Response of four corner simulation in HSPICE

5 Conclusion

An automatic gain control system with programmable gain amplifier system has been designed and fabricated in 0.18 $-$ μm CMOS process. Besides, the overall system has been simulated in Matlab with the relative analog PGA mathematical model. There is a small gain error and almost fixity gain jitter due to the digital feedback design. The post-simulation results show the $-66dB$ third-

Table 3. Programmable Gain Amplifier Performance Summary

Specification	Post-Simulation
Technology	TSMC 0.18 μm 1P6M
Gain control range	0~49 dB
Gain step	Coarse : 6 dB
	Fine: 1 dB
Total harmonic distortion	0.043%
Input referred noise ($v/\sqrt{Hz}$)	1.5 μ @ min gain
	80 n @ max gain
Chip area	1.063×1.063 μm^2
Power consumption	13 mW
Supply voltage	1.8 V

harmonic distortion and $85n(\frac{v}{\sqrt{Hz}})$ with 49 gain dynamic range.

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