Silicon Area Efficient Design of RF Tuner for Digital Television Receiver

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Abstract: - In this study, a single-chip is designed with MOS techniques for the digital TV tuner. The chip consists of the modules of low noise amplifier (LNA) , RF mixer, digital voltage control oscillator, and polyphase filter. The tuner is designed with the structure of a single conversion by mixing the Quadrature local signal with polyphase filter. The frequency band is designed from 530 MHz to 602 MHz for DTV channels in Taiwan. The gain of the entire tuner can be over 32 dBm, and the image rejection ratio (IRR) of the tuner is above 30 dBm. The local oscillator built-in digital-to-analog converter can be directly controlled by a digital code to select the TV channel. The silicon chip had been designed with a full-custom layout, where the chip size and core size is about 0.497 and 0.1095 mm^2, respectively, when implemented by TSMC 0.18μm CMOS process. The maximum power dissipation is about 136.7 *mW* when the chip works 3.3V.

Key-Words: - DTV, polyphase, active filter, mixing, tuner, polyphase filter and LNA.

1. Introduction

A wireless RF communication systems had widely used for portable devices, such as cell-phone, TV receiver, and GPS and so on. For the portable device, the chip size and power dissipation is as small as possible [1-3]. The digital TV had been popular because of high quality and low noise. For TV broadcasting, the tuner is required to select the TV channel from the RF signal modulation [4-11]. The main function of a tuner is to transform RF signal to IF (intermediate frequency) one for TV receiver. The tuner architectures can be split to the single conversion and dual conversion with zero IF, low IF and IF [9-11]. The single conversion requires a tracking filter that employs high Q inductance, which is hardly implemented in a silicon chip. The double conversion method is widely used to reject the image frequency for the cable TV systems [11]. The architecture is shown in Fig. 1(a). The first is an up-conversion that modulates the video signal to the high frequency band. The frequency of the first local oscillator is 1220~2080MHz, and the TV band is from 48~860MHz. One can select the IF from the differential of mixing of local oscillator and TV signal. Due to harmonic frequency, the image signal would appeas on spectrum. The first IF is 1220MHz that is away from the band of TV program channel to reduce the interference with the image signal. The SAW filter is used to select the IF from a mixer. The second stage is a down-conversion that IF is about 30~60MHz from the second SAW filter. The SAW filter is always implemented with off-chip because of the difficulty on MOS process. Recently, the image rejection by a ployphase filter becomes popular since it can be implemented on MOS chip as working on low IF or zero IF [7-8]. However, the zero IF is not easy to design due to the problem of DC offset and flicker noise. The architecture with the ployphase filter operated on low IF is suggested, as shown in Fig. 1(b). This architecture requires the mixers to generate four phase signals.

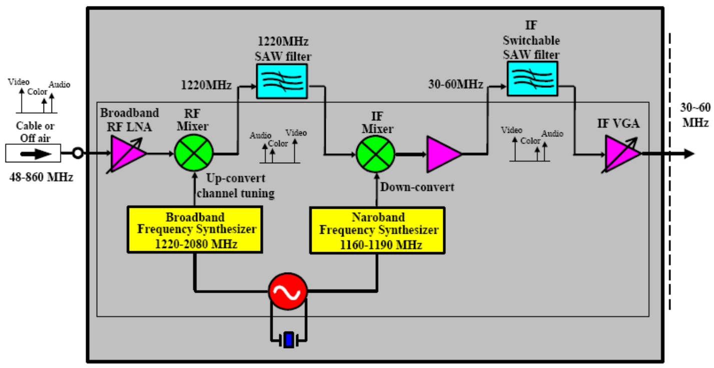

Fig. 1(a) The architecture of dual conversion with IF.

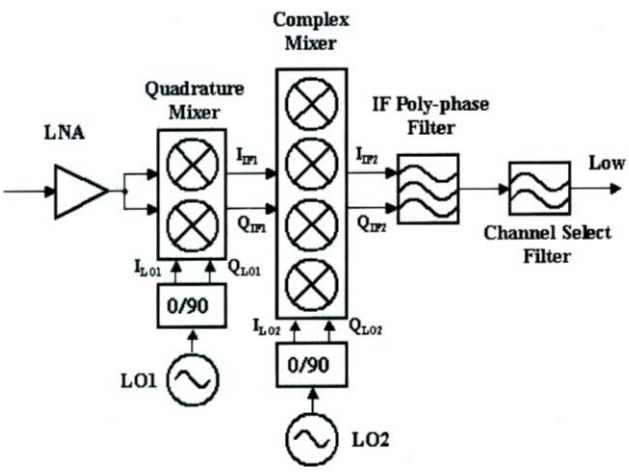

Fig. 1(b) The architecture of tuner with low IF polyphase filter.

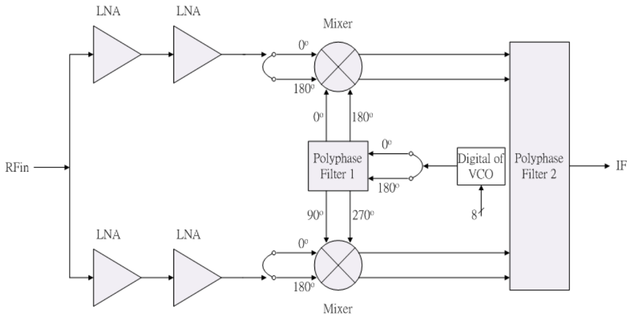

Figure 2 The architecture of the proposed DTV tuner.

TV tuner can be implemented with either discrete chip or single chip. The former can easily adjust the feature of tuner in various processes. However, the power consumption and tuner size is larger, which is not appreciated for a portable device. In order to improve the performance of tuner, a single silicon chip for tuner implementation is studied in recent [9-11]. In this paper, we design a silicon tuner with TSMC 0.18*um* process. First each sub-module, such as low noise amplifier (LNA), mixer, filter, and local oscillator, is implemented respectively. Then an entire tuner is combined with these sub-modules within a silicon chip. The cost-efficient chip is designed with small area and high gain for a low cost TV receiver.

2. Proposed Tuner Design

To achieve cost-efficient design, the proposed tuner adopts a single stage conversion for low-IF output. Figure 2 shows the architecture of proposed DTV tuner. The two-step LNA is used to amplify the weak signal from an antenna. The LNA chip is designed by referring to [6] with active inductor to reduce the core size. For the single stage conversion, the local oscillator employs Quadrature Local Oscillation (QLO) [7]. For QLO signals, the ployphase filter 1 is used to generate 0, 90, 180, 270 degree signals, which are generated with a simple RC circuit with one stage [7]. Then the QLO signals are sent to the mixers to generate the four-phased IF signals. The QLO signal frequency can be controlled by the digital code from a local oscillator. The four phased IF signals are further filtered by the ployphase filter 2. The main purpose of the ployphase filter 2 is : (1) can filter the selected low IF frequency from the differential signal to the output; (2) reduce the image signal level. The module of the ployphase filter 2 is designed with four stages, where the detail is shown in our previous paper [8].

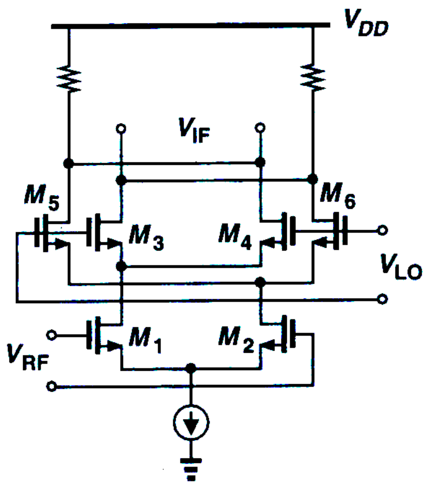

Fig. 3 The active mixer.

The mixer is designed with active two-balance structure [2], as shown in Fig. 3. If RF input signal and local signal is $V_1=A_1Cos(w_1t)$ and $V_0=A_0Cos(w_0t)$ respectively, after mixing, we can achieve

$$2A_1A_0\cos(\omega_1 t)\cos(\omega_0 t) = A_1A_0\left[\cos(\omega_1+\omega_0)t+\cos(\omega_1-\omega_0)t\right] \quad (1)$$

Besides the basic frequency, the additive and differential frequencies generated can be applied to up conversion and down conversion for RF signal.

The mixer can feed two-phased RF signals, and two-phased local frequencies. With two mixers, one can achieve four phased signals. Each mixer can output two basic signals, one differential signal and one additive signals. Then the polyphase filter is used to catch the differential signal to find IF signal.

The local oscillator is designed with a digital-based voltage control oscillator (VCO). The digital VCO consists of the digital to analog conversion and the five-stage ringing oscillator, as shown in Fig. 4. The input digital code with 8 bit can directly control the frequency

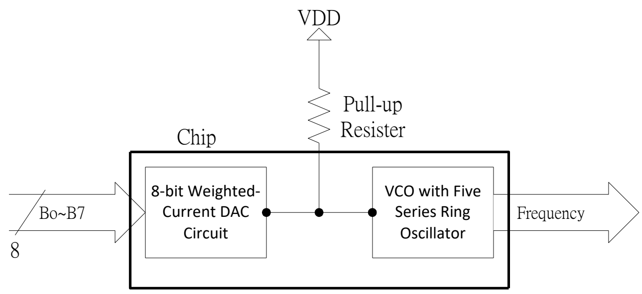

Fig. 4 The digital-based voltage control oscillation.

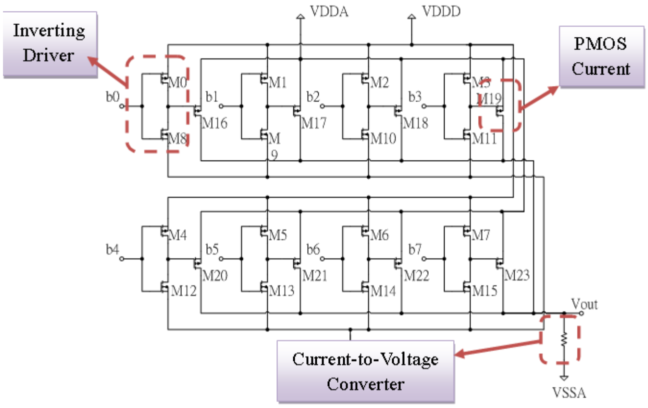

Fig. 5 The weight digital to analog conversion.

from 500 to 600 MHz for DTV band in Taiwan. The pull-up resister is used to promote the voltage of DAC output to overcome the threshold of VCO to improve the linearity between voltage and frequency. The VCO is designed with five-stage inverters ringing [12]. A low pass filter is employed at the end of VCO, to smooth the harmonic of ringing oscillator. However, the frequency of VCO may be deviated in process changed. The digital correction with micro-processor can be employed to calibrate the deviation to meet the current DTV band. The digital local oscillator can directly select the TV channel with micro processor control.

The digital to analog conversion (DAC) is designed with by the current mode, as shown in Fig 5. P-MOS devices, M16 to M23, are employed to control the current switching. The PMOS driving current is dependent on channel width (W) and length (L), which can be expressed by

$$I_d = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{gs} - V_{thp})^2. \quad (2)$$

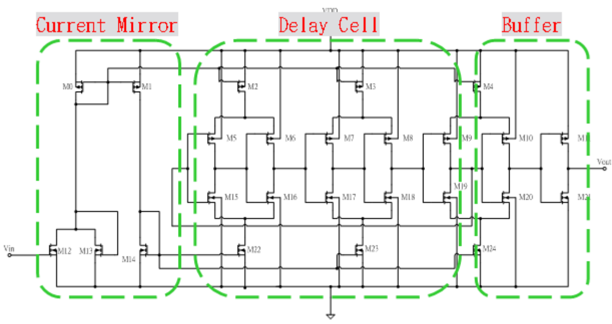

Fig. 6 The five stages inverter oscillator.

The PMOS M16 is LSB, and M23 is MSB. Since PMOS switch turns on when its gate is low, the inverter is used for positive logical control. Also, the inverter can isolate the digital circuit from the analog current to reduce the digital noise. The ration of W/L in each bit is designed to generate 2^n-degree weighting. We have Iref, 2 Iref, 4Iref…256Iref from LSB bit, 2nd LSB, 3rd LSB, to MSB, where Iref is basic reference current. All PMOS devices are in parallel, and the resistor is employed to transform the current to voltage by Vout=I_{DAC}×R, where I_{DAC} is the total output current from DAC, which can be given by

$$I_{DAC} = S_0\, I_{ref} + S_1\, 2I_{ref} + S_2\, 4I_{ref} + ..S_7\, 256I_{ref}\,. \quad (3)$$

where S_0 to S_7 is the PMOS switch from LSB to MSB.

The five stage ringing local oscillator is shown in Fig. 6 [12]. The input stage is a current mirror, which the input voltage can control the bias to change the current. The second stage is five ringing inverters. The current mirror can control the capacitance charging time for each inverter to change the delay. As the current is high, the charging time becomes short and the frequency increases accordingly. The last stage is buffer, which can provide driving power and avoid the loading effect for VCO.

3. Chip Implementation and Comparisons

Based on the proposed circuit in Fig. 2, the tuner chip is realized with TSMC 0.18*um* 1P6M process. First, we individually implement the modules of LNA, mixer, DAC, oscillator and ployphase filter. Then the entire tuner consists of these modules. With Agilent Advanced Design System (ADS) tool simulations, the results of DAC and VCO are shown in upper and bottom of Fig. 7 respectively. The linearity of DAC is checked by a 8-bit binary counter, where the output voltage is from 0 to 1.6v as the counter from 0 to 255. The VCO output may be not good linearity when the input is at the low and high voltage. In the linearity region, the VCO can generate 530MHz to 680MHz corresponding to the input voltage from 0.75v to 2.5v. To overcome the MOS offset, the pull resistor used in Fig. 4 can increase about 0.75v offset voltage.

Table 1 Chip Features of the Proposed Tuner

Receiving Frequency	530 to 602 MHz
PDC/Power Supply	136.692 mW/1.8 & 3.3 V
Process	TSMC 18μm 1P6M
Core Area	300 * 365 um²
Chip Area with PAD	705 * 705 um²
Gain	32 to 37 dBm
IRR	30 to 103 dBm

The parameters of MOS width/length and resistor are extracted from the results of ADS simulator. The chip layout with the full-custom methodology is according to the MOS parameter. The chip has been verified with LVS and DRC tools in success. Table 1 lists the chip features.

The chip can be worked under 1.8V or 3.3V , and the average power dissipation is about 137mW as estimating from Powermill tools. When the operation frequency is from 530 to 602 MHz, the gain can be over 32dBm.

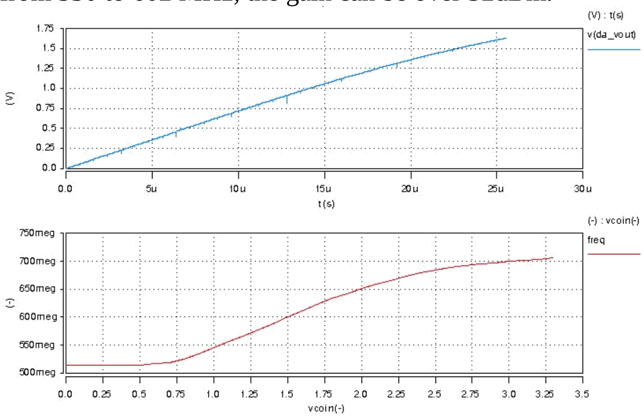

Fig. 7 The simulated results of DAC and VCO.

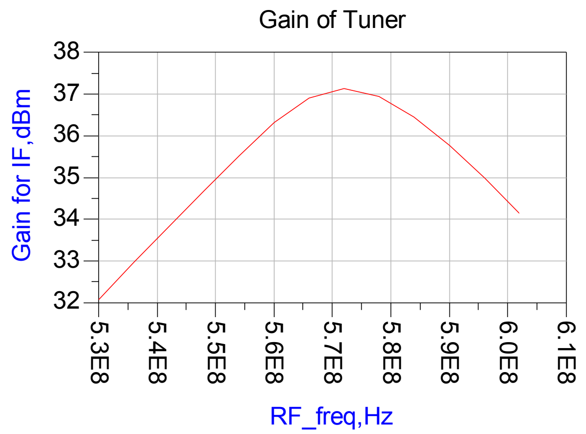

Fig. 8 The frequency response of the proposed tuner.

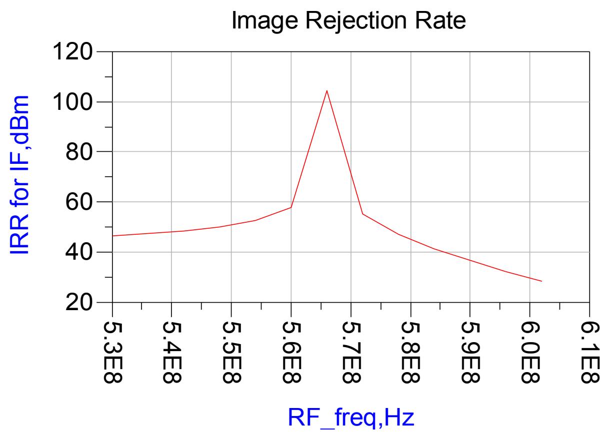

Fig. 9 The image rejection response using proposed tuner

Figure 8 shows the gain of the tuner, where the chip can gain about 35dB in average. Figure 9 shows the image rejection power, where the maximum rejection power at the central frequency can achieve about 103dBm, and the image frequency rejection is at least 30dBm among all bands. The image rejection ration (IRR) can achieve about 67dBm in average. The operation band is designed from 530MHz to 602 MHz for the current DTV tuner in Taiwan. The photo for the chip layout is shown in Fig. 10, where the size is 705 * 705 um^2 as included I/O pad.

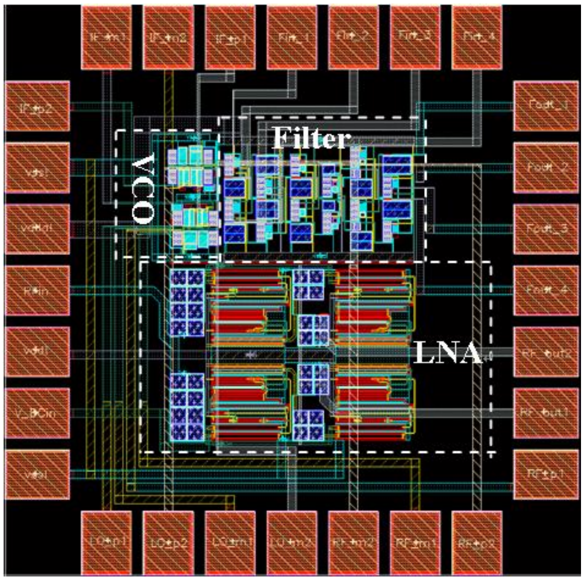

Fig. 10 Photomicrograph of the proposed tuner.

One can extract the parameters from the post layout to estimate the performance when encountering the process, supply and temperature spread. The tuner is designed by the relative ration of MOS. When the process occurs deviation, but the ration of MOS parameter can be always hold, and the chip feature can be almost kept. With ADS simulations, when the parameter of MOS changes 10%, the gain will degrade 0.8dB at the center frequency. As the power supply has ±10% spread, the chip also can work in normal, but the frequency will shift about 32MHz at maximum. The chip also can work under various temperatures during 0~80ºC. However, the center frequency may shift about 1.5MHz, when the temperature changes ±10ºC.

Now we evaluate the performance for the proposed tuner with some parameters. (1) The **group delay** is about 0.4~0.6 ns in the DTV band, as shown in Fig. 11. (2) The **stability of filters** operates at entire frequency range, as shown in Fig. 12. These values in operated band all can be over 1, which denote that the tuner can work stably. (3) The **dynamic Range** is

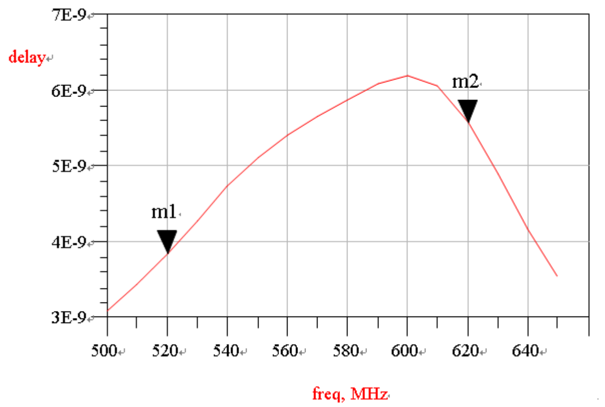

Fig. 11 The group delay of the proposed tuner.

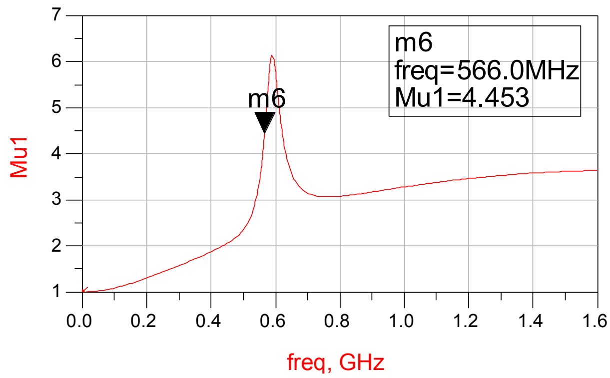

Fig. 12 The stability of filters from IF output ports.

Table 2 Comparisons of Tuner Chips.

	[9]	[10]	[11]	Proposed
Chip Process	0.13μm	0.13μm	0.18μm	0.18μm
Architecture	Single Conv. Low IF	Single Conv. Low IF	Dual Conv. Low IF	Single Conv. Low IF
VOC	Analog	Digital	Analog	Digital
TV Standard	Hybird	DBS	Cable	DVB
RF Gain	45dB	45dB	26dB	35dB
IRR	65dB	55dB	36dB	67dB
Power Consumption	1.2W/3.3v	0.7W/3.3V&1.8V	410mW/3.3V	136.6mW/3.3v&1.8V
Area	3 mm^2	8.6 mm^2	2.6 mm^2	0.497mm^2

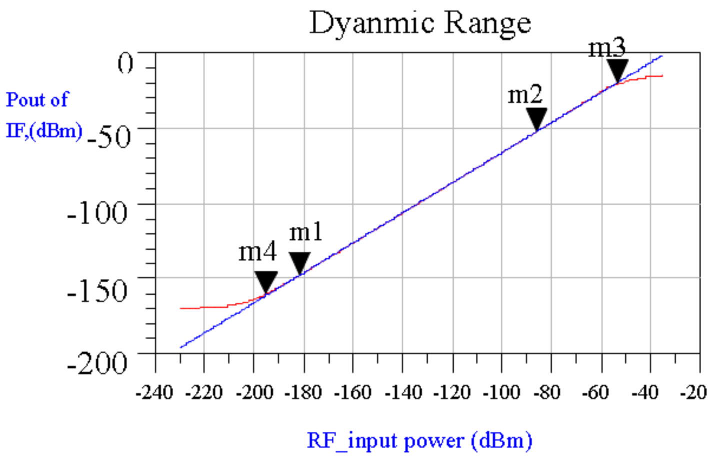

Fig. 13 The dynamic range(RD) of the proposed tuner.

measured at IF 36.2 MHz when input power is from -190 dBm to -55 dBm. The dynamic range of proposed tuner is about 135 dBm, as shown in Fig. 13. (4) The **linearity** of filter between input and output is shown in Fig. 14. The points m3 is located at 1dBm gain compression, where the output becomes non-linearity when input power is over –55dBm.

Table 2 lists the comparisons with the competing chips. A. Maxim el at. [9] presented a hybrid tuner for ATSC/DVB-T digital terrestrial TV standards with ployphase filter. However, the chip consumes about 1.2W power, which is not suitable for mobile TV device. A DBS satellite tuner [10] is presented with the single conversion. A ring oscillator-based frequency synthesizer is designed, which the local oscillation frequency can be controlled by the digital circuit. However, its chip area is 8.6mm^2 that is too large for most of low-cost TV receivers. R. Montemayor [11] presented a dual-conversion tuner IC for cable TV. Its power dissipation and chip area is clearly lower than [9] and [10].

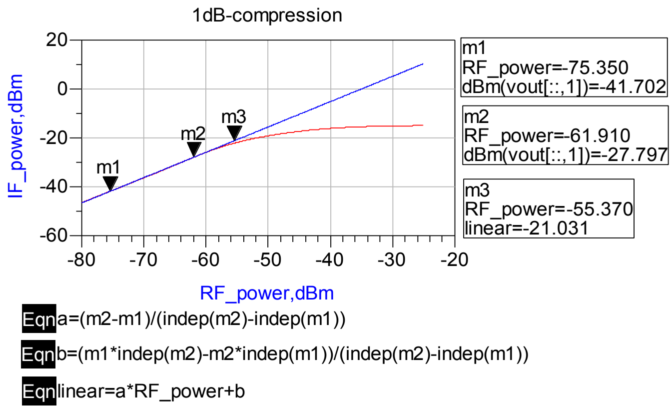

Fig. 14 The linearity evaluation for the proposed filter.

However, the down conversion is designed with trifilar transformer that is not easily implemented in CMOS chip. We proposed a cost-effective tuner chip for DTV with DVB standard. The chip is designed with the single conversion based on ployphase filter. The power dissipation can be reduced by 88%, 51%, 30% compared with [9], [10] and [11] respectively. Also, the silicon area is only about 16%, 5.8% and 19% that of [9], [10] and [11] respectively. Clearly, the proposed tuner is not only to achieve low power but also to keep low cost, which can be applied on mobile TV system. Besides, the digital circuit, such as extra micro-processor, can directly control the VCO to select the TV channel.

4. Conclusions

This paper presented a low-cost tuner module for DTV. The chip is successfully implemented with TSMC 0.18*um* process. Comparisons with the existed tuner chips, there are many advantages using this approach. (1) The silicon area can be greatly reduced on-chip. (2) The power dissipation can be much reduced. (3) The chip can be directly controlled by the digital circuit. (4) The chip without using any inductor is easily implemented in silicon chip. When polyphase filter combined with a mixer, the image frequency can be rejected about 67dBm in average for DTV tuner band. With area cost-effective design, the chip size is only 0.49 mm^2 (included I/O pad) and its core size is only 0.11 mm^2 with TSMC 0.18*um*. With low power and small area, this tuner chip can be embedded to the set-top-box for the DTV system.

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