Design of a Class-D Audio Amplifier With Analog Volume Control for Mobile Applications

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Abstract: - A class-D audio amplifier with analog volume control (AVC) section and driver section for wireless and portable applications is proposed in this paper. The analog volume control section, including an integrator, an analog MUX, and a programmable gain amplifier (PGA) is implemented with three analog inputs (Audio, Voice, FM). For driver section, including a ramp generator, a comparator, a level shifter and a gate driver is designed to obtain a low distortion and a high efficiency. Designed with 0.18 um 1P6M CMOS technology, the class-D audio amplifier with analog volume control achieves a total root-mean-square (RMS) output power of 0.5W, a total harmonic distortion plus noise (THD+N) at the 8-Ω load less than 0.06%, and a power efficiency of 89.9% with a total area of 1.74 mm2.

Key-Words: - *Class-D,* Analog volume control, Pulse width modulation, Ramp generator.

1 Introduction

Small size, low-cost and high-efficiency class-D audio amplifiers are in widespread demand for mobile applications. Conventional linear amplifiers feature low-distortion performance but have several disadvantages versus market needs [1-2]. The main drawback using linear amplifiers is low efficiency. Low efficiency translates into more power dissipation inside the chip which uses a heat sink to dissipate the heat and also lowers the battery life. This increases the cost and the area of the audio solution.

To achieve similar low-distortion performance, higher power efficiency, and hence smaller size and cost, the recent research has been focused on class-D audio amplifiers [18-19]. However, the choice of the class-D audio amplifier with pulse-with modulation (PWM) architecture becomes critical for the better performances of a class-D audio amplifier.

A class-D amplifier is attractive because of the high power efficiency and low distortion by using (PWM) compared to a linear amplifier, which realizes a longer battery life and eliminates the heat sink requirement. This allows design of compact and low cost multi-channel high-power systems [3-6].

In a class-D amplifier, the audio signal is converted in to a high-frequency PWM signal whose pulse width varies with the amplitude of the audio signal. The varying-width pulses switch the output transistors of the class-D output stage at a fixed frequency. A low-pass filter (LPF) then converts the output pulses in to an amplified audio-signal that drives the speaker.

Most of the class-D reported in literature does not contain a module allowing the analog volume control for audio, voice and FM [20-21]. In this work we will propose an architecture of a Class-D audio amplifier with analog volume control for high efficiency and low THD. Moreover we will propose a new architecture of the ramp generator which uses 4 bits trim; 2 bits (LSB) to trim the ramp amplitude to vdd/5 peak-to-peak and 2 bits (MSB) to adjust the ramp continuity, the trimming procedures consists on putting a zero input signal, and adjust the trim code such as to get a 50% duty cycle PWM output signal and reduction of inter-modulation in case of mixing of audio and voice.

The proposed Class-D audio amplifier shown in Fig.1 consists of an analog volume control section and a driver section. The AVC section is composed of an integrator, an analog MUX, and a programmable gain amplifier (PGA). The driver section is composed of a ramp generator, a comparator, a level shifter and a gate driver targeted for portable applications. The Class-D is configured

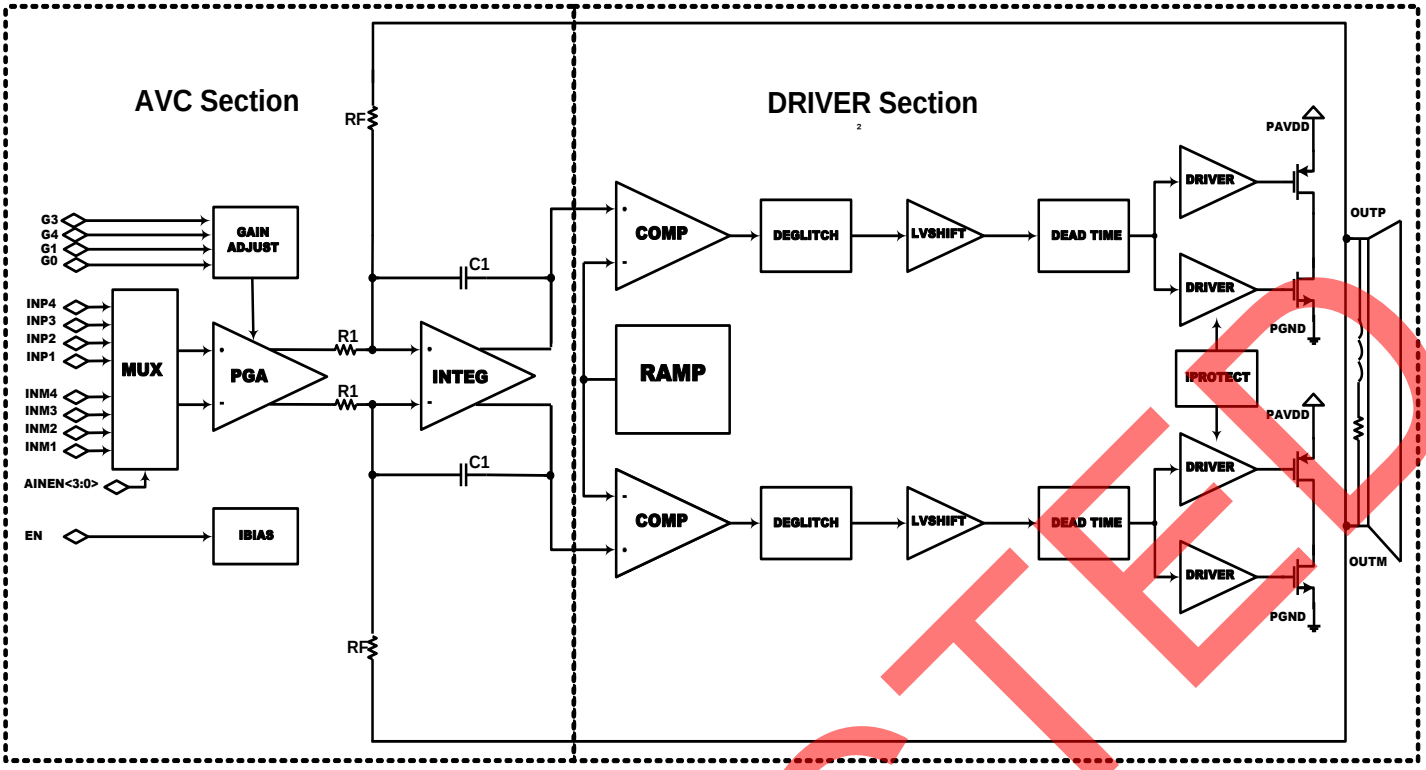

Fig.1 Block diagram of Class-D with AVC

to drive a bridge-tied load (BTL) capable up delivering 0.5W of average power into a 8 Ω load at <1.0% THD+N from a nominal 3.6 V power supply at an audio frequency of 1kHz, while switching the output bridge at a frequencies of 320kHz, 294kHz, 320kHz for the audio and 333.33KHz for the voice. Shutdown for the Class-D is active low. Maximum recommended power supply for operation is 5.0V with a 5.5V absolute maximum supply voltage. The input resistance will be fixed to 200KΩ. Unlike traditional implementations utilizing binary modulation, the modulation scheme of the Class-D allows for direct drive of a speaker in close proximity of the IC without the use of an output low-pass filter, while still maintaining a low quiescent current draw. However, it is expected in applications where the speaker is not located close to the amplifier that an output filter of some type will be used. In any case, the modulation allows for higher efficiency when compared to the traditional binary method. Quiescent current operation of the device while driving the load with no audio input signal will be targeted 6.0 mA maximum. A short circuit protection and limitation is implemented to increase device reliability.

The organization of this paper is as follows. Section 2 presents the design of the AVC, while Section 3 addresses the design of driver section. The measurement results are shown in Section 4, and conclusions are given in Section 5.

2 AVC Circuit Design

The analog volume control is proposed to provide the flexibility of having different amplifier gain settings. The main block of the analog volume control is programmable gain amplifier (PGA).

2.1 Programmable Gain Amplifier (PGA)

The proposed programmable gain amplifier is based on the conceptual scheme shown in Fig.2. It is a high-gain amplifier with resistor network feedback. The gain varies by changing the ratios of resistors R12/R11. If the gain of the operational is not high enough, the variation of the feedback factor results in variation of the bandwidth and hence increases the total harmonic distortion (THD) [7]. For cost-effective applications, the target of this programmable gain amplifier for audio and voice volume control is making possible to amplify the input signal from 0 to -24dB in steps of -3 dB.

The transfer function of PGA can be expressed as:

$$F = \frac{VOUTP - VOUTM}{VINP - VINM} = \frac{R_{12}/R_{11}}{1+jR_{12}Cw} \quad (1)$$

With $R_{11} = R_1 + R_2 + R_3 + R_4 + R_5$ and $R_{11} = R_6 + R_7 + R_8 + R_9 + R_{10}$

The gain and cutoff frequency of the PGA can be expressed as:

$$Gain(dB) = 20\log\left(\frac{R_{12}}{R_{11}}\right) \text{ and } F_c(Hz) = \frac{1}{2\pi . R_{12} . C} \quad (2)$$

The value minimum of R11 is 200KΩ, thus the value of R12 is 200KΩ for 0dB and 20K for -24dB and for mute the value of R12 is 0Ω. Fig.3. shows selectable gains of the PGA with the frequency.

The resistor-network are specified with an absolute gain error and relative gain error at the first setting, a total gain difference between the highest and lowest setting, and the gain step size from each gain setting to the next as shown in Fig. 5.

The matching of the PGA resistor is critical because portion of PSR and CMRR is due to mismatch of resistor.

$$1/sqrt(W * L) \sim 12.2m \rightarrow MM(1\sigma) < 0.025$$

The detailed architecture of PGA implementation is shown in Fig.4. The architecture including resistance network and High amplifier. For the PGA resistors network the switches of decoder at not placed at input side, such as to optimize the THD of the class-D amplifier.

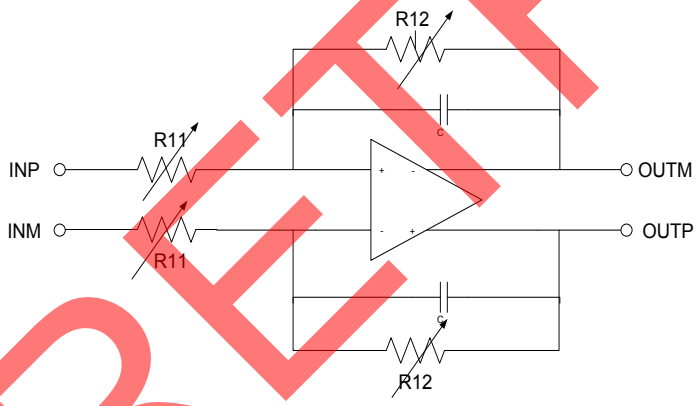

Fig.2.The proposed programmable gain amplifier

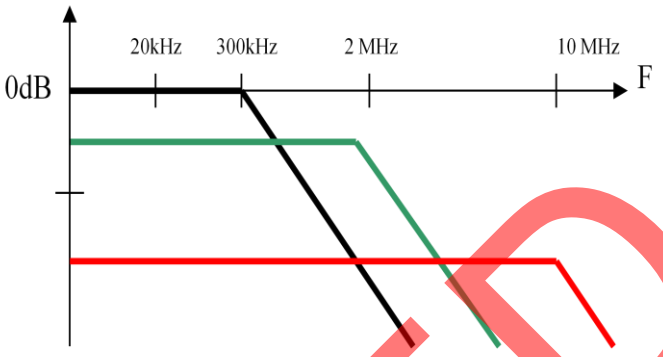

Fig.3. Gain of the PGA

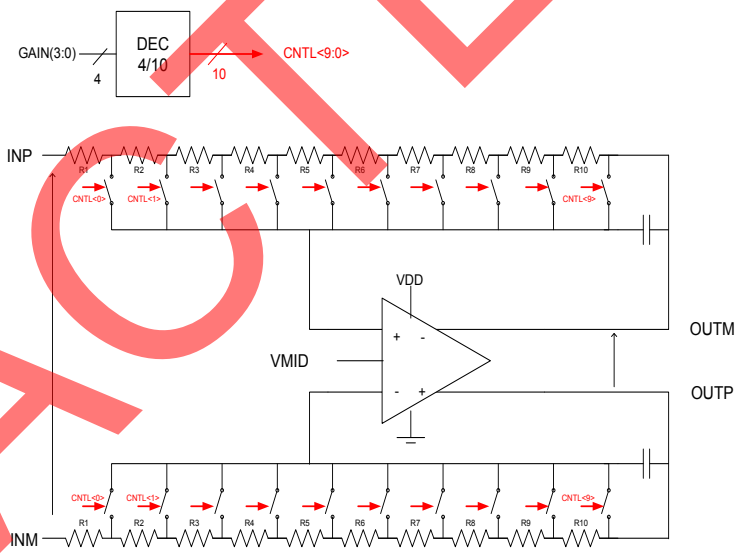

Fig.4. Detailed architecture of PGA

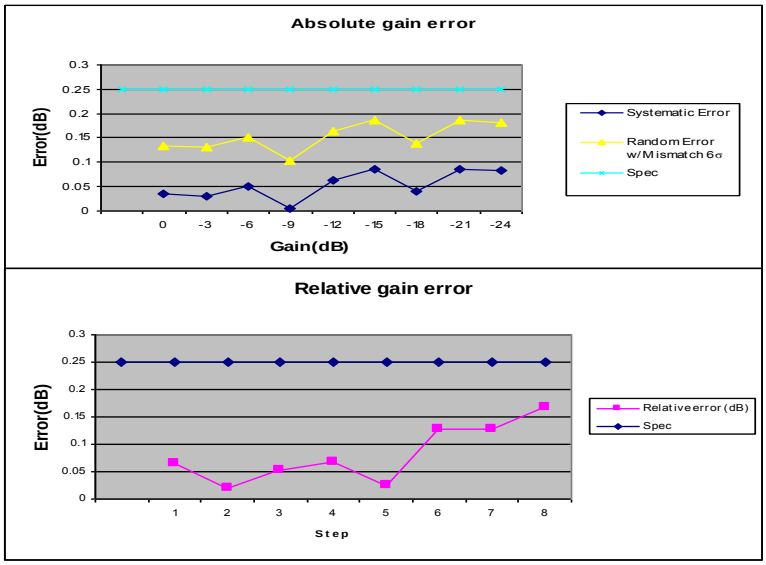

Fig.5. Absolute and Relative gain error of the PGA

2.2 Differential amplifier Circuit

The PGA using an amplifier with low input impedance and resistor-network feedback to achieve high linearity and wide bandwidth simultaneously. The differential amplifier for PGA is shown in Fig.6 with common mode loop feedback and use PMOS input diff-pair for low noise, the integrator amplifier provides feedback control for the class-D output stage.

The transfer function of pre-amp can be expressed as:

$$A = \frac{A_{v1} * A_{V2}\left[1 - s.C_c\left(\frac{1}{g_{m6,9}} - R_c\right)\right]}{(1 + s.r_{o1} * A_{v2} * C_c)\left(1 + s.\frac{c_l}{g_{m6,9}}\right)} \quad (3)$$

With $A_{v1} = g_{m1} * r_{o1} * r_{o3}$ and $A_{v2} = g_{m6} * r_{o6} * r_{o6}$

Where gm1 and gm6 are the transconductance of the transistors M1, M6, and ro1, ro3, ro6, ro7 are output resistance of M1, M3, M6, M7. When the frequency is low, the pole created by Miller capacitor dominates.

Expression (3) could be reduced to

$$A \cong \frac{A_{v1} * A_{v2}}{(1 + s.r_{o1} * A_{v2} * c_c)} \quad (4)$$

The Integrator performs error cancellation between the incoming signal and the output signal of the class D, The crossover frequency (0dB) of the integrator will be designed between 60 KHz and 120 KHz.

The differential amplifier and integrator are identical in design and layout.

The AVC's main performances are summarized in Table 1, it consumes less than 0.1uW from 1.8V supply. The gain increases linearly from 0dB to -24dB, as shown Fig.7, which reproduces the frequency responses for the main gain settings.

The AVC features a mute control input pin. When this input is pulled to ground, the power amplifier internally disconnects the input signal. The INP and INM input pins sets the gain of AVC. The gains listed in table 1 are achieved by changing the taps on the input resistor inside the amplifier.

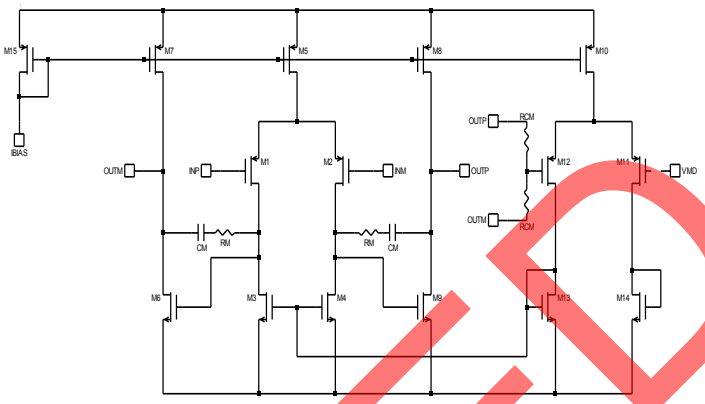

Fig.6. The schematic of differential amplifier

Tableau1 Summary of PGA performances

Parameters	Comments	Value
Supply voltage		1.8V
Gain	VOCTL =0000	0 dB
	VOCTL =0001	-3 dB
	VOCTL =0010	-6 dB
	VOCTL =0011	-9 dB
	VOCTL =0100	-12 dB
	VOCTL =0101	-15 dB
	VOCTL =0110	-18 dB
	VOCTL =0111	-21 dB
	VOCTL =1000	-24 dB
Gain Mute	VOCTL =1001	-104dB
Absolute Gain Error	0 dB Gain	0.15dB
Relative Gain Step Error	0 dB down to -24	0.18dB
THD, 1 kHz		118dB
Bandwidth -3dB	VOCTL=1000,24dB	2MHz
Power consumption	Vin=0.5Vinpp*sin(2pi*1kHz)	0.1uW

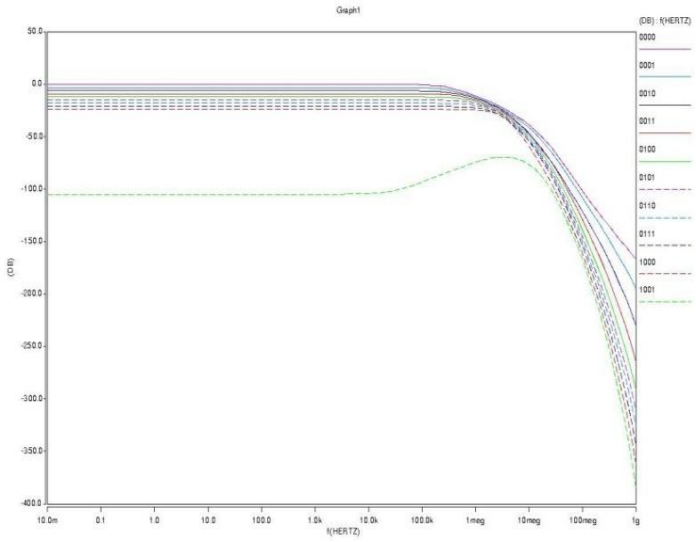

Fig.7. PGA frequency response

3 Driver section design

The driver section illustrated in Fig.1 consists of a ramp generator, a comparator, a level shifter, a gate driver and a power FET's.

3.1 Ramp generator

Figure 8 shows the circuit implementation of the proposed ramp generator which is generated by constant charging current into the capacitors C1 and C2, which is connected between the ground and successively cascode current source and cascode current sink.

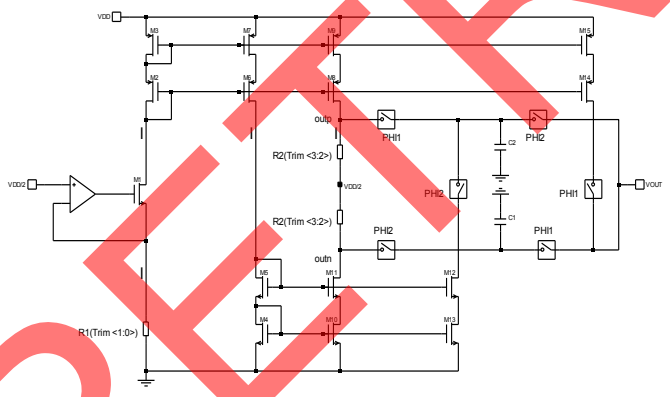

Fig.8. Ramp Generator Schematic

The basic operation of the ramp generator is based on charging and discharging capacitors with constant current. The switching mode of ramp generator is synchronized to system clock. The class-D will works at different frequencies that depend on the modes and the DAC Clock. The input clock frequency Range of the ramp is: 250 kHz – 550 kHz. The trimming procedures of the ramp generator consists on putting a zero input signal, and adjust the trim code such as to get a 50% duty cycle PWM output signal. We use fourth trim; trim<1:0> to trim the ramp amplitude to vdd/5 peak-to-peak and trim<3:2> to adjust the ramp continuity.

The current through R1 is the charging current, kept constant by forcing the voltage across R1 to equal VDD/2 by op amp, configured as follower voltage. The ramp slope is:

$$\frac{dV_{ramp}}{dt} = \pm\frac{VDD}{2R1*C} \qquad (5)$$

The resistance R1 is adjusted by tow digital bits Trim<1:0> for adjust finally the current charging, the ramp slope and Vramp peak-to-peak to equal Vdd/5.

The charge make in two phases PHI1 and PHI2:

a) In the phase PHI1 ,the switches PHI2 will be open and the switches PHI1 will be closed, the capacitor C1 will be in charge by constant current and the ramp output is the charge voltage of C1, thus Vout will be :

$$Vout(t) = \frac{VDD}{2R1*C}t + (\frac{VDD}{2} - R2*I) \qquad (6)$$

At the same time the capacitor C2 is in pre-charge state.

$$V_{c2}(t) = \left(\frac{VDD}{2} + R2*I\right)\left(1 - e^{-\frac{t}{R2*C}}\right) \qquad (7)$$

b) In the phase PHI2 , the switches PHI1 will be open and the switches PHI2 will closed ,the capacitor C2 will be in discharge by constant current, thus Vout will be

$$Vout(t) = -\frac{VDD}{2R1*C}t + \left(\frac{VDD}{2} + R2*I\right) \qquad (8)$$

In the same way the capacitor C1 is in RC discharge.

$$V_{c1}(t) = \left(\frac{VDD}{2} + R2*I\right)\left(2e^{-\frac{t}{R2*C}} - 1\right) \qquad (9)$$

As shown in Fig.9. The ramp output no continuity ($\Delta V \neq 0$), such as the resistor R2 is adjusted by tow digital bits trim<3:2> to adjust the value of outp and outn. The fist condition to get the continuity ($\Delta V=0$) of the ramp output is trim<3:2>=01, ie the value of R2=38.4KΩ as shown in Fig.10, The second condition to get ramp slope or ramp output peak-to-peak equal VDD/5 is trim<1:0>=10, ie the value of R1=55KΩ, and the third condition is that the half period T/2 will be large enough such that C2 voltage achieves 95% of its final value (ie $\frac{VDD}{2} + R2*I$), thus: $e^{(-\frac{T}{2R2*C})}$=0.05. So the minimum input clock period with the value of two capacitors is C1=C2=C=5pF.is

$$T_{min} = 2R2*C*\ln 20 = 2*2.99*R2*C =$$

1.725us. So the maximum input clock frequency Fmax = 580 kHz.

At top Class-D level, we can adjust the value of two resistors R1 and R2, by putting on both inputs (positive and negative) of the class-D a constant signal equal to VDD/2 (ie a zero differential input signal is going to the class-D). Then we adjust the value of Trim such as to have on both outputs of the class-D a square signal with duty cycle equal 50%.

The advantage of the ramp generator is the reduction of inter-modulation in case of mixing of audio and voice.

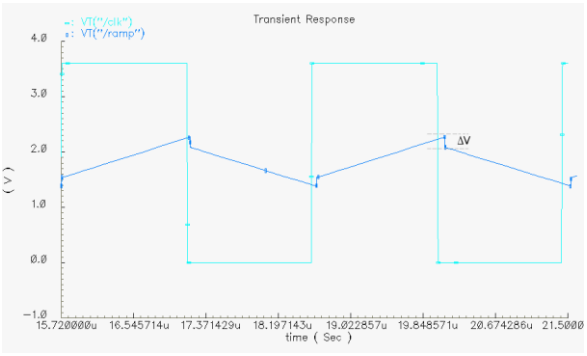

Fig.11: Ramp output before adjustment of Trim<3:3> (No continuity)

Fig.2: Ramp output after adjustment of Trim<3:2> (continuity)

3.2 Comparator circuit

Figure 11 shows the circuit implementation of the proposed comparator which is a rail-to-rail input circuit with constant Gm was designed to converts integrator output to PWM [16].

A simple rail-to-rail input can be easily constructed as a composite of P and N channel differential pairs, but this suffers from two drawbacks. First, at the extreme input range, only one input pair is active and so effective Gm is halved. Second, the large signal output current is also halved. Stabilization of the total Gm can be obtain by increasing the bias current in active differential pair by four, so that its Gm doubles when the other is inactive. Thus in normal operation each active differential pair have a current of I, that give a total current of 2I, when one differential pair is inactive (Gm=0), the other one have 4I and Gm double.

An enhanced input structure has been developed to achieve a constant current density at the output. At the input summer a total of current=2I is available whatever the common mode input level.

The current summation is a composite current mirror and current source. The current mirror is placed on n-channel side in order to increase speed.

For latch circuit, Two sources follower M0 and M1 provide a feedback path to the input node. When the current comparator output is somewhere between logic levels, there is not enough gate bias to turn on either of source followers, and the circuit has high input impedance. However, once there has been some excursion from the inverter's balance point, its gain produces a larger inverted output excursion, which quickly becomes large enough to turn either M0 or M1. Current is thus fed back to the transconductor output.

Consequently, the action of M0 and M1 is to provide an automatic clamp for the transconductor, maintaining the current summer devices in their normal active conditions. Fig. 12 shows the output and input signal versus time.

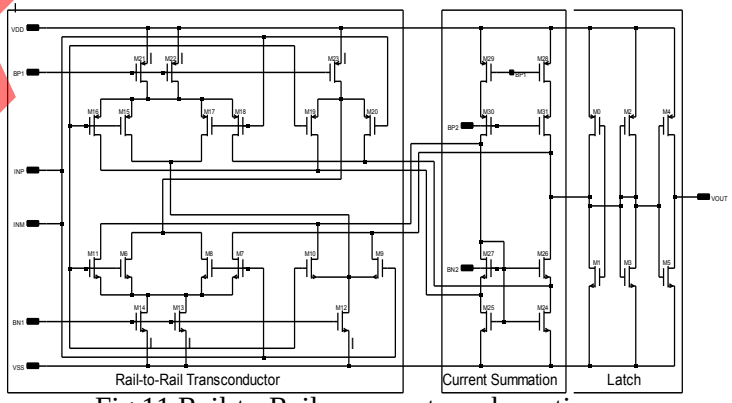

Fig.11.Rail-to-Rail comparator schematic

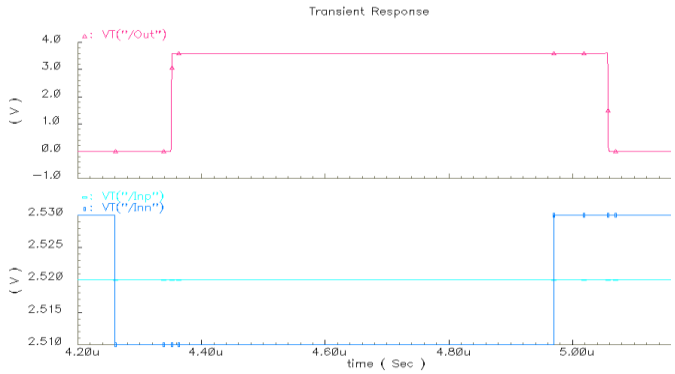

Fig.12. Input and output signals versus time

3.3 Level shifter circuit

Fig.13 shows the circuit implementation of the proposed Level shifter circuit which translates the low power PWM signal to the gate drive circuit. We have optimized the P/N ratio to improve the delay. Fig.14 shows the output and input signal versus time. The main performances are summarized in table 2.

Tableau 2 Summary of Level Shift performances

Parameter	Value
delay from in rising to out rising	0.8 ns
delay from in falling to out falling	2.1ns

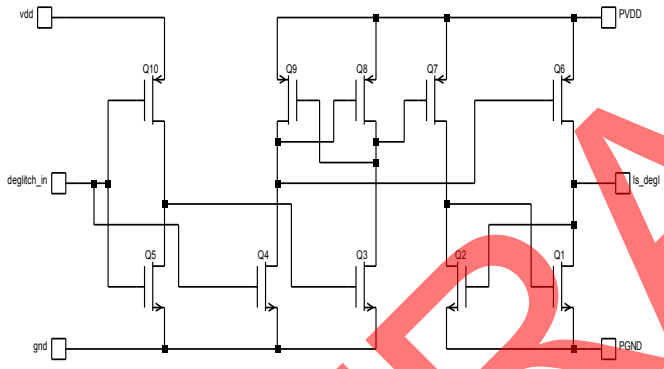

Fig.13. Level Shift Schematic

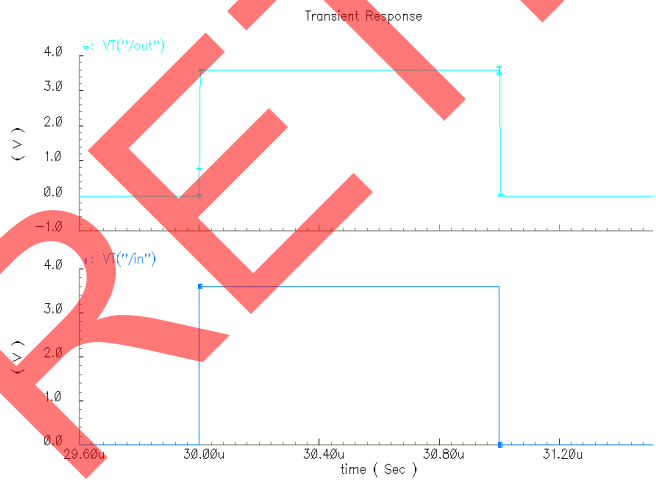

Fig.14. Input and Output signals versus time

3.4 Gate driver

The gate driver acts as buffer to drive the gate of each device to prevent loading by each of the switching device's parasitic capacitance. Fig.15 shows the circuit implementation of the proposed gate drive circuit and output Power FET's have been designed to limit the rise and fall times of the output switching and reduced EMI without increasing the propagation delay and dead time. Dead time is a source of distortion and an important design parameter in class-D audio amplifiers [8]. The dead time tradeoff between minimum dead time that allow to avoid any shot circuit between P/N MOS. The beak before make have to be implemented with the minimum dead time to allow better THD. The dead time control has been designed with new technique used which bases the turn on off one FET and inherent shoot-through limiting. Both PMOS and NMOS in the output stage are turned off during a dead time to prevent flow of cross conduction current directly from the supply to the ground, which degrades amplifier efficiency. Fig.16 and Fig.17 shows the turn-on time and dead-time when NMOS goes off and on, and PMOS goes on and off.

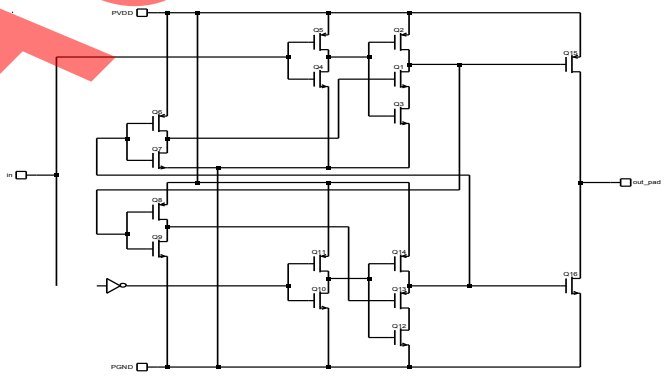

Fig.15. Gate drive conceptual circuit

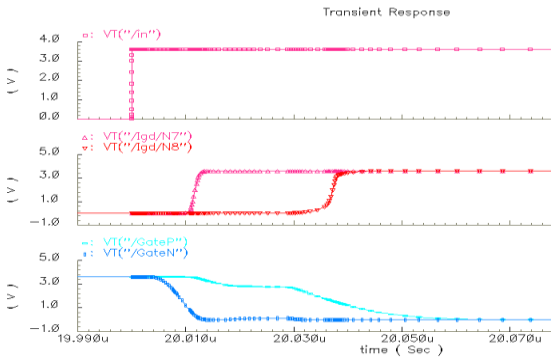

Fig.16. Turn-on Time and Dead-Time when NMOS goes off, and PMOS goes on

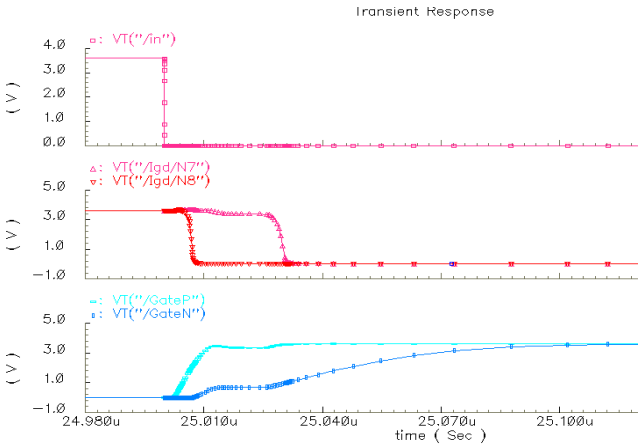

Fig.17. Turn-on Time and Dead-Time when PMOS goes off, and NMOS goes on

3.5 Output stage

Fig.18 shows the schematic of the H-bridge power stage. The PRMS is the root-mean-square power delivered to the load, Vp the peak output voltage (Vpp/2), and Ip the peak output current.

$$P_{RMS} = \frac{(\frac{Vp}{\sqrt{2}})^2}{R_L} \quad \text{so} \quad Vp = \sqrt{2.R_L.P_{RMS}} \qquad (10)$$

$$I_p = \frac{Vp}{R_L} = \sqrt{2.P_{RMS}/R_L} \qquad (11)$$

Making ideal assumptions, PWM duty cycle = 100%, MOS RDSon = 0 Ω, and RL=8Ω, PRMS=500mW.

Since the amplifier must deliver a peak-to-peak output voltage greater than the power supply voltage, the load has to be differentially driven, involving on H-bridge power stage architecture [17]. In order to evaluate in a fast way the size of this output stage, it's necessary to define the RDSon of MOS transistors to deliver the required output peak-to-peak voltage to the load. With the 0.18um technology, PMOS transistors have to be size 2.8 times greater than NMOS ones. With this ratio, the voltage drop across the N device is equal to the one across the P.

$$Vds_{on} \leq \frac{PVDD - \frac{Vp}{\eta}}{2}$$

With η =PWM duty cycle (12)

Assuming in first approach η = 94%

$Vds_{on} \approx 150mV$ since

$$Rds_{on} = \frac{Vds_{on}}{Ip} = \frac{1}{\frac{W}{L}.\mu_n.C_0.(Vgs - Vt)} \qquad \text{So } \frac{W}{L} \approx 11000$$

The main performances of the power stag are summarized in table3.

Tableau 3 Summary of power stage performances

Parameter	Value
Time rising – No Load	4.1ns
Time falling – No Load	3.2ns
Dead time – 8 Ω	2.3ns
Prop Delay – 8 Ω	4ns
RDSON – N	116 mΩ
RDSON – P	149 mΩ

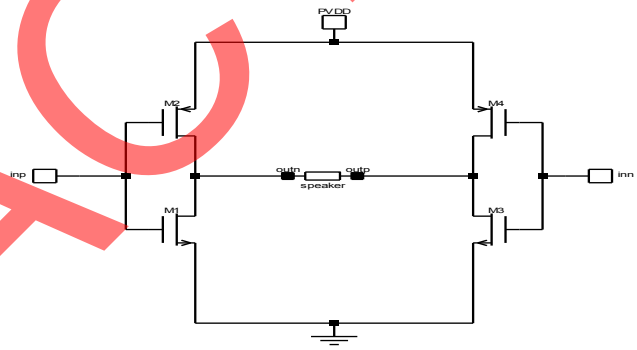

Fig.18. H-bridge architecture

4 Simulation results

The design of a class-d audio amplifier with analog volume control has been implemented in a 0.18 um single-poly, six-metal, CMOS process for mobile applications. The Layout is shown in Fig.19. The active area is about 1.74 mm2. The power stages can occupy about half the area. Fig.20 shows the THD+N versus output power into an 8Ω load at 2.5V, 3.6V and 5.5Vsupplies for Gain-12dB. The load for these measurements was Rspeaker = 8Ω, Lspeaker = 2*15uH and Cspeaker= 2*1nF as the speaker model and a 1-kHz test input signal was used in some measurements. The performance was quite good across a broad range of power delivered.

Fig.21 shows the measurement results for TSNR versus input level into an 8-Ω load at 2.5V, 3.6V and 5.5Vsupplies for Gain-12dB. Fig. 23 shows the power efficiency of amplifier versus varies the

output power at 1 kHz and obtains a power efficiency of 89.9%.

Two power supplies are considered, VDD/GND supply the circuit whereas PVDD/PGND supply the power stage. VDD/GND supply the circuit between the input signal to the gate drive sub circuit. Several simulations have been carried out over the temperature range, and its influence can be neglected. The consumption with no Load of the analog part is independent of the load but dependent on the power supply as shown Fig. 22.

A comparison between the proposed class-D amplifier and other state-of- the art amplifier is summarized in Table 5.

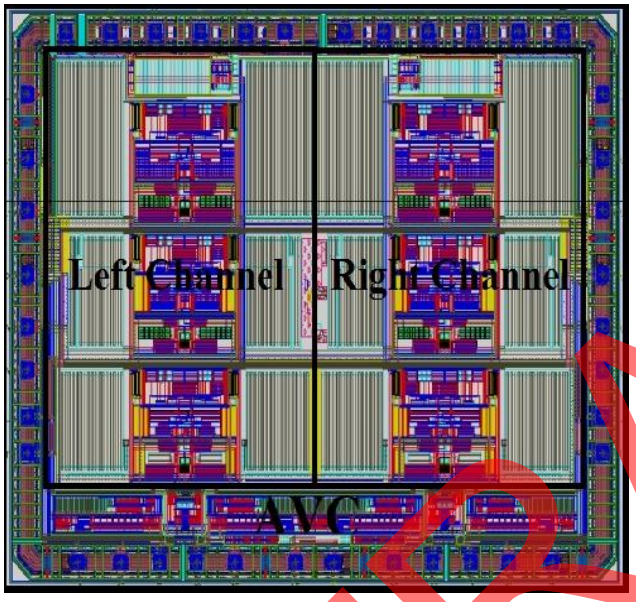

Fig.19. Class-D Layout

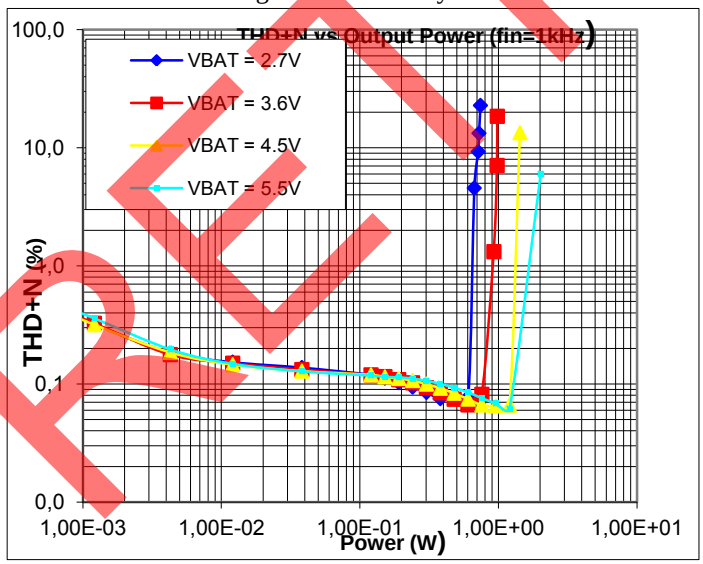

Fig.20.THD+N versus output power with Gain-12dB

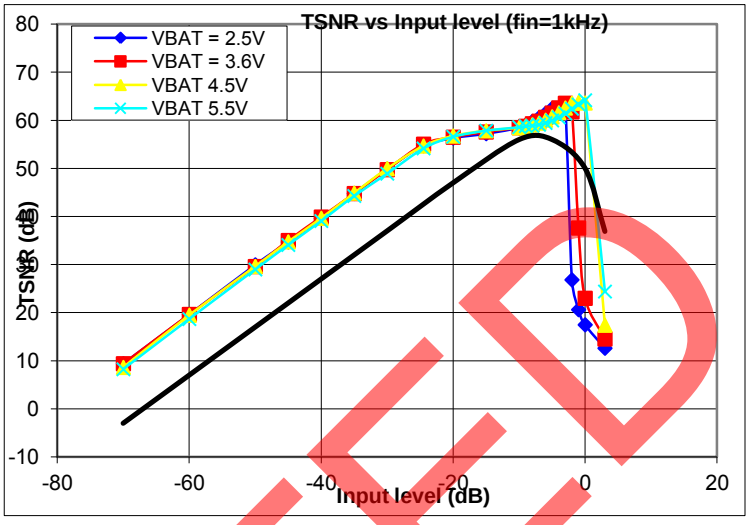

Fig.21.TSNR versus iput level with Gain-12dB

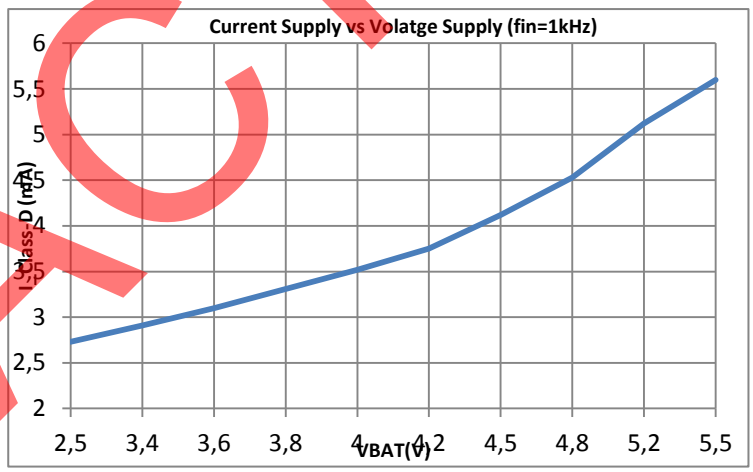

Fig.22. Current Consumption with no Load

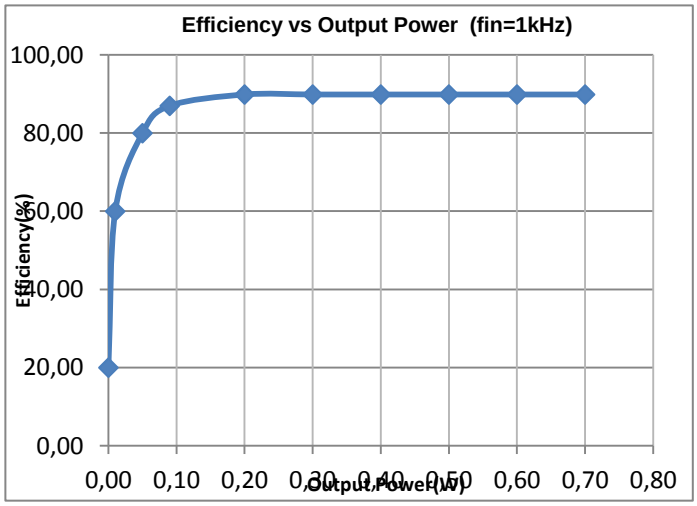

Fig.23. Efficiency versus output power

Tableau 4 Performance comparison

Reference	[9]	[10]	[11]	[12]	[13]	[14]	This Work
THD+N (%)	0.018	0.03	0.7	0.022	0.08	0.1	0.06
Efficiency (%)	85.5	90	88	77	92	79	90
Supply (V)	2.7/4.9	3.7/5	3.3/18	3	2.7	2.3/4.8	2.5/5.5
Load (Ω)	8	4	8	32	-	8	8
Output power (W)	1.15	3.4	100	-	- ..	1	0.5
Fs(KHz)	320	-	384	-	500	-	48
Architecture	PWM	DPWM	PWM/DSM	$\Delta\sum$	SMC	PWM	PWM
Area(mm^2)	1.01	1.59	48.9	1.6	1.6	0.42	1.47
Process	0.18 um CMOS	0.14 um CMOS	0.35 um CMOS	0.18 um CMOS	0.18 um CMOS	0.45 um CMOS	0.18 um CMOS

5 Conclusion

A design of a class-D audio amplifier with analog volume control (AVC) is presented. The proposed AVC can making possible to amplify the input signal from 0 to -24dB in steps of -3 dB for Audio, Voice and FM Volume Control. The proposed class-D amplifier use pulse with modulator (PWM) achieves high quality audio performance with a THD+N of 0.06%. An efficiency of 89.9% can be achieved with a 8-Ω load while delivering an output power of 0.5W. The proposed class-D amplifier was implemented in a 0.18um 1P6M CMOS technology, the total area of the class-D amplifier is 1.47mm2 .The results of this study show good efficiency and low distortion. Therefore, the proposed class-D amplifier is suitable for wireless and portable applications.

References:

[1] D. Self, Audio Power Amplifier Design Handbook, Newnes, Oxford, UK, 4 the dition,2006.

[2] S. Saponara,"Current-feedback architecture for high-slew rate and low-THD high-end audio amplifier," Electronics Letters, vol.44, no.25,pp.1433–1434,2008

[3] Score, Michael, and Donald Dapkus. "Audio Power Amplifier Solutions for New Wireless Phones," Wireless Symposium, February 2000.

[4] Van der Zee, Ronan A. R., and Ed van Tuijl, "A Power-Efficient Audio Amplifier Combining Switching and Linear Techniques," IEEE Journal of Solid-State Circuits, vol. 34, pp. 985-987, July 1999.

[5] Choi, Soo-chang, Jun-woo Lee, Woo-kang Jin, Jae-hwan So, and Suki Kim, "A Design of a 10-W Single Chip Class D Audio Amplifier with Very High Efficiency using CMOS Technology," IEEE ransactions on Consumer Electronics, vol. 45, pp. 465 – 473, August 1999.

[6] Jeong, Jay H., Hawn H. Seong, Jeong H. Yi, Gyu H. Cho, "A class D switching power amplifier with high efficiency and wide bandwidth by dual feedback loops," Proc. of International Conference on consumer Electronics, 1995, pp. 428 –429.

[7] C-C Hsu, and J-T Wu," A highly linear 125-MHz CMOS switched-resistor programmable-gain amplifier " IEEE J. solid-State circuits, vol.38, no.10, Oct 2003, pp. 1663-1630

[8] I. D. Mosely, P. H. Mellor, C. M. Bingham, "Effect of dead time on harmonic distortion in Class-D audio power amplifiers", Electronics letters, 1999, vol. 35, pp. 950-952.

[9] Y. Choi, W.Tak, Y.Yoon, and J. Roh, "A 0.018% THD+N, 88-dB PSRR PWM Class-D. Amplifier forDirect Battery Hookup" IEEE

J.solid-Stat circuits, vol. 47, no,2. Fabruary 2012, pp.454-463.

[10] L. Dooper and M. Berkhout, "A 3.4 W Digital-In Class-D Audio Amplifier in 0.14µm CMOS" IEEE J. Solid-State-Circuits, vol.47, no.7, july 2012. pp. 1524 – 1534.

[11] J-M. Liu, S-H. Chien, and T-H. Kuo, "A 100 W 5.1-Channel Digital Class-D Audio. Amplifier With Single-Chip Design" IEEE J. Solid-State-Circuits, vol. 47, no.6, june 2012. pp. 1344 – 1354.

[12] K. Kang, J Roh, Y. Choi, H. Roh, H. Nam, and S. Lee, "Class-D Audio Amplifier Using 1-Bit Fourth-Order. Delta-Sigma Modulation" IEEE Trans.Circuit Sys.II, vol. 55, no.8, august 2008. pp. 728 – 732.

[13] M. A. Rojas-Gonzálezand E. Sánchez-Sinencio, "Design of a class D audio amplifier IC using sliding mode control and negative feedback," IEEE Trans. Consumer Electron., vol. 53, no. 2, pp.609–617, May 2007.

[14] M.A .Teplechuk, G. Anthony, and A. Christophe. "*True Filterless Class-D Audio Amplifier"* IEEE J. Solid-State-Circuits, vol. 46, no.12, december 2011. pp. 2784 – 2793.

[15] A. Matamura, N. Nishimura, and B. Y. Liu, "Filter less multi-level delta-sigma class-D amplifier for portable applications," in Proc. ISCAS, May 2009, pp.1177–1180.

[16] W. Redman-White "A High Bandwidth Constant gm and Slew Rate Rail-to-Rail CMOS input circuit and its Application to Analog Cells for Low Voltage VLSI Systems", IEEE Journal of solid-state circuits, vol. 32, no. 5, may 1997.

[17] "Analog MOS integrated circuits for signal processing" Gregorian & Temes April 1986.

[18] M.Berkhout and L.Dooper " Class-D Audio Amplifiers in Mobile Applications " IEEE Transactions on circuits and systems—I, regular papers,vol.57,no.5,pp 992-1002,may2010.

[19] J.Lu and R.Gharpurey " Design and Analysis of a Self-Oscillating Class D Audio Amplifier Employing a Hysteretic Comparator " IEEE J.Solid-State-circuits vol.46,no.10, pp 2336-2349 ,october 2011.

[20] C. K. Lam, M. T.Tan, S. M. Cox and K. S.Yeo " Class-D Amplifier Power Stage With PWM Feedback Loop " IEEE Transactions on Power Electronics,vol.28, no.8, pp 3870-3881, August 2013.

[21] S. M. Cox, J. Yu, W.L.Goh and M.T.Tan "Intrinsic Distortion of a Fully Differential BD-Modulated Class-D Amplifier With Analog Feedback" IEEE Transactions on circuits and systems—I, regular papers, Vol.60,no.1,pp 63-73, january 201.