A Novel SVPWM Modulation Algorithm of Voltage Source Rectifier with Minimized Switching Losses

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Abstract: - Since PWM voltage source rectifier (VSR) can not only provide high-quality DC voltage but also realize four-quadrant operation, it is widely used in many applications. In order to improve the overall efficiency of rectifier, it is required to reduce its switching count and switching loss. Given that the switching loss of rectifier is closely related with its modulation algorithms, the existing modulation algorithms should be optimized. At first, what presented in the paper is the theoretical derivation of the multi-solution principle of VSR, as well as the theoretical analysis of the essential relationship between SPWM and SVPWM. Then the minimized switching loss SPWM and SVPWM modulation algorithms injecting zero-sequence component into the objective function of rectifier are presented, and a power loss formula of power device is also provided. The rectifier with minimized switching loss SPWM and SVPWM modulation algorithms is simulated by means of MATLAB/SIMULINK. Then the experimental platform of VSR with minimized switching loss PWM modulation algorithm is realized based on DSP F28335, which has verified the above theoretical analysis and simulation results. The results show that the overall efficiency of the rectifier with minimized switching loss PWM modulation algorithm increases about 2~3% compared to traditional SPWM and SVPWM modulation algorithms.

Key words: - Voltage source rectifier; Multi-solution; Objective function; Zero-sequence component; Minimized switching loss PWM

1 Introduction

With the development of the related technologies, three-phase voltage source rectifier (VSR) is now widely used in varies kinds of applications. Since VSR can not only provide high-quality DC voltage but also realize adjustable input power factor and four-quadrant operation, it has significant social and economic benefits[1-3].

For high power rectifier, higher power causes more switching loss to power devices, which results in harder heat dissipation handling, higher heat dissipation cost and lower power conversion efficiency.

In order to reduce the switching loss of VSR, the paper begins to study from its power circuits and modulation algorithms. A three-phase PWM rectifier in Ref. 5, which employs bidirectional switches and minimized switching loss modulation algorithm, is able to greatly increase its overall efficiency[4]. However, as regards the conventional three-phase bridge PWM VSR, it's the only way to reduce switching loss that a novel PWM modulation algorithm is proposed.

Since PWM rectifier is actually a PWM inverter operating in a different condition, we can maintain power switch stable over a period of time by injecting zero-sequence component into the objective function of rectifier to decrease the equivalent switching frequency and, therefore, reduce switching loss.

Based on the multiple-solution principle of VSR, a novel SPWM modulation algorithm that injects proper zero-sequence component into the objective function of rectifier is presented to minimize switching loss. And it is actually implemented by using the same zero-vector every 60° in space vector region. Moreover, the minimized switching loss VSR is simulated by means of MATLAB/SIMULINK and the above results are verified by experiments.

2 General Solution of VSR

As illustrated in Figure 1, the three-phase VSR is a kind of boost AC-DC converter, which consists of

three-phase AC voltage sources, three-phase boost inductors, 3H-bridge power device arrays and DC energy storage and filter part. In the three-phase VSR, 3H-bridge power device arrays are composed of six reverse inducting switches which include S1 and D1, S3 and D3, S5 and D5, S4 and D4, S6 and D6, S2 and D2, that is each reverse inducting switch consists of an IGBT and an anti-paralleled freewheeling diode (FWD).

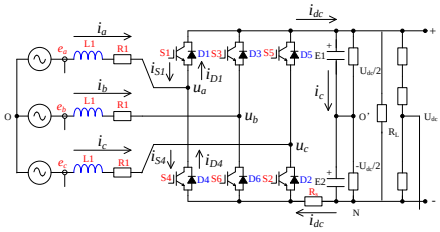


Figure 1. Power circuit of three-phase VSR

To facilitate the study, we assume that three-phase input voltages are symmetric and balanced with no negative-sequence component or zero-sequence component and three-phase input currents are continuous.

Defining k=a，b，c, which represent three phases. Two-valued logic switching function S_k is given as:

$$S_k=\begin{cases}1, & upper\ side\ switch\ on\ lower\ s\\ 0, & upper\ side\ switch\ off\ lower\end{cases} \tag{1}$$

Considering the symmetry of three-phase system, three-phase input voltages and currents are given as:

$$e_a + e_b + e_c = 0 \tag{2}$$

$$i_a + i_b + i_c = 0 \tag{3}$$

With the Kirchhoff voltage law and Kirchhoff current law, the equation of voltage-loop at AC side and the nodal equation of current at DC side are obtained as:

$$L_1 \frac{\mathrm{d}i_k}{\mathrm{d}t} = e_k - R_1 i_k - U_{dc}(S_k - \frac{1}{3}\sum_{k=a,b,c} S_k) \tag{4}$$

$$C_1 \frac{\mathrm{d}U_{dc}}{\mathrm{d}t} = i_a S_a + i_b S_b + i_c S_c - \frac{U_{dc}}{R_L} \tag{5}$$

Introducing FFT to switching function, Sk can be derived as:

$$S_k = d_k + \sum_{n=1}^{\infty}(-1)^n \frac{2}{n\pi}\sin(nd_k\pi)\cos(n\omega_s t) \tag{6}$$

Where, d_k is the average value of switching function S_k in one carrier cycle, or PWM duty cycle. Substituting equation 4 and equation 5 into equation 6 and ignoring the high-frequency components of FFT spectrum for convenience, the low-frequency mathematical model of three-phase VSR based on duty cycle is obtained as[5,6]:

$$L_1 \frac{\mathrm{d}i_k}{\mathrm{d}t} = e_k - R_1 i_k - U_{dc}(d_k - \frac{1}{3}\sum_{k=a,b,c} d_k) \tag{7}$$

$$C_1 \frac{\mathrm{d}U_{dc}}{\mathrm{d}t} = i_a d_a + i_b d_b + i_c d_c - \frac{U_{dc}}{R_L} \tag{8}$$

When selecting duty cycle d_k as the variable, the low-frequency mathematical model of three-phase VSR can be modified as:

$$\mathbf{AX} = \mathbf{B} \tag{9}$$

Where:

$$\mathbf{X} = [d_a, d_b, d_c]^{\mathrm{T}} \tag{10}$$

$$\mathbf{A} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \\ i_a & i_b & i_c \end{bmatrix} \tag{11}$$

$$\mathbf{B} = \begin{bmatrix} (e_a - R_1 i_a - L_1 \frac{\mathrm{d}i_a}{\mathrm{d}t})/U_{dc} \\ (e_b - R i_b - L_1 \frac{\mathrm{d}i_b}{\mathrm{d}t})/U_{dc} \\ (e_c - R i_c - L_1 \frac{\mathrm{d}i_c}{\mathrm{d}t})/U_{dc} \\ C_1 \frac{\mathrm{d}U_{dc}}{\mathrm{d}t} + \frac{U_{dc}}{R_L} \end{bmatrix} \tag{12}$$

With equation 2 and 3, the solution of equation 9 is obtained as:

$$\mathbf{X} = \begin{bmatrix} (e_a - R_1 i_a - L_1 \frac{\mathrm{d}i_a}{\mathrm{d}t})/U_{dc} \\ (e_b - R_1 i_b - L_1 \frac{\mathrm{d}i_b}{\mathrm{d}t})/U_{dc} \\ (e_c - R_1 i_c - L_1 \frac{\mathrm{d}i_c}{\mathrm{d}t})/U_{dc} \end{bmatrix} + \begin{bmatrix} u_0 \\ u_0 \\ u_0 \end{bmatrix} \tag{13}$$

Where, $u_k = e_k - R_1 i_k - L_1 \frac{\mathrm{d}i_k}{\mathrm{d}t}$ represents the neutral-point voltage function of each bridge, $(e_k - R_1 i_k - L_1 \frac{\mathrm{d}i_k}{\mathrm{d}t})/U_{dc}$ represents the duty cycle function of the neutral-point of each bridge， u_0 is any zero-sequence voltage component added. The neutral-point voltage modulation of each bridge is defined as:

$$m = U_{km}/U_{dc} \tag{14}$$

Where, U_{km} is the magnitude of the neutral-point voltage of each bridge.

As shown in Figure 1, point O and O′ are connected together to facilitate the study. The initial phase of grid voltage is set as θ_{m}, the initial phase of the inductor current is set as θ_{L}, the initial phase of the neutral-point objective voltage u_{a} of a-phase bridge relative to the voltage of grid side is set as θ_{B}. Thus, equation 13 is modified as:

$$\begin{aligned}\mathbf{X} &= \begin{bmatrix} m\sin(\omega t+\theta_{\mathrm{B}}) \\ m\sin(\omega t+\theta_{\mathrm{B}}-2\pi/3) \\ m\sin(\omega t+\theta_{\mathrm{B}}+2\pi/3)\end{bmatrix}+\begin{bmatrix} d_0 \\ d_0 \\ d_0\end{bmatrix} \\ &= \begin{bmatrix} d_{\mathrm{ap}} \\ d_{\mathrm{bp}} \\ d_{\mathrm{cp}}\end{bmatrix}+\begin{bmatrix} d_0 \\ d_0 \\ d_0\end{bmatrix}\end{aligned} \tag{15}$$

Where, $m\in[0,1]$ is the modulation, d_{kp} is the positive-sequence component of switching function d_{k}, while d_0 is its zero-sequence component. Due to the switching function $d_{\mathrm{k}}\in[0,1]$, the value range of zero-sequence d_0 should meet the following condition:

$$0\le d_{\mathrm{kp}}+d_0\le 1 \tag{16}$$

Based on the above said, the solution of switching function of the rectifier with symmetric and balanced three-phase input voltages and currents has the following characteristics: (1) there is only one positive-sequence component in steady state whose magnitude is exactly the voltage modulation m; (2) there are varies zero-sequence components satisfying equation 16.

By injecting different zero-sequence components into objective function, different kinds of PWM modulation algorithms can be obtained, such as SPWM, SVPWM and minimized switching loss PWM[7-9].

3 The Principle of Minimized Switching Loss Modulation Algorithm

3.1 Traditional SPWM Modulation Algorithm

All the existing modulation algorithms of VSR satisfy the general expression of switching function. Based on high-frequency synthesis theory[10-11] and the operation progress of VSR, the general expression of switching function of the rectifier with bipolar modulation algorithm is given as:

$$\begin{cases} m_{\mathrm{H}}(t)=\dfrac{1}{2}\left(1+\dfrac{g(t)}{U_{\mathrm{dc}}/2}\right) \\ m_{\mathrm{H}}(t)=\dfrac{1}{2}\left(1-\dfrac{g(t)}{U_{\mathrm{dc}}/2}\right)\end{cases} \tag{17}$$

Where, $m_{\mathrm{H}}(t)$ and $m_{\mathrm{L}}(t)$ are the switching functions of upper side switch and lower side switch on a bridge of VSR, respectively. They meet the conditions: $0\le m_{\mathrm{H}}(t)\le 1$, $0\le m_{\mathrm{L}}(t)\le 1$, and $m_{\mathrm{H}}(t)+m_{\mathrm{L}}(t)=1$。 $g(t)$ is the expected output voltage objective function of VSR, U_{dc} is the DC voltage of VSR that may contains ripple voltages. Under linear modulation, the magnitude of $g(t)$ is below $U_{\mathrm{dc}}/2$, and the ratio of $g(t)$ to $U_{\mathrm{dc}}/2$ is exactly the modulation (maximum linear modulation is 1).

$g(t)$ is the fundamental component of the neutral-point voltage of each bridge of VSR, as can be any waveform satisfying the requirements. Since three objective functions of the three bridges have 120° phase differences and the power switches work independently, there can be varies kinds of switch combinations representing zero-vector and nonzero-vector in each switching cycle[12].

3.2 Traditional SVPWM Modulation Algorithm

The three input phase voltages and line voltages are given as:

$$\begin{cases} u_{\mathrm{a}}=U_{\mathrm{m}}\sin(\omega_i t) \\ u_b=U_{\mathrm{m}}\sin(\omega_i t-2\pi/3) \\ u_{\mathrm{c}}=U_{\mathrm{m}}\sin(\omega_i t+2\pi/3)\end{cases} \tag{18}$$

$$\begin{cases} u_{\mathrm{ab}}=\sqrt{3}U_{\mathrm{m}}\sin(\omega_i t+\pi/6) \\ u_{\mathrm{bc}}=\sqrt{3}U_{\mathrm{m}}\sin(\omega_i t+\pi/6-2\pi/3) \\ u_{ca}=\sqrt{3}U_{\mathrm{m}}\sin(\omega_i t+\pi/6+2\pi/3)\end{cases} \tag{19}$$

Where, U_{m} is the magnitude of phase voltage; ω_{i} is the rotational frequency of grid voltage.

In traditional SVPWM, the eight switch combinations are all used to produce different neutral-point voltages, which can be transformed to eight space vectors with fixed location through PARK transformation, as depicted in Figure 2. In the figure, the length of nonzero-vector is $(2/\sqrt{3})U_{\mathrm{dc}}$, and switch combination “XXX” is the two-valued function of three bridges, where “1” indicates upper side switch on and lower side switch off, “0” indicates upper side switch off and lower side switch on.

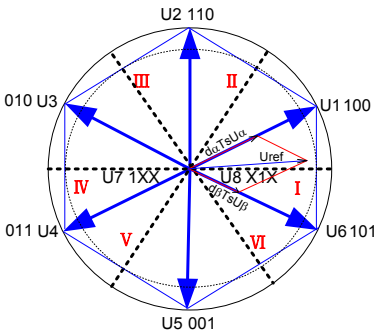


Figure 2. The distribution of voltage space vectors

When entering different section, the reference voltage space vector U_{ref} is synthesized by two nonzero-vector and two zero-vector surrounding the section. The duty cycles of nonzero-vector and zero-vector are determined as:

$$\begin{cases} d_\alpha = (\sqrt{3}U_m / U_{dc})\sin(\pi/3 - \omega_i t) \\ d_\beta = (\sqrt{3}U_m / U_{dc})\sin(\omega_i t) \\ d_0 = 1-(d_\alpha + d_\beta) \end{cases} \quad (20)$$

$$\begin{cases} d_7 = k \cdot d_0 \\ d_8 = (1-k)\cdot d_0 \end{cases} \quad (21)$$

Where, d_α is the duty cycle function of vector α of the section where the reference vector is located, $d_\alpha \in [0,1]$; d_β is the duty cycle function of vector β of the section where the reference vector is located, $d_\beta \in [0,1]$; d_0 is the total duty cycle function of zero-vector, $d_0 \in [0,1]$, $d_\alpha + d_\beta + d_0 = 1$; d_7 is the duty cycle function of the zero-vector with three upper side switches on, while d_8 is the duty cycle function of the zero-vector with three upper side switches off; k is constant, $k \in [0,1]$.

Taking section 2 for an example, the switching mode for traditional 8-segment SVPWM using zero-vector U_7 in the middle of switching cycle is shown in Figure 3.

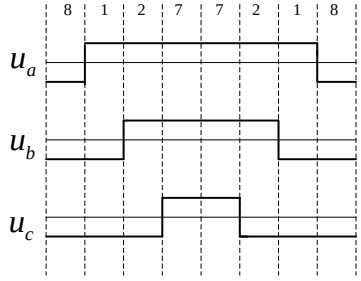


Figure 3. The switching mode of traditional 8-segment SVPWM in section 2.

3.3 Minimized Switching Loss SPWM Modulation Algorithm

With equation 15, when adopting traditional SPWM modulation algorithm, the input sinusoidal objective functions of a-phase, b-phase and c-phase are given as:

$$\begin{cases} u_{aref} = m\sin(\omega_i t + \theta_B) \\ u_{bref} = m\sin(\omega_i t + \theta_B - 2\pi/3) \\ u_{cref} = m\sin(\omega_i t + \theta_B + 2\pi/3) \end{cases} \quad (22)$$

According to SPWM modulation algorithm, we select a zero-sequence component as:

$$\begin{aligned} u_0 = &-\mathrm{k}\cdot\max(u_{aref},\ u_{bref},\ u_{cref}) \\ &-(1-\mathrm{k})\cdot\min(u_{aref},\ u_{bref},\ u_{cref}) \\ &+(2\mathrm{k}-1) \end{aligned} \quad (23)$$

Thus, the new non-sinusoidal objective functions of a-phase, b-phase and c-phase are given as:

$$\begin{cases} u'_{aref} = u_{aref} + \mu \\ u'_{bref} = u_{bref} + \mu \\ u'_{cref} = u_{cref} + \mu \end{cases} \quad (24)$$

As seen in equation 24, different zero-voltage vectors lead to different objective function waveforms. When the modulation changed, the objective function will change accordingly, and u_0 will change too.

The three-phase VSR with minimized switching loss SPWM modulation algorithm is simulated by MATLAB/SIMULINK. The simulation conditions are as follows: grid voltage is the standard commercial power; the expected value of output DC voltage is 650V; the value of load resistor is 50Ω and the output power is 8.45kW. Thus, in unity power factor, the RMS value of phase current is calculated as 12.805A and the magnitude of phase current is calculated as 18.106A.

Assuming the initial phase of grid voltage is $\theta_m = 0$ and the rectifier is working in the state of inductive reactive power, where inductor current lags grid voltage 15°. In this state, the reactive component of inductor current is calculated as $I_q^* = \sqrt{\frac{3}{2}}\cdot\mathrm{tg}(-15°)\cdot 18.106 = -5.942\mathrm{A}$ and the active component of inductor current is calculated as $I_d^* = \sqrt{\frac{3}{2}}\cdot 18.106 = 22.2\mathrm{A}$. The simulation values of the two components of inductor current are -5.942A and 22.6A, respectively. The neutral-point voltage of each

bridge, whose magnitude is 604V, lags grid voltage 11.20°. The dead time of PWM driving signal is set as 0.

If $k=0$, the zero-sequence is given as:

$$u_0 = -[1+\min(u_{\text{aref}},\ u_{\text{bref}},\ u_{\text{cref}})] \tag{25}$$

In this case, the lower switch is turned on for 120° to achieve minimized switching loss SVPWM, and the objective function of a-phase is shown in Figure 4.

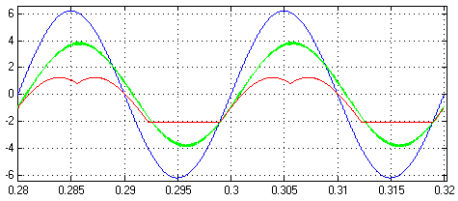


Figure 4. The objective function of a-phase with k=0

If $k=0.5$, the zero-sequence is given as:

$$u_0 = -[\max(u_{\text{aref}},\ u_{\text{bref}},\ u_{\text{cref}}) + \min(u_{\text{aref}},\ u_{\text{bref}},\ u_{\text{cref}})]/2 \tag{26}$$

In this case, the objective function of a-phase is shown in Figure 5, which indicates that this method is the traditional SVPWM modulation algorithm.

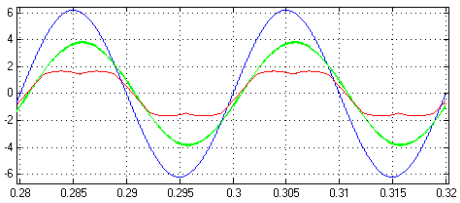


Figure 5. The objective function of a-phase with k=0.5

If $k=1$, the zero-sequence is given as:

$$u_0 = 1-\max(u_{aref},\ u_{bref},\ u_{bref}) \tag{27}$$

In this case, the upper switch is turned on for 120° to achieve minimized switching loss SVPWM, and the objective function of a-phase is shown in Figure 6.

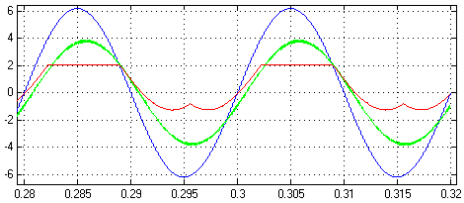


Figure 6. The objective function of a-phase with k=1

If k is switched between 0 and 1 every 60°, the zero-sequence is given as:

$$u_0 = \begin{cases} -\min(u_{aref},\ u_{bref},\ u_{cref}) - 1 & k=0 \\ -\max(u_{bref},\ u_{bref},\ u_{cref}) + 1 & k=1 \end{cases} \tag{28}$$

In this case, the upper switch and lower switch are both turned on for 60° to achieve minimized switching loss SVPWM, and the objective function of a-phase is shown in Figure 7.

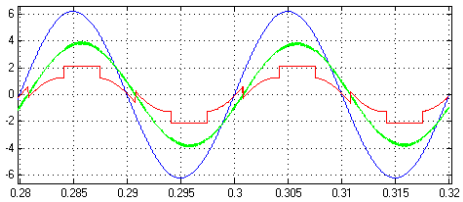


Figure 7. The objective function of a-phase with k=0/1

3.4 Minimized Switching Loss SVPWM Modulation Algorithm

Due to the symmetric control of traditional SVPWM VSR, the power loss of each reverse conducting switch, which consists of IGBT and FWD, is equal. The power loss includes conducting loss and switching loss, as is determined by[13]:

$$P_{\text{Loss}} = g(\bar{U}_{\text{ce}}, \bar{I}_{\text{c}})\, \bar{f}_{\text{s}} \tag{29}$$

Where, $\bar{U}_{\text{ce}}$ is the average conduction voltage drop across power switch, $\bar{I}_{\text{c}}$ is the average conduction current flowing through power switch, $\bar{f}_{\text{s}}$ is the average switching frequency of power switch, P_{Loss} is the average power loss of power switch, which is a monotonically increasing function of $\bar{U}_{\text{ce}}$ and $\bar{I}_{\text{c}}$, and reversely proportional to $\bar{f}_{\text{s}}$.

The above power loss calculation expression is also applied to FWD.

For traditional SVPWM modulation algorithm, $\bar{U}_{\text{ce}}$, $\bar{I}_{\text{c}}$ and $\bar{f}_{\text{s}}$ are not optimized in every section and every switching cycle where $\bar{f}_{\text{s}}$ is equal to carrier frequency f_{c}, which results in much switching loss.

As illustrated in Figure 2, any three adjacent vectors share a same bit (1 or 0), which means that there can be one bridge at most not working to reduce the switching count by one thirds at most. By using the same zero-vector (111 or 000) on both sides of the phase current peak, the minimized switching loss modulation algorithm can not only reduce switching count by one thirds but also avoid switching around the phase current peak(that is(60°, 120°) and

(240°, 300°). Therefore, the maximum peak value of phase current where switch is switching can be reduced by $1-\sqrt{3}/2$ and the switching loss can be reduced by more than one thirds.

There are two methods to realize minimized switching loss SVPWM modulation algorithm, which include single zero-vector modulation and double zero-vector modulation.

Single zero-vector modulation uses only one zero-vector in all sections of voltage space vector plane: U_7 or U_8, which correspond to k=1 and k=0 in equation 21, respectively. Even though this modulation algorithm can reduce switching loss dramatically, it introduces lots of harmful harmonic voltages. The two methods of single zero-vector modulation are named method one and method two, respectively.

While, double zero-vector modulation uses zero-vector U_7 (k=1) in section I、III、V and U_8 (k=0) in section II、IV、VI, as is named method three. It can also uses zero-vector U_8 (k=0) in section I、III、V and U_7 (k=1) in section II、IV、VI, as is named method four.

As for method one and method two, there can be a period of 120° in every output cycle when two power switches of each bridge are not chopping and cause no switching loss. However, one disadvantage of the two methods is that their control is not symmetric, which brings about non-uniform heat to two power switches of each bridge.

As for method three and method four, there can be a period of 60° in both positive half and negative half of output cycle with an interval of 180° when two power switches of each bridge are not chopping and cause no switching loss. Moreover, they will cause no asymmetric control problem and bring uniform heat to two power switches of each bridge[14,15].

The above four methods can all reduce the average switching frequency by one thirds relative to carrier frequency. According to equation 29, the switching loss is related with the angle between the expected input voltage and current ($\theta_L-\theta_B$), which is also a monotonically increasing function of U_{ce} and I_c.

In order to reduce switching loss further, the fifth method of double zero-vector modulation algorithm is proposed. The method five places the switching point of the value of k at the centre line of each section to realize that the 60° non-switching sections in both positive half and negative half of output cycle are placed on both sides of the phase current peak symmetrically, as shown in Figure 8. In the 30° regions on each side of the phase current peak of positive half of output cycle, the upper side switch is on, while the lower one is off. On the contrary, in the 30° regions on each side of the phase current peak of negative half of output cycle, the upper side switch is off, while the lower one is on. In this way, the switching loss can be dramatically reduced, especially for high frequency and high phase current applications.

Defining the angle by which the 60° non-switching section's central line lags grid voltage peak point as the non-switching section's lag angle δ. If δ is equal to $\theta_m-\theta_L$, two 60° non-switching sections will be located in the two 60° sections around the phase current peak in both positive and negative half of output cycle. Based on

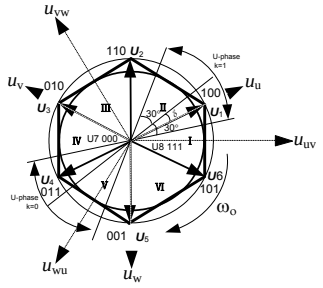


Figure 8. Minimized switching loss SVPWM modulation algorithm

inductive reactive power or capacitive reactive power delivered to the grid by rectifier, $\theta_m-\theta_L$ is set as positive value and negative value, respectively. Defining $\delta'=\delta-30°$ to facilitating the analysis, so δ, δ', $\theta_m-\theta_L$ and k are given as:

$$\delta=\begin{cases}\theta_m-\theta_L & |\theta_m-\theta_L|\le 30^\circ\\ 30^\circ & \theta_m-\theta_L>30^\circ\\ -30^\circ & \theta_m-\theta_L<-30^\circ\end{cases} \tag{30}$$

$$\mathrm{k}=\begin{cases}1 & \omega_o t\in[330^\circ+\delta',360^\circ]\\ & \quad\cup[0,30^\circ+\delta']\\ 0 & \omega_o t\in[30^\circ+\delta',90^\circ+\delta']\\ 1 & \omega_o t\in[90^\circ+\delta',150^\circ+\delta']\\ 0 & \omega_o t\in[150^\circ+\delta',210^\circ+\delta']\\ 1 & \omega_o t\in[210^\circ+\delta',270^\circ+\delta']\\ 0 & \omega_o t\in[270^\circ+\delta',330^\circ+\delta']\end{cases} \tag{31}$$

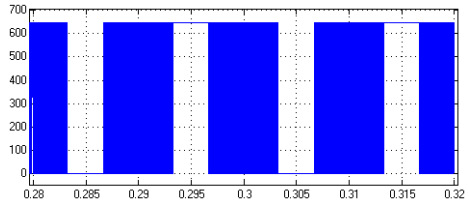
Where, ω_o is the rotational frequency of grid voltage.

If $|\theta_m - \theta_L| \le 30^\circ$ and $\cos(\theta_m - \theta_L) \ge 0.866$, two 60° non-switching sections will be located in the two 60° sections around the phase current peak in both positive and negative half of output cycle. Due to the four-quadrant operation of VSR, equation 31 is very useful. For example, when the rectifier is working with unity power factor ($\delta = \theta_m - \theta_L = 0$), the zero-vector varying with $\omega_o t$ is given as:

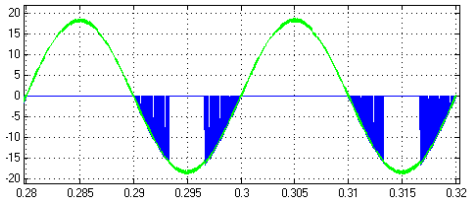
$$U_o = \begin{cases} 111 & \omega_o t \in [0^\circ, 30^\circ] \\ 000 & \omega_o t \in [30^\circ, 90^\circ] \\ 111 & \omega_o t \in [90^\circ, 150^\circ] \\ 000 & \omega_o t \in [150^\circ, 210^\circ] \\ 111 & \omega_o t \in [210^\circ, 270^\circ] \\ 000 & \omega_o t \in [270^\circ, 330^\circ] \\ 111 & \omega_o t \in [330^\circ, 360^\circ] \end{cases} \quad (32)$$

The three-phase VSR with minimized switching loss SVPWM modulation algorithm is simulated by MATLAB/SIMULINK. The simulation conditions are as follows: grid voltage is the standard commercial power; selecting 680μF electrolytic capacitor and 10mH inductor with ESR of 0.1Ω; the expected average voltage of DC loop is set as 650V; The rectifier is operating in power supply state with resistive loads, whose output power is 8.45kW; Switching frequency is 10khz; Dead time is not considered in the simulation.

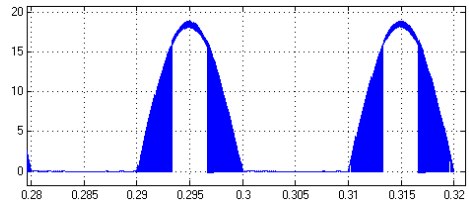
In unity input power factor state, Figure 9 shows (a) the voltage across the upper switch S1, (b) the current flowing through S1 and the input current of a-phase, (c) the current flowing through D4, (d) the switching function of a-phase, (e) the zero-sequence component. The angle between grid voltage and input current is 0 and the angle between the expected input voltage and grid voltage is $\theta_B = -10.3°$ and the magnitude of neutral-point voltage of a-phase bridge is 620V.



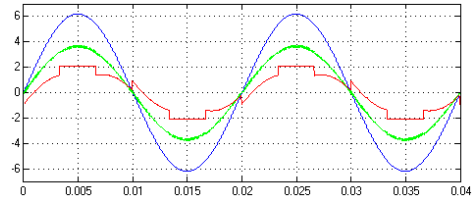
(a) The voltage across upper side IGBT



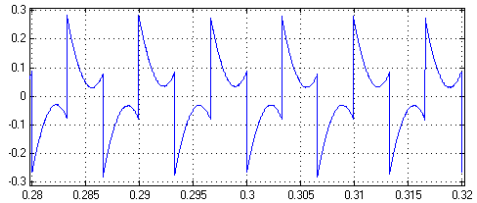
1-the current of upper side IGBT S1; 2-input current
(b) The current of upper side IGBT S1 and input current



(c) The current of FRD D4



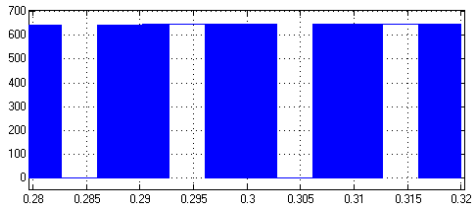
(d) Synthesized switching function of a-phase



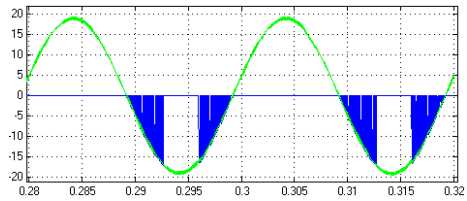
(e) Zero-sequence component

Figure 9. The voltage across switch and current for minimized switching loss modulation algorithm

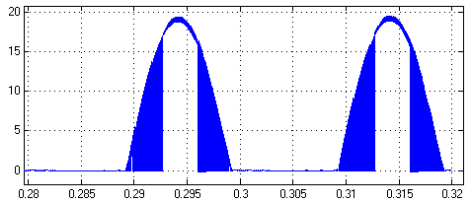
In capacitive input power factor state, Figure 10 shows (a) the voltage across the upper switch S1, (b) the current flowing through S1 and the input current of a-phase, (c) the current flowing through D4, (d) the switching function of a-phase, (e) the zero-sequence component. The angle between grid voltage and input current is +15° and the angle between the expected input voltage and grid voltage is $\theta_B = -10.3°$ and the magnitude of neutral-point voltage of a-phase bridge is 650V.



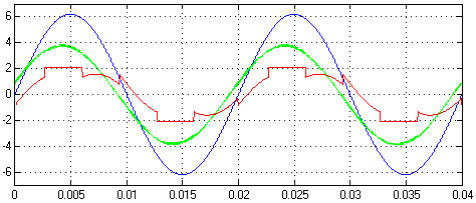
(a) The voltage across upper side IGBT



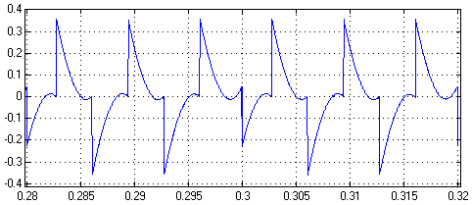
1-the current of upper side IGBT S1; 2-input current
(b) The current of upper side IGBT S1 and input current



(c) The current of FRD D4



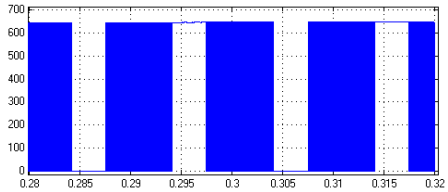
(d) Synthesized switching function of a-phase



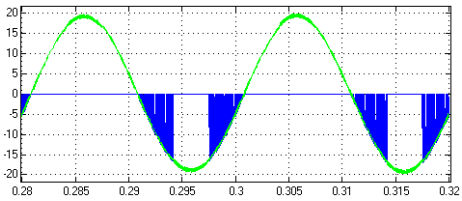
(e) Zero-sequence component

Figure 10. The voltage across switch and current for minimized switching loss modulation algorithm

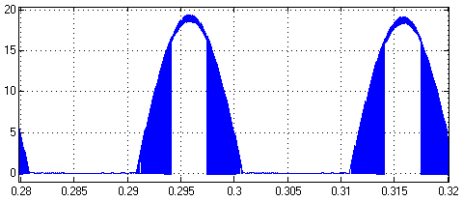
In inductive input power factor state, Figure 11 shows (a) the voltage across the upper switch S1, (b) the current flowing through S1 and the input current of a-phase, (c) the current flowing through D4, (d) the switching function of a-phase, (e) the zero-sequence component. The angle between grid voltage and input current is -15° and the angle between the expected input voltage and grid voltage is $\theta_B = -10.3°$ and the magnitude of neutral-point voltage of a-phase bridge is 604V.



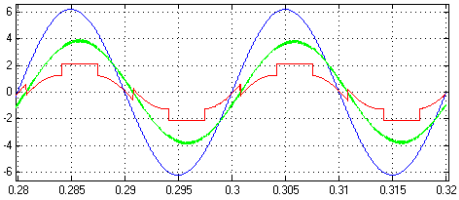
(a) The voltage across upper side IGBT



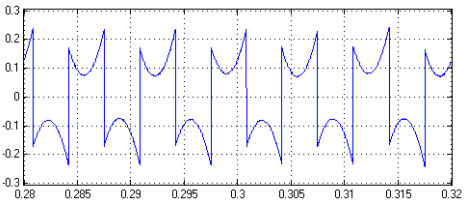
1-the current of upper side IGBT S1; 2-input current
(b) The current of upper side IGBT S1 and input current



(c) The current of FRD D4



(d) Synthesized switching function of a-phase



(e) Zero sequence-component

Figure 11. The voltage across switch and current for minimized switching loss modulation algorithm

As seen in the above figures, the minimized switching loss SVPWM modulation algorithm is corrected.

By analyzing the direct power control (DPC) algorithm of PWM VSR, the DPC algorithm is actually similar to minimized switching loss SVPWM algorithm, except for starting point of control and switching frequency[16]. Though combining control with modulation, the switching frequency of DPC algorithm is not fixed, as is bad for inductor selecting and device safe. It is sure that DPC can be modified as direct power SVPWM modulation algorithm with fixed switching frequency. The switching table for DPC is shown in table 1.

TABLE I. THE SWITCHING TABLE FOR DPC

S_p	S_q	S_a S_b S_c					
		I	II	III	IV	V	VI
0	0	101	100	100	110	110	010
0	1	100	110	110	010	010	011
1	0	101	111	100	000	110	111
1	1	111	111	000	000	111	111
S_p	S_q	VII	VIII	IX	X	XI	XII
0	0	010	011	011	001	001	101
0	1	011	001	001	101	101	100
1	0	010	000	011	111	001	000
1	1	000	000	111	111	000	000

3.5 The Loss Calculation for Minimized Switching Loss SVPWM Modulation Algorithm

Defining the angle between inductor current and neutral-point voltage of each bridge as $\theta_{LB}=\theta_L-\theta_B$. Based on the phase relationship between switching function and input current, the average conducting loss of the power switch (IGBT) and freewheeling diode (FWD) is determined as:

$$P_{S1}=\frac{1}{2\pi}\int_0^{\pi}\frac{1-u'_{aref}}{2}u_{ce(sat)}\cdot I_p\sin(\omega_i t-\theta_{LB})d\omega_i t \qquad (33)$$

$$P_{D1}=\frac{1}{2\pi}\int_0^{\pi}\frac{1+u'_{aref}}{2}u_{ce(sat)}\cdot I_p\sin(\omega_i t-\theta_{LB})d\omega_i t \qquad (34)$$

Where, I_p is the peak value of input current, $i_c=I_p\sin(\omega_i t-\theta_{LB})$. $u_{ce(sat)}$ is the saturation voltage drop across power switch, which is a function of collector current i_c. Obviously, the conducting loss of IGBT is increasing, while decreasing for FRD compared with traditional SVPWM modulation algorithm.

The average switching loss for IBGT and FWD is determined as:

$$P_{S1}=2\times 50[\int_0^{\pi/6}(E_{on}+E_{off})d\omega_i t \qquad (35)$$

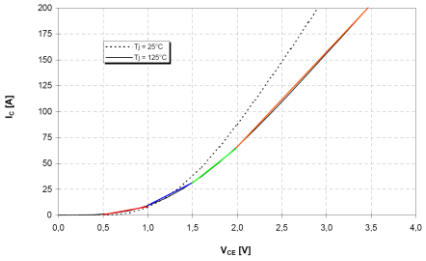
$$P_{D2}=2\times 50\times\int_0^{\pi/6}E_{err}d\omega_i t \qquad (36)$$

Where, E_{on} and E_{off} are the power consumption during the turn-on progress and turn-off progress of IGBT respectively, each of which is a function of collector current i_c. E_{err} is the power consumption during the reverse recovery progress of FWD, which is a function of forward current i_c. The switching loss for each IGBT and FWD is greatly reduced compared with traditional SVPWM modulation algorithm.

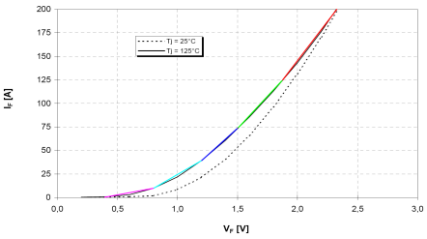
In the above equations, the voltages across power switch and freewheeling diode vary nonlinearly with the current flowing through them. Refer to the related product specification for calculation.

Taking the IGBT module BSM100GB50DLC of EUPEC for an example, the test conditions are as follows: V_{GE}=15V，R_{gon}=R_{goff}=18Ω，Uce=1200V，Tj=125°C。

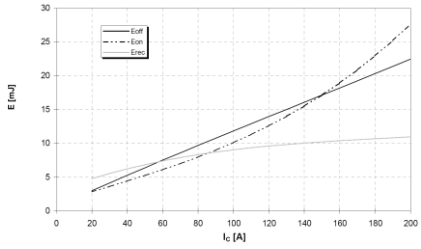
The characteristic curves of IGBT and Diode are shown in Figure 12, in which the data provided by firms is the calculation basic for the power loss of power devices.



(a) IGBT output characteristic curve



(b) Diode forward characteristic curve



(c) IGBT and diode reverse recovery power loss curves

Figure 12. IGBT and diode power loss curves

Assuming that the rectifier is operating in power supply state with resistive loads, whose output power is 8.45kW; The dead time is set as 0; The efficiency of the VSR is 95%; the RMS value of input current is 12.805A and the magnitude of input current is 18.106A.

By calculation, the conducting loss and switching loss of a-phase's upper switch with minimized switching loss SVPWM modulation algorithm are given as:

Average conducting loss: P(S1+D1) ≈5.2W

Average switching loss: P(S1+D1) ≈52W

The conducting loss and switching loss of a-phase's upper switch with the traditional SVPWM modulation algorithm are given as:

Average conducting loss P(S1+D1) ≈3.8W

Average switching loss: P(S1+D1)≈88W

Therefore, the total loss of a-phase's upper switch is reduced by 34.6W with minimized switching loss SVPWM modulation algorithm, which means that the total loss of six switches of the rectifier is reduced by 207.6W. Since the output power of the rectifier is 8.45kW, the efficiency of the rectifier system is improved by 2.4%.

4 The Realization Principle of VSR

4.1 The Block Diagram of Rectifier System

The three-phase VSR adopts the structure of voltage outer-loop and current inner-loop, where the current inner-loop introduces the minimized switching loss PWM modulation algorithm. The power circuit and control circuit of three-phase VSR with unity power factor at grid side are shown in Figure 13.

The output DC voltage is detected and, then compared with the given output DC voltage to get a voltage error, which can produce the given current of d-axis through PI regulator. Set the given current of q-axis as positive value for capacitive input power factor, while negative value for inductive one. Detect the three-phase grid voltages and input currents with sensor, which can obtain the actual currents of d-axis and q-axis through coordinate transformation. In order to achieve the three-phase VSR with unity input power factor, the given current of q-axis is set as 0. The given currents of d-axis and q-axis minus the actual currents of d-axis and q-axis are the current errors, which can produce the given voltage U_d^* and U_q^* through PI regulator, respectively. Then U_d^* and U_q^* are transformed to U_α^* and U_β^* through coordinate transformation, based on which the driving signals can be generated by MCU or DSP to control PIM module.

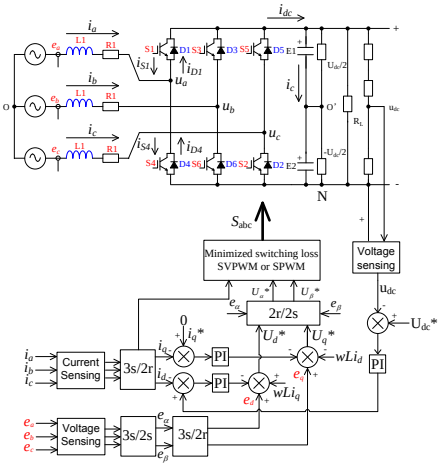


Figure 13. The power circuit and control circuit of three-phase VSR

4.2 Experiment Analysis

In order to verify the above analysis, an experiment is done.

Experiment conditions: standard commercial power with three-phase AC input voltages of 380VAC and 50Hz gird frequency; 680μF electrolytic capacitor , 10mH inductor; the expected average voltage of DC loop is set as 650V; the rectifier is operating in power supply state with resistive loads, whose output power is 8.45kW; switching frequency is 10kHz.

Main components: select 10mH boost inductor designed by silicon steel whose frequency is 10kHz and 680μF filtering capacitor. BSM50GB120DLC: 50A/80°C/1200V is selected as IGBT driven by TPS2812. DSP TMS320F28335 is chose as the controller, which supports floating point operation.

Experimental purpose: unity power factor at grid side.

By software programming and hardware debugging, the VSR system with minimized switching loss PWM modulation algorithm as shown in Figure 13 is implemented.

In steady state, the measured voltage of DC loop is 650V, the peak-to-peak value of ripple voltage is 15V. Figure 14 shows the driving pulse of the lower switch of a-phase after a low pass filter, which is the duty cycle waveform. Figure 15 shows the waveforms of grid voltage and input current with full loads. As seen in the figure, the lower the input current ripple is, the higher the quality of the input current is. Moreover, the input current has the same phase with grid voltage, which means that the input power factor approaches one. By test, within several kW power, the minimized switching loss PWM modulation algorithm can improve the efficiency of

the rectifier system by 2~3% over the traditional PWM modulation algorithm, which will be benefit for heat dissipation and system reliability.

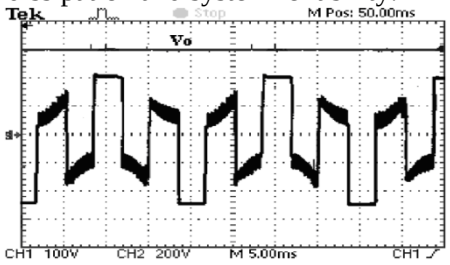


Figure 14. Duty cycle of the lower switch of a-phase

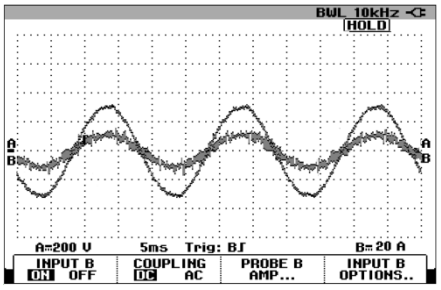


Figure 15. The grid voltage and input current with full loads

5 Conclusion

Based on the multiple-solution principle of voltage source rectifier and the operation principle of SVPWM and SPWM modulation algorithms, a minimized switching loss PWM modulation algorithm is presented in the paper. The VSR with minimized switching loss SPWM and SVPWM modulation algorithm is simulated and verified by means of MATLAB/SIMULINK, and the power loss calculation of minimized SVPWM is also provided. The above theoretical analysis and simulation results are verified by the experiment based on DSP TMS320F28335 control circuit. The results show that the minimized switching loss PWM modulation algorithm can improve the overall efficiency of the rectifier system by 2~3% over the traditional PWM modulation algorithm, which will be benefit for heat dissipation and system reliability.

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