

A New CMOS OP-AMP Design with an Improved Adaptive biasing circuitry

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Abstract: - This paper sets out a new technique for designing an operational amplifier (OP-AMP) using tanner EDA 1um FDSOI CMOS Technology. Fully Depleted Silicon on Insulator used for building integrated circuits to support the temperature changes, the proposed OP-AMP operates at 3.75V power supply and 70uA bias current using the proposed Adaptive Biasing Circuitry (ABC), which its devices operate at the weak inversion to allow low power dissipation of 0.62mW. The 0.064us settling time and 37.016V/ μ s slew rate parameters improved by the ABC technique, reducing the power dissipation by operating the ABC devices in weak inversion. The phase margin is more than 100 degrees for the DC gain of 13.97dB, which is a reasonable margin when temperature range increases.

Key-Words: - Analog Design, OP-AMP, Amplifier, CMOS, Low Power, Settling Time, Weak Inversion.

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1 Introduction

The operational amplifier (OP-AMP) is one of the essential analog circuits for all modern instrumentations such as aerospace and industrial instrumentations, where the output voltage changes quickly from one level to another is mandatory. The parameters of low power dissipation, high temperature, high speed, excellent power supply rejection, and high gain are becoming more important in miniature analog circuits to provide the significant results; these results could be a concern in high-resolution systems [1]. Furthermore, the OP-AMP is one of the fundamental analog blocks of every signal processing tasks, either in weak signal amplifications or complex processing applications in mixed-signal domain such as portables application and a among various audio/video applications [2]. The OP-AMP is so denominated because its original purpose was to provide mathematical operations such as subtraction, multiplication, integration and differentiation, etc. It can be used in instrumentation, scale changing, and a great variety control system [3].

An OP-AMP is essential to deliver the appropriate parameters to match the requirements of various analog converters. In Low dropout (LDO) regulators and switching converters, an OP-AMP

used as an error amplifier to increase the control accuracy of the power transistor [4] [5]. In the Analog/Digital Converters (ADC), the op amp can be used as a buffer to provide the appropriate offset and gain to match the output signal to the input range [6]. Choosing the correct amplifier for a specific application needs to have a precise design. Therefore, it is necessary to develop a design that helps providing the desired parameters such as the (Width/Length) ratio, as well as choosing the best process technology [7]. These inspire developing a special biasing technique, which increases the OP-AMP performances.

At a high temperature operation, the System-On-Chip (SOC) circuits implemented in SOI CMOS are characterized by many benefits including: sub-threshold region or weak inversion and power reduction, and high transconductance (gm). The proposed Silicon on Insulator (SOI) 1um technology in the SoC solutions is being as the next node in the analog design of low power, the benefits of this technology such as minimizing the input voltage and reducing the gate capacitances led to minimize the power dissipation, which is important for the embedded applications. The transistor canal in SOI technology is invented to separate from the bulk by an insulation layer to reduce the gate capacitors thus turns the SoC faster and reducing overall noise.

Moreover, the benefits of high-energy efficiency and low power in weak inversion operation region can also provide the highest transconductance gm. These make SOI technology an ideal choice for analog circuits and low power application. Transconductance Amplifiers in SOI technology process with Low power dissipation have been obtained in previous works [8, 9].

Taking into consideration high-temperature design, we will focus on the design of an OP-AMP in this present work, which is a critical analog block in any embedded system. We will discuss the design, performance and simulation results of the OP-AMP and its bias circuit (ABC).

2 Design Considerations of The Proposed Op-Amp

The conceptual schematic of the proposed OP-AMP is shown in figure 2, which contains the bias circuit to make the OP-AMP self-biased. Indeed, the main grant of the present OP-AMP in the embedded systems is that it has a low power dissipation of the output stage, as well as a significant phase margin that allows working in very high temperature with guaranteed stability in a wide frequency range.

The OP-AMP architecture is chosen in this work since it has been proven to have a good stability and a high performance at high temperatures. Moreover, the layout of the proposed OP-AMP presented in figure 10 has been designed in compliance with all layout design rules and transistor matching standards in order to integrate it in a SoC.

The operating in weak inversion of MOS transistors in this OP-AMP allows reducing the power consumption of the global system. The current I_{DS} through the MOS transistor channel operating in sub-threshold region based on the channel diffusion current.

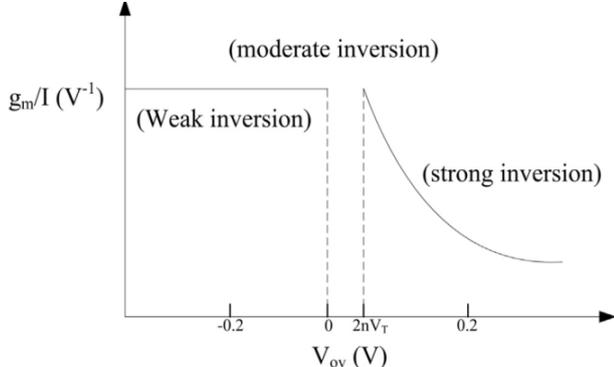


Figure 1. The over drive voltage Vs function regimes.

When $V_{DS} \geq 3kT/q$, the transistor will be saturated and I_{DS} can be given by:

$$I_{DS} = \frac{1}{2} g_{m-sat} (V_{GS} - V_{TH}) = \frac{1}{2} g_{m-sat} V_{OV} \quad (1)$$

While in sub-threshold region can be expressed by:

$$I_{DS} = g_{m-sub} \eta V_T \quad (2)$$

Where g_{m-sub} and g_{m-sat} are the transconductance in sub-threshold and saturation regions respectively current, n is the factor of slope in sub-threshold region which can be defined as $1 + g_{mb}/g_m$.

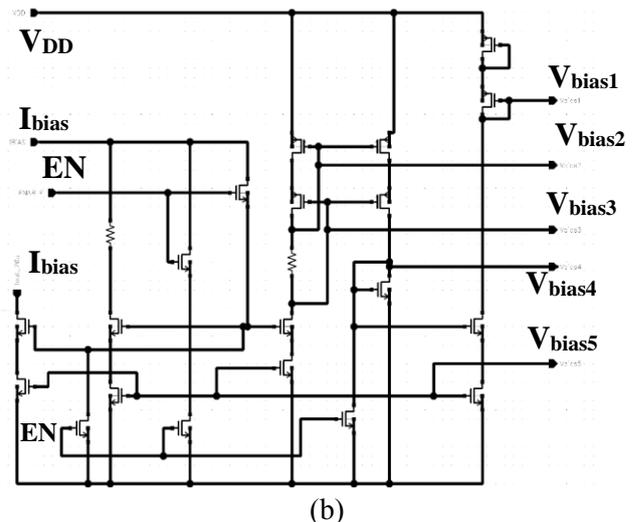
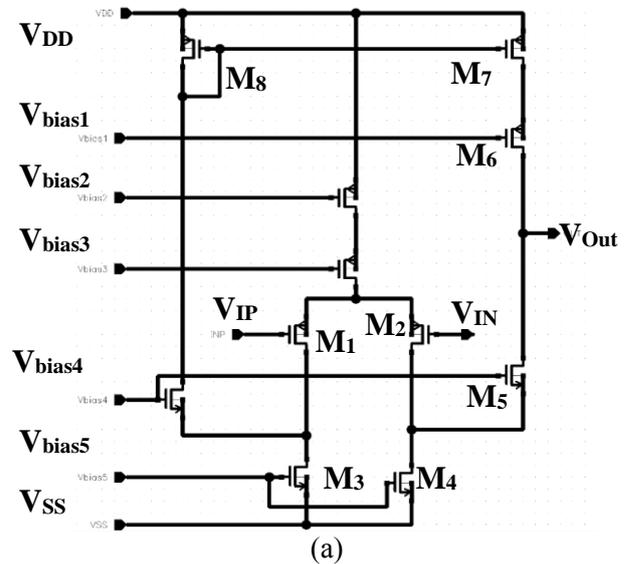


Figure 2. (a) Schematic of the proposed OP-AMP (b) the Adaptive Biasing Circuitry (ABC)

Since threshold voltage $V_{TH} = V_{TO} - (n-1) V_{BS}$, V_{OV} is the over drive voltage and the other symbols

have their usual meanings. To make sure the Adaptive Biasing Circuitry (ABC) works in sub-threshold region instead of the strong inversion function in order to have a high transconductance, VGS should be less significant than $V_{OV} + V_{TH}$ as shown in fig 1:

In the following subsections, the composition of the proposed OP-AMP will be discussed and simulations will show that an excellent settling time is obtained with a significant save in power consumption by implementing the folded cascode biasing circuit, providing a good combination of gain and minimum on chip size.

2.1 The Proposed Adaptive Biasing Circuitry (ABC)

The implementation of the bias circuit shown in fig.2 (b) allows increasing driving capability with an increase of the OP-AMP complexity. Thus, short slew rate and high-speed driving capabilities can be completed during the transient operation. Moreover, to adapt the proposed OP-AMP to function in the desired high temperature, we have adopted a biasing circuit in order to generate a constant transconductance g_m of each device, which affects the DC gain, and stability of the OP-AMP.

As shown in [10] a classic bias circuit was proposed to have constant g_m . Neglecting the body effects, the g_m is given by:

$$g_m = \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_{Ds}} \quad (3)$$

2.2 The proposed OP-AMP design

The schematic diagram of the proposed OP-AMP is shown in Fig.2 (a). It consists of cross-coupled pairs P-channel (M1-M2) with the two series current generator (M10-M11), a multi-current comparators (M3;M4), (M5;M9), and a current mirror (M7;M8), controlled ultimately by the ABC circuit in order to determine the quiescent current and minimize the power dissipation, as well as the architecture is designed to minimize the mismatching, providing overall a simple design. Indeed, when a transient input voltage step applied, the currents I_{ds} through the transistors (M1- M2) increase and decrease proportionally. Considering ΔV^+ and ΔV^- , the positive and the negative input steps amplitudes, the drain current of M6 will increase and decrease to switch ON or OFF the transistor M5, while its gate can be reached the input voltage. As shown in [11] ISR, the drain current of M5 and represents the

contribution to the amplifier SR (slew-rate) and can be expressed by:

$$SR = \frac{\Delta V_{\pm}}{dt} \cong \frac{I_{SR}}{C_L} \quad (4)$$

The Slew-rate enhancement depends on the large load capacitor, this capacitor pushes the dominant pole into the high frequencies which reduces the AC response performance [12]. In this proposed OP-AMP, the ABC circuit is used to improve the SR and enable low-voltage operation consuming much less power and driving a 5 (pf) load capacitor.

2.3 Frequency analysis of the proposed OP-AMP

Since the biasing circuit Fig.2. (b) provides five reference voltages (constant voltages), only the equivalent small signal diagram of Fig.2. (a) is shown and all reference voltages are connected to the ground. To obtain the gain equation, the small signal model of the proposed OP-AMP shown in Figure 3 is needed:

The differential gain equation is given by: $A_d = \frac{V_{out}}{V_{id}}$.

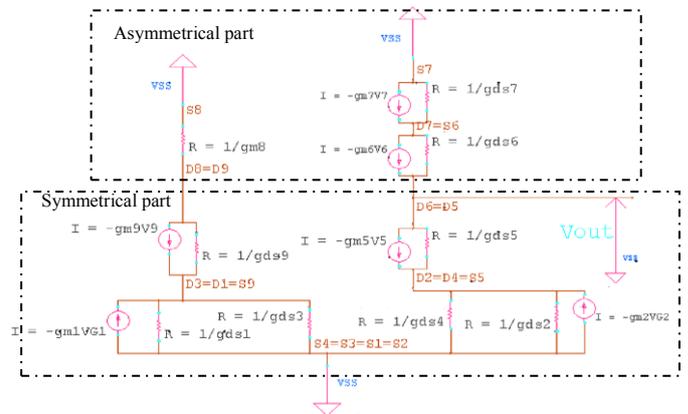


Figure 3. Small signal model of the proposed OP-AMP

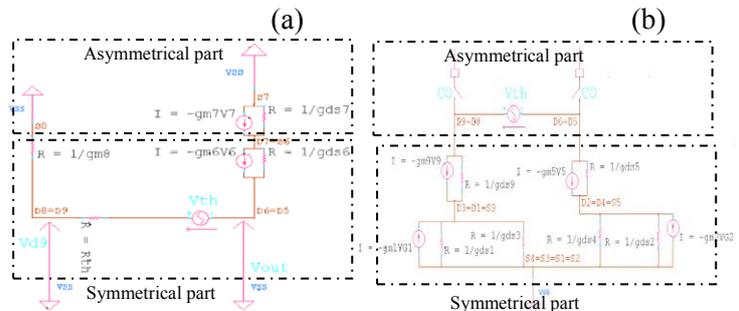


Figure 4. Small signal model of the proposed OP-AMP: (a) and (b) Thevenin presentations of the proposed OP-AMP

The symmetrical part will be replaced by a generator (V_{th}) and a Thevenin resistor (R_{th}), the following diagram is then obtained: Fig.4 (a) and (b). The equivalent scheme for the calculation of V_{th} (symmetrical part operating in differential mode), $V_{s1,2} \approx 0$ will be as follows:

$$R_{th} = 2\left(\frac{1}{g_{DS9}} + \frac{1}{g_{DS1} + g_{DS3}}\right) \quad (5)$$

$$V_{th} = 2V_{D9} = \frac{\left[-\frac{g_{m9,5} * g_{m1,2}}{g_{DS2,1} * g_{DS4,3}}\right] [r_{DS5,9} (r_{DS1,2} // r_{DS3,4})]}{[r_{DS5,9} + (r_{DS1,2} // r_{DS3,4})]} V_{Id} \quad (6)$$

$$A_d = \frac{V_{out}}{V_{id}} = \frac{g_{m9,5} * g_{m1,2} * r_{ds9,5} (r_{ds1,2} // r_{ds3,4})}{(g_{DS2,1} + g_{DS4,3}) (r_{ds9,5} + (r_{ds1,2} // r_{ds3,4}))} \quad (7)$$

3 simulation results

The circuit implementation of the proposed OP-AMP is implemented in 1um FD-SOI CMOS process. All the simulations that simulated with (5pF) load mentioned in Table 1 demonstrate that the proposed amplifier has achieved high performances, such as a fast transient response, low power dissipation and a good phase margin. To allow a high GBW (Gain Bandwidth), the ABC circuit should be as low as possible since the UGF of the OP-AMP proposed is stronger dependent on temperature compared to the gain DC.

3.1 Simulation AC response

AC analysis allows us to characterize the cell performance in order to determine the parameters of the open loop gain, the phase margin, CMRR and PSRR. AC analysis is useful to analyze the effect of noise and to determine the distortion characteristics of the circuit. Figure 5 illustrates the gain and phase of the open-loop op amp. As shown in fig.5, the DC gain is 13.97 dB while the phase margin is 101.62 deg.

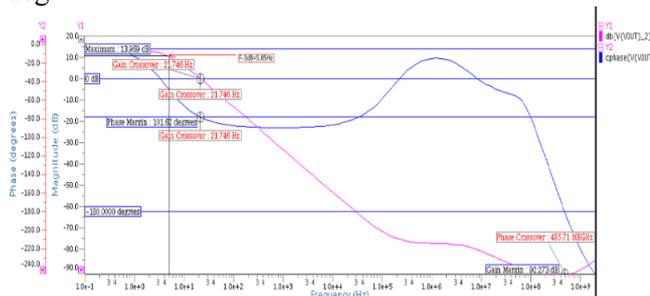


Figure 5. AC response of the proposed OP-AMP

3.2 transient simulation

The transient simulation of the amplifier connected as a follower and supplied as an input in the form of a square-wave signal is shown in Figure 6, which is obtained from the Eldo software.

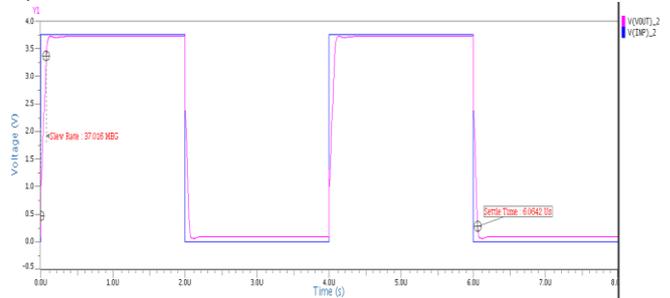


Figure 6. Transient response of the proposed OP-AMP

This analysis allows us to validate the stability of the system by ensuring that the output does not oscillate and that it follows the input. The Slew Rate can be defined as the output signal sweep rate, SR given by the expression (4): According to the curve the settling time (ST) and the Slew Rate (SR) are respectively given by $ST = 0.064 \mu s$, $SR = 37.016 \text{ MG V/s} = 37.016 \text{ V}/\mu s$.

3.3 DC Analysis

The DC analysis is useful for determining the steady-state point (or bias point) of the circuit, the input or output resistance of the circuit, and the sensitivities of the output variables as a function of circuit parameters. First, we start with the simulation of the biasing circuitry in Figure 2 (b), which generates five reference voltages: V_{bias1} , V_{bias2} , V_{bias3} , V_{bias4} and V_{bias5} . The simulation result shown in Figure 7:

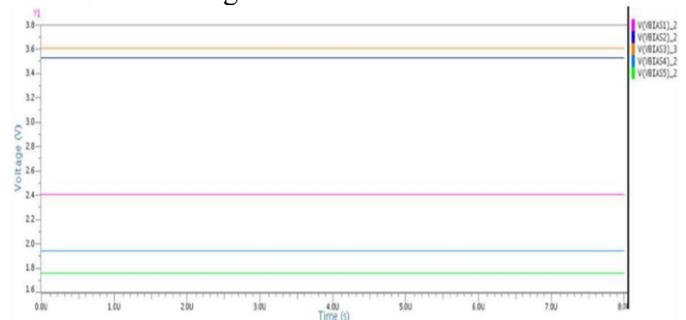


Figure 7. Simulation du circuit de polarisation

3.4 CMRR Simulation

The CMRR (Common Mode Rejection Ratio) of an OP-AMP is calculated by multiplying the common mode gain of the differential input stage by the gain of the second stage (the output stage) and

dividing the open-loop gain on this product $CMRR = A_d / A_{cm}$. The higher CMRR value, the less sensitive to interferences of the amplifier. In this case the simulation prove that the $CMRR = 41.12\text{dB}$ As shown in fig.8

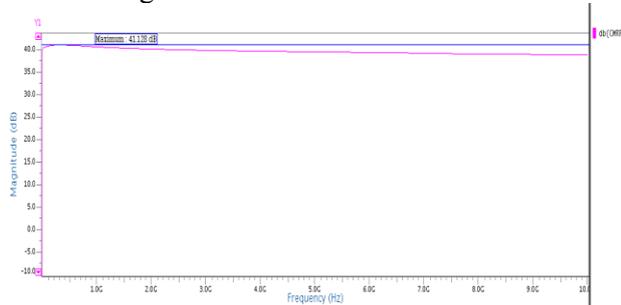


Figure 8. CMRR Magnitude of the proposed OP-AMP

3.5 PSRR simulation

The PSRR is defined as the variation ratio of the supply voltage to the output voltage of the OP-AMP. The $PSRR+$ is the effect of the VDD variation on the output voltage, given by the following formula: $PSRR+ = \Delta V_{dd} / V_{out}$. The $PSRR-$ is the effect of VSS variation on the output voltage, given by the following formula: $PSRR- = \Delta V_{ss} / V_{out}$. The simulation result of the rejection rate of the supply voltage is shown in the following figure :

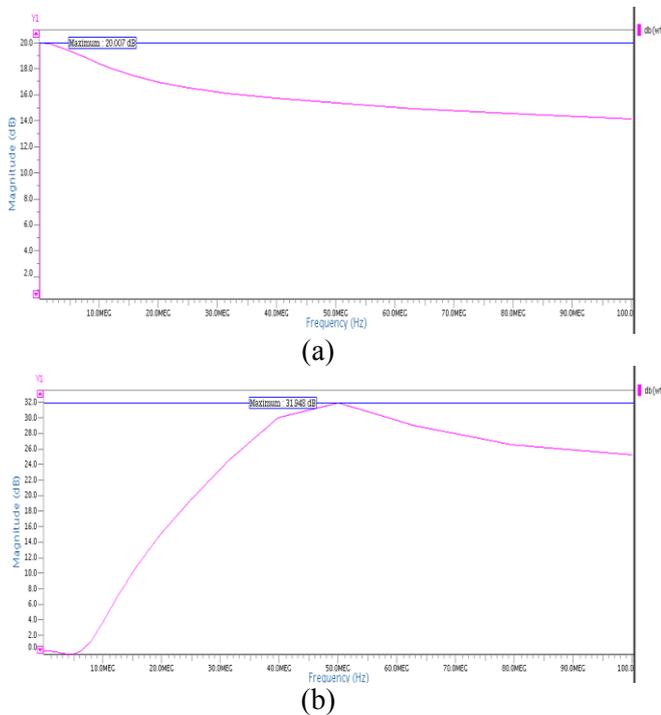


Figure 9. Power Supply Rejection Ratio Simulation (a) $PSRR+$ (b) $PSRR-$

3.6 Full-on-Chip Layout of the proposed op-amp

The layout of the OP-AMP circuit is shown in Fig. 10 with an optimized chip size of 0.0313mm^2 ($182\mu\text{m}$, $172\mu\text{m}$).

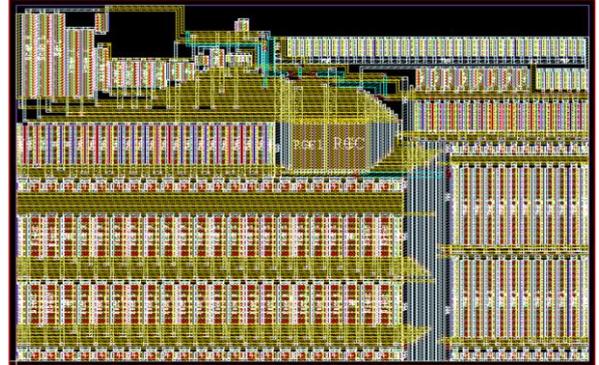


Figure 10. Layout of the proposed OP-AMP, including the ABC circuit

Table 1. Performance of the proposed op-amp and comparison with other works

Parameters	[7]	[11]	This work
Technology process	CMOS $1.8\mu\text{m}$	CMOS $0.35\mu\text{m}$	SOI $1\mu\text{m}$
Input Voltage (V)	1	3	3.75
Temperature ($^{\circ}\text{C}$)	100	-10 to 85	-55 to 225
Biasing Current (μA)	N/A	1.6	7
Load capacitor (pF)	N/A	1000	5
DC Gain(dB)	67.81	N/A	13.97
Phase margin (Deg)	45.9	53	101.62
Gain Margin(dB)	67.81	91	92.27
Slew Rate(V/us)	0.052	6.5/8.1	37.01
ICMR+, ICMR- (V)	[0;0.854]	N/A	[0.22; 3.6]
Settling time(μs)	N/A	1.1	0.064us
CMRR (dB)	104.45@10hz	N/A	41.12
$PSRR-$, $PSRR+$ (dB)	N/A	N/A	20.07; 31.94
Offset (mV)	N/A	N/A	0.5
Power Consumption	7.243 uW	N/A	0.62 mW

4 Conclusion

This work reported the design and simulations of a novel OP-AMP scheme capable of driving a large capacitive load implemented in $1\mu\text{m}$ FDSOI technology. The biasing circuitry eliminates the need for an extra large circuitry allowing saving in power consumption without deteriorating the gain bandwidth. From the presented results summarized in table 1, this low power OP-AMP achieves a good stability, higher gain and lower power dissipation with an optimized chip size.

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