

Phase Locking in Millimeter Wave Frequency Synthesizers - Design overview of Charge Pump Phase Locked Loops

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Abstract: Phase Locked Loops are key blocks which are widely adopted in all area of electronics, especially transceivers in wireless communication systems. The application of Phase Locked Loop varies from generation of local oscillator signal for upconversion and down conversion, generation and distribution of clock signals and jitter reduction. The most extensive use of Phase Locked Loop is for frequency synthesis. The requirements of synthesizer architectures depend on various system requirements and specifications which are based on regulatory standards. The design of Phase Locked Loop components involves the consideration of various techniques to resolve the nonidealities at front end high frequency components as well as back end low frequency components. This paper presents the background and importance of a Phase Locked Loop, various approaches over the years, design choices for each block and practical design methodology for Charge Pump Phase Locked Loops. This paper also presents the system level design of Phase Locked Loop and supply noise interactions among sub modules inside a charge pump Phase Locked Loop.

Key- Words: Phase locking, Charge Pump, Voltage Controlled Oscillator, Frequency dividers, Loop filter
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1 Introduction

Phase locking is an important technique widely employed in majority of analog, digital and RF systems. It is an integral part especially in high speed serial links for clock and data recovery as well as in clock synthesizers. Modern processors and system-on-chips utilize multiple Phase Locked Loops (PLL) to cater their varying demands. Conventional PLLs are implemented using Charge Pump architecture as shown in figure 1.

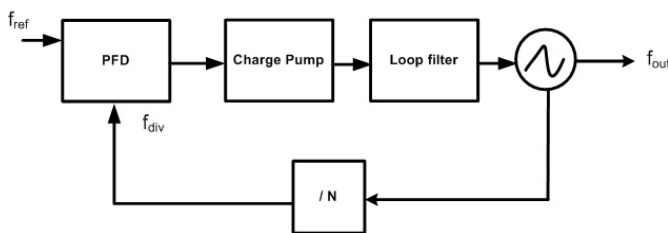


Figure 1: Conceptual diagram of Charge pump PLL

The popularity of charge pump based PLL is because of numerous reasons. Basically it provides flexibility by decoupling various tightly cou-

pled parameters like loop bandwidth and damping factor. A plenty of design examples are available in this arena. The most popular references are provided by [1] and [2]. A typical Charge Pump implementation of PLL consists of a phase and frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO) and divider in feedback to use it for varying applications.

This paper presents an overview of operating principles, basic architecture, and selection of circuit blocks and design methods of Charge Pump Phase Locked Loop based on CMOS technology. The paper is organized as follows. Section 2 gives the fundamentals of Phase Locking, s domain representation of charge pump PLL and frequency synthesizer and figures of merit of PLL. Section 3 and 4 describes the front end and back end components of PLL and its design choices. Section 5 gives the practical design methodology and Section 6 presents system level design of PLL. Finally Section 7 and 8 sums up the state-of-the-art performance of PLLs and supply noise interaction in a charge pump PLL and section 9 concludes the paper.

2 Fundamentals of Phase Locking

PLL is generally characterized in terms of phase and frequency variables. The best analogy to understand PLL is by using a voltage follower as given in figure 2. As the feedback forces V_{out} to be equal to V_{in} in a voltage follower, in a PLL feedback forces output and input phases to be equal. Using the phase variables, all the analysis of any feedback systems like stability analysis or noise analysis could be extended to PLLs also [3]-[5].

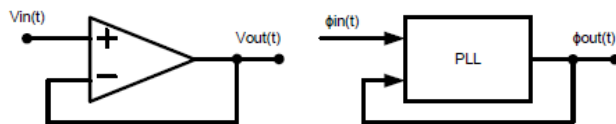


Figure 2: Voltage buffer and PLL

2.1 Classification of Phase Locked Loops

PLL architectures are classified basically depending on the crucial block – Voltage Controlled Oscillator (VCO). Depending on the architecture selected for the implementation of a VCO, PLLs are broadly categorized as Wide band PLL and Narrow band PLL[6]-[8].

2.1.1 Wideband PLL

Wide-band PLLs use VCOs which are generally classified as relaxation oscillators which are implemented as ring oscillators. The frequency of the oscillator depends on the time constant of the individual inverters, the building block of ring VCOs. Ring VCOs generally have a large tuning range and occupy relatively small on-chip footprint, and potentially low power. However, these benefits are offset by the inferior long-term jitter characteristics and for that reason wide-band PLLs are seldom used in applications with stringent long-term jitter requirements[9]-[10].

2.1.2 Narrowband PLL

In Narrow-band PLLs,[11]-[16] VCOs are implemented using resonant characteristics of LC tank circuit. The long-term jitter performance of narrowband PLLs makes them a superior choice over

wideband PLLs. At the same time, these types suffer from a very low tuning range which is only 10-20% of the center frequency. These PLLs consume more area for realizing on chip inductors.

2.2 PLL as a frequency synthesizer

PLL fundamentally corrects the phase difference between the two periodic input signals and the output of the PLL is always a multiplication of the input reference frequency[17]. The output frequency or synthesized frequency can be expressed as

$$f_{out} = N f_{ref} \quad (1)$$

Depending on the N value, synthesizers are classified as an integer synthesizer or a fractional synthesizer[18]-[22].

2.3 S domain model of PLL as a frequency synthesizer

Even though PLLs are nonlinear feedback systems, their operation can be approximated by linear analysis using Laplace transforms. All the individual blocks are represented in s domain to get the complete model. The Fig 3 represents the simplified s domain model of synthesizer[23]-[26].

The type and order of PLL is mostly determined by the number of poles located at origin and the number of poles in the system. All VCOs have a pole at origin which makes all PLL at least type 1. In order to track the phase, another pole is added by a capacitor C_1 at dc. This makes the overall PLL a type 2. But the presence of two poles at origin causes instability. So a resistor R_1 in series with C_1 capacitor is added which introduces a zero and hence stabilizes the loop. The current pulses from charge pump may further produce ripples in the control line of VCO [27]-[31]. The ripples deteriorate the spectral purity and generate spurs. This can be minimized by the addition of another capacitor C_2 , which makes the PLL a type 2, third order synthesizer. Higher order and types of PLL are possible, but seldom used because of loop stability issues. The figure 3 shows the s domain representation of a Type II order 3 system.

The phase frequency detector and charge pump are combined and represented by K_{PFD} . The loop filter used here is of the order two. K_{VCO} , VCO conversion gain represents the tuning or sensitivity of the frequency which is measured in rad/s [32],[33]. The open loop transfer function

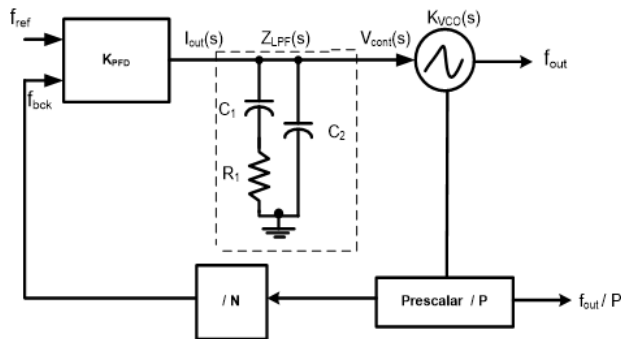


Figure 3: s domain model of PLL as frequency synthesizer

of the synthesizer can be defined as

$$H_{OL}(s) = \frac{K_{PFD}K_{VCO}Z_{LPF}(s)}{NP_s} \quad (2)$$

2.4 Figures of merit of a PLL frequency synthesizer

The design of a PLL is a detailed process which involves multitude of variables. In the preliminary design phase, limiting the number of such variables help in deciding the architecture of each block and adopting the technology node. The three fundamental figures of merit considered in the design of PLL are phase noise, spurs, lock time[34]-[39].

2.4.1 Phase Noise

It is the random deviation of a frequency tone that is spread around the center frequency. Ideally the tone of a PLL is characterized by an impulse, whereas the real one is spread in the frequency domain shown in the figure 4. A transfer function based study will help to estimate the contribution of phase noise of each block to the total phase noise of the PLL. The figure 5 shows the typical phase noise of PLL components.

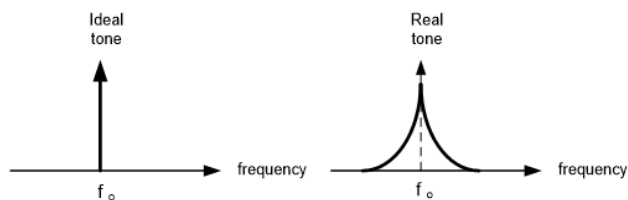


Figure 4: Phase noise effect of a frequency tone

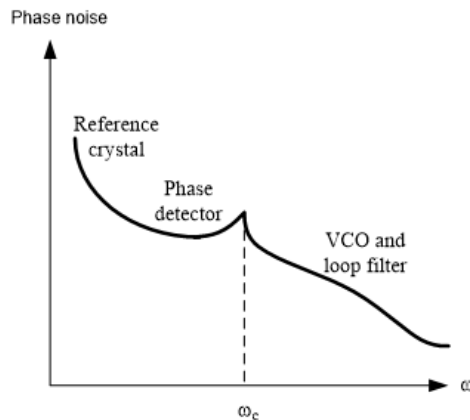


Figure 5: Typical phase noise of PLL components

2.4.2 Spurious Emissions / Spurs

The two fundamental reasons for reference spurs are mismatches of currents in a charge pump and the leakage currents. Banerjee [17] and Maxim [18] proposed two models to predict the spurious emissions. The expression proposed by Banerjee is used to calculate the spurs.

$$Spur_{leak} = Spur_{bl} + 20 \log \frac{Leak}{K_{\phi}} + Spurgain \quad (3)$$

where

$$Spurgain = 20 \log \frac{K_{vco}K_{\phi}Z(s)}{s} \quad (4)$$

2.4.3 Lock time

Lock time specifies the maximum time that can be used in the commutation of a channel to another. This is defined by IEEE 802.11a standard and must be less than 1 ms. In a frequency synthesizer lock time is determined by a set of parameters identified in the loop.

3 PLL front end components and design choices

The components of a frequency synthesizer operate at varying range of frequencies. The prescalars, which are the first stage frequency dividers and voltage controlled oscillators typically operates at high frequency and are together known as front end high frequency components[40]-[43].

3.1 Prescalars / Frequency dividers

The first frequency divider (FD) stages in a synthesizer are called as prescalars. They are not treated separately for a low frequency synthesizer, but for a mm wave synthesizer, prescalar needs to operate at the highest frequency of the loop and thus its design is challenging.

The figure 6 shows the basic classification of prescalar for mm wave frequencies. It is categorized as analog, digital and a combination of both known as hybrid. The choice of different topologies depends on various requirements like power consumption, locking range, phase noise and complexity of design.

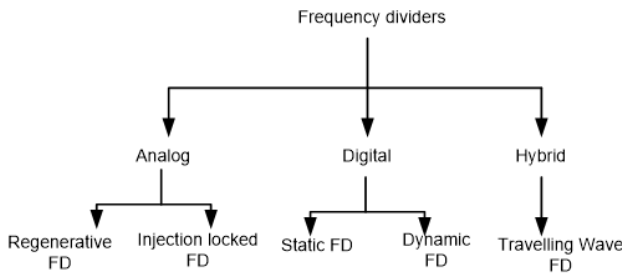


Figure 6: Design choices of prescalars

3.1.1 Analog frequency dividers

The basic analog frequency divider if first proposed in [44] is a regenerative type where it employs a mixer based on a Gilbert cell. These types of dividers does not self oscillate. Moreover the performances of these dividers are not satisfactory above 60 GHz [45-50]. The locking range which is based on eqn 1 is less for these types and power requirement is also more.

$$Lockingrange(\%) = \frac{f_{max} - f_{min}}{f_{center}} \times 100 \quad (5)$$

The promising analog divider which is widely used is of injection locking type where the oscillators are forced to oscillate from its resonant frequency. By properly choosing the amplitude and frequency of the sinusoid, the circuit will oscillate at the injection frequency; the figure 7 shows the injection locking principle. These dividers can be adopted for high frequency division but at the cost of lock range and design complexity.

3.1.2 Digital frequency dividers

The digital dividers are of two types – static and dynamic. Static dividers are mostly based on edge

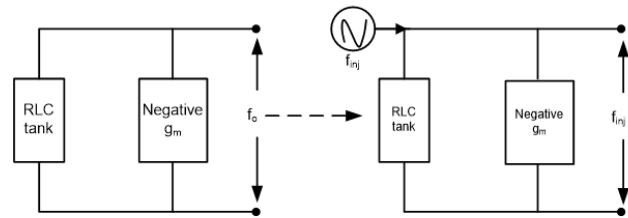


Figure 7: Principle of injection locking

triggered flip flops in a negative feedback loop. The maximum operating frequency of a static FD is given by

$$f_{max} = \frac{1}{2\tau_{pd}} \quad (6)$$

where τ_{pd} is the propagation delay from input to output. [25]- [27] Dynamic dividers are different from static in the use of latches and true single phase clock dividers in the circuit topology. If static is good for better locking range, dynamic is good for its low power consumption.

3.1.3 Travelling Wave frequency dividers

This topology was first proposed in [51] with bipolar technologies and later with CMOS technologies. This topology offers many advantages like differential outputs and less number of transistors leading to less parasitics.

The figure 8 shows a travelling wave FD, where it consists of three differential amplifiers. The operation resembles that of a bistable differential amplifier that can switch between master and slave state. The analog nature of the circuit can be identified by studying the current transitions between different branches of the circuit.

3.2 Voltage Controlled Oscillator

Voltage Controlled Oscillator (VCO) [52]–[53],[63] is considered as the heart of any synthesizer that operates at the highest frequency. It provides the actual oscillations at the output. The spectral purity of the synthesizer depends on VCO and its ability to reject common mode noise. The lock range of the PLL is determined by the tuning range of VCO. Figure 9 shows the classification of VCOs [54].

Ring oscillator is a popular resonator less VCO, where it uses cascade stages of inverters. The tuning of these kinds of oscillators is done by varying the transconductance of the delay stages.

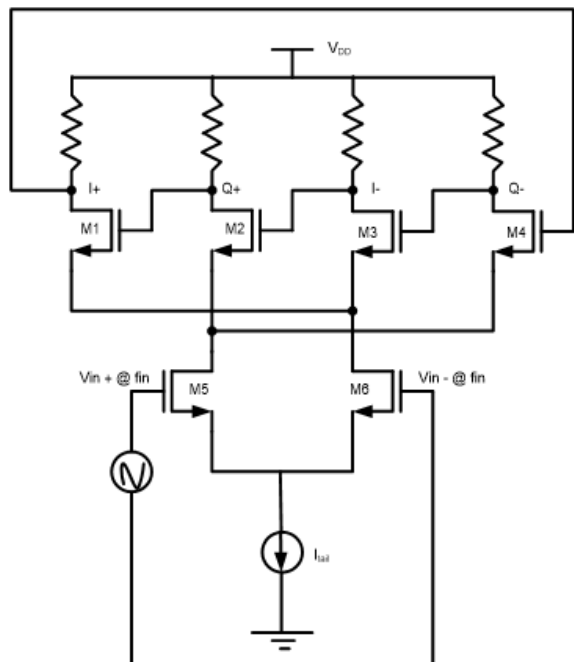


Figure 8: Travelling wave frequency divider

Typically a tuning range of more than 30% is possible with these types. But tuning can be achieved at the cost of spectral purity and phase noise performance. The ring oscillators reported are limited to a maximum of 15 GHz in bulk CMOS processes and therefore not a choice for mm wave frequency synthesizers [55].

Another category is resonator based VCO [54], where a tank circuit is employed. The main advantages of using a resonator based VCO is it can work close to the maximum frequency f_{max} of a given technology [56]. The frequency of oscillation is determined by

$$f_{osc} \approx \frac{1}{2\sqrt{LC}} \quad (7)$$

where L and C are the inductance and capacitance. The design of oscillator with low phase noise can be done using the Leeson's phase noise model as shown in figure 10 [57] – [59]. This model shows the variation of phase noise based on the frequency offset, center frequency and the Q factor of the LC tank.

$$L(\Delta\omega) = 10 \log \left[\frac{2kT}{P_{sig}} F \left(1 + \left(\frac{\omega_o}{2Q\Delta\omega} \right)^2 \right) \left(1 + \frac{\Delta\omega}{f^3} \right) \right] \quad (8)$$

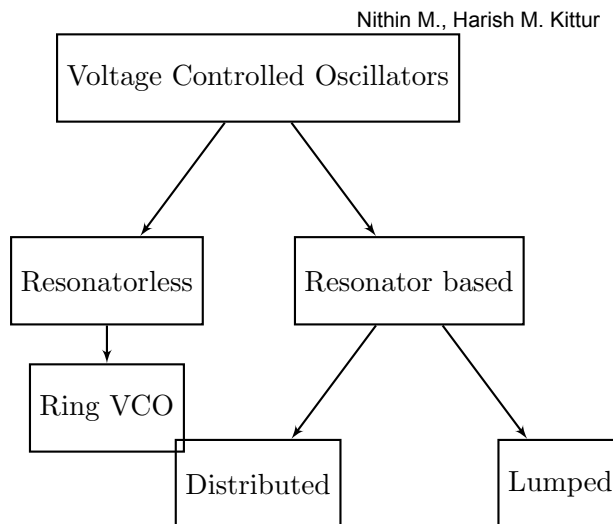


Figure 9: Design choices for VCO

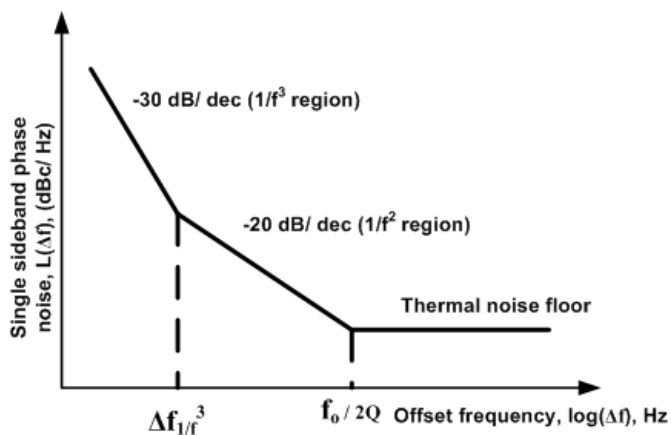


Figure 10: Leeson's phase noise model

The circuit in figure 11 shows a CMOS based VCO. The oscillation frequency is varied by the tuning mechanism and is usually accomplished by the capacitors.

$$Tuningrange = \frac{\Delta f}{f_{center}} \times 100 \quad (9)$$

The voltage swing in the CMOS cross-coupled oscillator is twice the voltage swing in the NMOS cross-coupled oscillator. From (1), the phase noise decreases as the voltage swing increases. In order to have lower phase noise, CMOS topology is better than NMOS type.

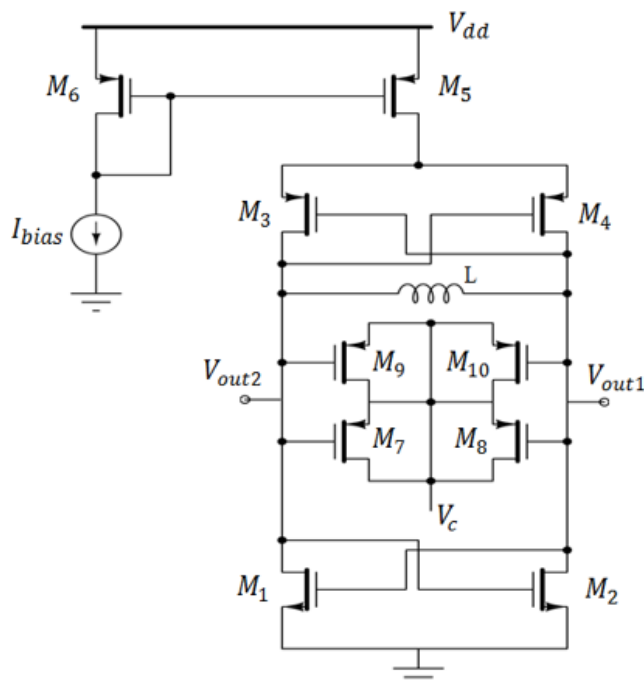


Figure 11: CMOS Cross coupled oscillator

4 PLL Back end Components & design choices

Compared to front end components, PLL back end components including Phase Frequency Detector, Charge pump and feedback divider chain operates at lower frequencies. This section presents an overview and design choices for back end circuits.

4.1 Feedback divider

Feedback divider generates an output which is very close to synthesizer reference frequency. The input for the divider chain comes from the prescaler. In most of the cases the prescaler frequencies will be in the range of GHz and feedback dividers need to divide those frequencies into MHz range to get close to reference frequency.

A dual modulus divider is a widely used circuit to change the division ratio in a frequency synthesizer. These circuits are used when area is a concern and are commonly implemented in MOS Current Mode Logic MCML or Source Coupled Logic (SCL). The different approaches in the design of CML dividers relate the gate delay to the power consumption, with the constraint of a given output swing and voltage gain of the differential pairs, in order to satisfy the requirement on the noise margin. Phase noise is an impor-

tant criterion in the design of dividers, as there is a tight compromise between low phase noise and high frequency of operation. A popular CML based topology is shown in figure 12.

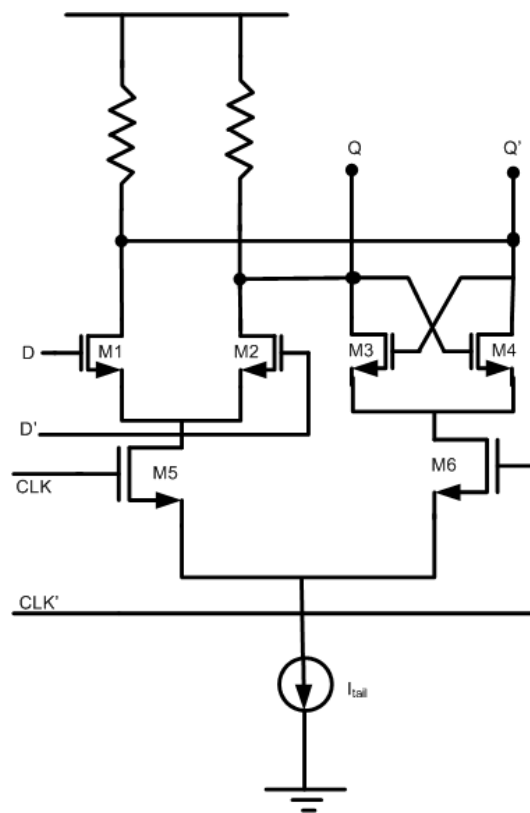


Figure 12: CML based divider

4.2 Phase Frequency Detector, Charge Pump and Loop filter

The components PFD, CP and loop filter forms the rest of the PLL back end whose combined task is to provide a stable dc tuning voltage to the VCO so that synthesizer can move towards lock state.

PFD is a circuit which detects both the phase and frequency between two signals and generates an output in proportion to them. The simple and widely used implementation is with two edge triggered D flip flops.

4.2.1 Practical considerations for the design of PFD

Three fundamental steps are followed in the design of a PFD.

1. The delay estimation of the reset latch
2. Proper scaling of the logic gates

3. Selection of the delay block

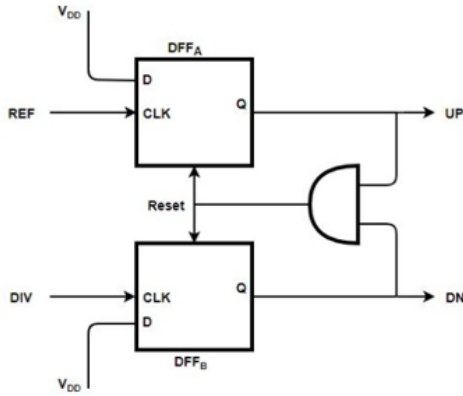


Figure 13: Phase Frequency Detector

PFD implementation has a potential problem known as dead zone problem when the phase error is very small which leads to incorrect operation of subsequent stages or even zero loop gain. This dead zone prevents the synthesizer to work until the phase error reaches a certain minimum value. Many PFD implementations are reported [59-61] aimed at robust designs in improving the various characteristics of PFD like operating frequency, dead zone, complexity, and symmetry. The next component in the line is the charge pump which converts the output signal of PFD into a charge and thereby responsible for moving control voltage of VCO up or down by pumping current in or out of the loop filter as shown in figure 14.

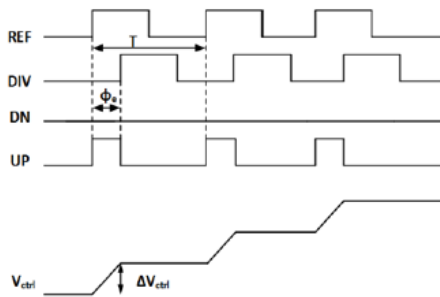


Figure 14: Charge pump output

The increase in V_{ctrl} is given by

$$\Delta V_{ctrl} = \frac{I_{cp}}{C_p} \frac{\Phi_e}{2\pi} T \quad (10)$$

The average charge dumped per cycle is given by

$$Q_{ctrl} = C_p \frac{\Delta V_{ctrl}}{T} = \frac{I_{cp}}{2\pi} \Phi_e \quad (11)$$

The transfer function of the PFD and the charge pump is given by

$$PD(s) = K_{PD} = \frac{I_{CP}}{2\pi} \quad (12)$$

4.2.2 Practical considerations for the design of charge pump

The design of charge pump is done in such way that reduces mismatches between up and down currents and thereby nullifies charge deposition at the loop filter. Fluctuations or variations in the filter voltage due to current mismatch in the charge pump result in reference spurs or discrete spurs in the output spectrum of the frequency synthesizer, called as reference feedthrough. In addition, to maintain a constant loop-bandwidth, the magnitude of the charge pump output currents must be independent of the output voltage.

Authors in [5] proposed a charge pump for low-voltage PLLs that combines a replica biasing technique and a feedback structure. Current matching is improved over a wide output voltage range. Apart from the mismatches, output impedance of the charge pump is also considered invariably.

The loop filter, the last circuit in the back end, suppresses the high frequency components at the charge pump output. The overall loop dynamics and stability depends on loop filter. It consists of a resistor in series with a capacitor C_1 both of which are in parallel with another capacitor C_2 . The capacitor C_1 introduces a pole which is balanced by the resistor introducing a zero so that it is stable in the given frequency range. The addition of C_2 is to suppress the ripples in the control voltage, V_{ctrl} . This may lead to the system becoming unstable. Hence, the capacitor and resistor values are chosen such that they ensure optimum stability and maximum high frequency noise component rejection. The transfer function of the loop filter is given by

$$F(s) = \frac{s + \frac{1}{RC_1}}{s + \frac{C_1 + C_2}{RC_1 C_2} s C_2} \quad (13)$$

The schematic of PFD-CP-LF is as shown in figure 15.

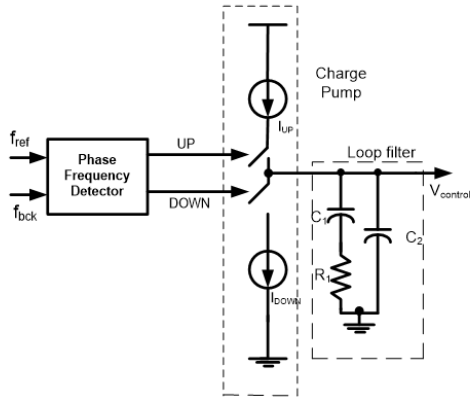


Figure 15: PFD CP Loop Filter

5 Practical Design Methodology

The most crucial part in the design of a frequency synthesizer is the determination of practical and realizable specifications for the back end and front end circuits. This section proposes a practical design methodology to determine the initial requirements for the various specifications that need to be considered for the design. Table 1 shows specifications to be targeted in the design of a mm wave frequency synthesizer.

Table 1: Target specification of millimeter wave frequency synthesizer

Frequency Synthesizer	Locking range	
	Settling time	
	In band phase noise	
	Out of band phase noise	
Front end circuits	Prescalar	Locking range
		Phase noise
	VCO	Tuning range
		Phase noise
Back end circuits	Feedback divider	Division ratio
	PFD	Dead zone

5.1 Identifying Initial requirements of a synthesizer

The first step in the design of a synthesizer is to develop the initial requirements. A sample initial requirement for a mm wave synthesizer is as shown in Table 2.

Table 2: Initial requirements of frequency synthesizer

Initial requirement	Unit or relevant data
Application	WLAN / Wicomm
Technology	Standard CMOS 90 nm
Output frequency	GHz
Reference frequency	MHz
Reference accuracy	ppm
Phase noise @ 1 MHz	dBc/Hz
Reference spurious level	dBc
Settling time	μ s
Supply Voltage	V
Power	mW

5.2 Architectural selection

With the initial requirements, architecture selection can be done for both front end and back end circuits. Depending on the target specifications architectures can be selected and simulated in block level and later.

5.3 Synthesizer integration

The overall circuits can be simulated in any of the available CAD tools. Transistor level simulation of complete synthesizer is a tedious process. Due to the large simulation time, front end and back end circuits are simulated separately before integration. The figure 16 shows practical methodology for the design of synthesizer. It is a good practice to start with the system level simulation before implementing individual blocks in circuit level.

6 System level design of PLL

This section discusses the system level design of PLL using the CPPSim toolkit. The CPPSim package includes two tools namely, PLL Design Assistant and Sue2. Initially the designing is done using PLL Design Assistant which considers the ideal conditions. Further, Sue2 is used to complete the system level design by including the non-idealities like charge pump mismatch and non-zero phase error.

A black box approach in order to understand the operation of PLL is performed using the PLL Design Assistant tool by CPPSim software. The PLL design assistant tool provides a graphical user interface to design PLL at the transfer function level. This section presents the analysis of results obtained using design assistant tool.

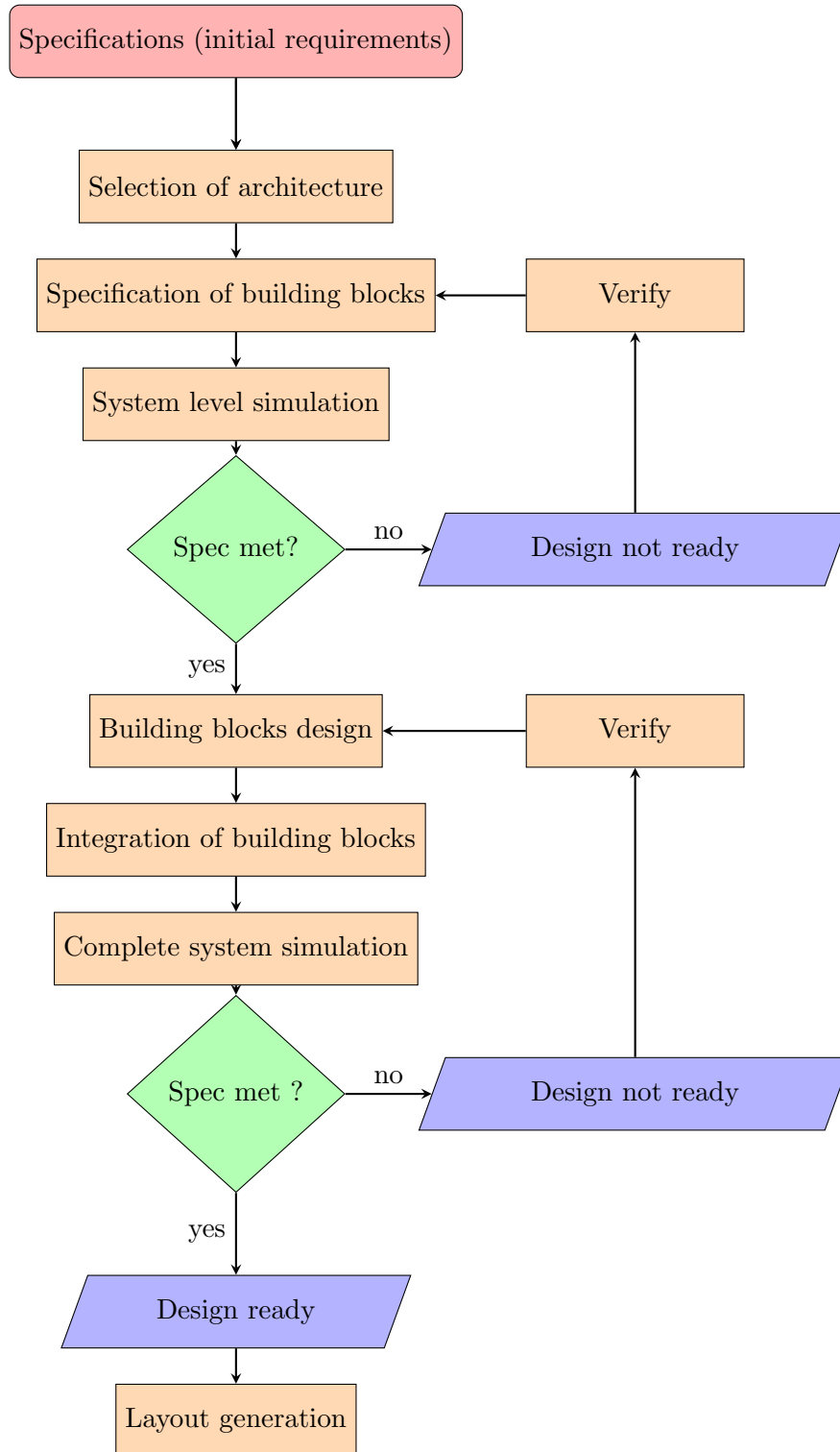


Figure 16: Practical design methodology

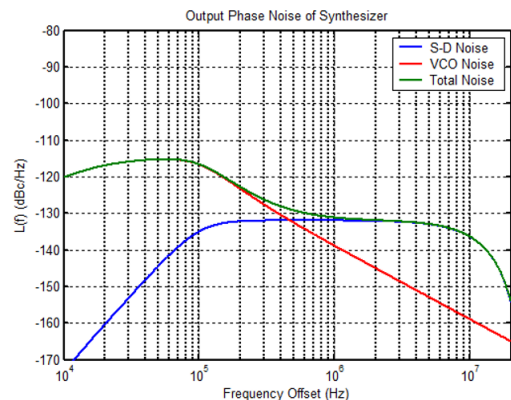


Figure 17: Phase noise plot

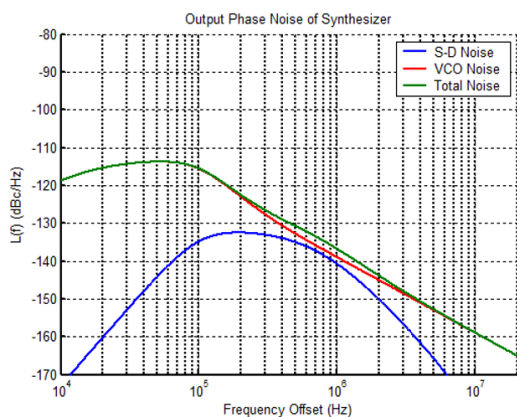


Figure 18: Phase noise plot with addition of parasitic poles

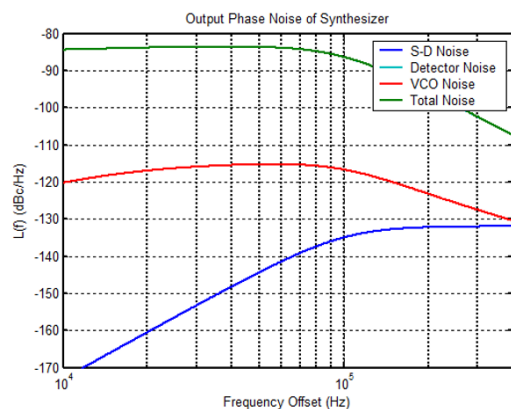


Figure 19: Phase noise plot with -90 dBc/Hz PFD referred noise

With the PLL design assistant, noise performance of the PLL under different configurations was examined and we decided on the system parameters needed to meet the GSM phase noise specifications and also to meet the settling time

requirements. Also, the impact of parameter variations was analyzed along with its effects on phase noise and settling time. Fig 17 to Fig 19 shows the results of phase noise under various conditions and closed loop step response and stability analysis of a PLL designed with PLL design assistant tools.

7 State-of-the-art in CMOS PLL

This section compares different CMOS frequency synthesizers implemented so far in diverse technology processes. An overview of recent state-of-the-art synthesizers representing their technology node and fundamentals figures of merit is given in Table 3. The frequency is expressed in Giga Hertz, technology node in nm, phase noise measured at 1 MHz offset in dBc per Hz and power in milli watts.

Table 3: State-of-the-art CMOS frequency synthesizer

Ref	V_{DD}	f	Tech	PN	P
10	1.2	5.5	130nm	-116.7	36
22	1	5.5	180nm	-115.7	27.5
23	1.8	5.2	180nm	-116.2	-
24	1.8	3.5	180nm	-120.7	-
35	1.8	5.2	180nm	-114.2	-
36	2.5	4.3	250nm	-	117.5
47	1.8	5.2	180nm	-119.2	-
58	2.5	4	250nm	-114	180
59	1.5	4.9	250nm	-104.7	25

8 Supply noise interactions in charge pump PLL

The output noise induced by supply interactions are mainly contributed by the exchange of signals between each sub block and power grid. There are typically five types of signal exchange as indicated in the figure as

1. supply current vs input voltage,
2. all supply currents of sub blocks super impose on the power grid
3. output voltage vs input voltage
4. supply current vs output voltage
5. supply current vs noise to the supply voltage

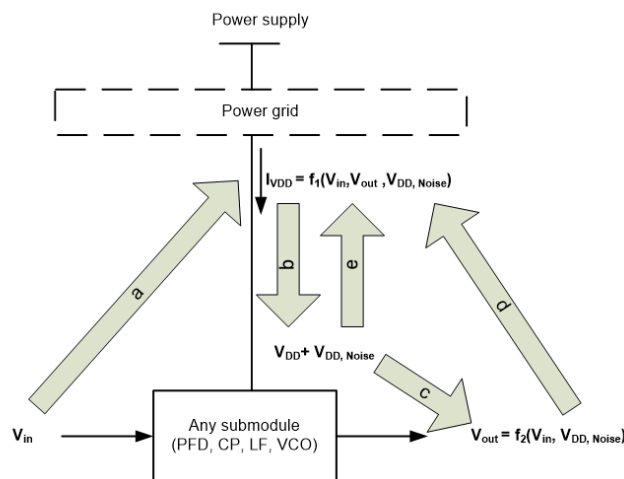


Figure 20: Supply noise interaction in PLL

9 Conclusion

Phase locking as described in this paper is one of the inevitable approaches for frequency synthesis. This paper presented the background and importance of a Phase Locked Loop, various approaches over the years, system level design approaches, practical design methodology, architectures for Charge Pump PLLs. The system level design of a Charge Pump Phase locked loop was presented with PLL design assistant tool and supply noise interactions among sub modules inside a charge pump PLL are also discussed.

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