A 3-Transistor Low Power Rectifier for Wideband RF Energy Harvesting with a Threshold Voltage Compensation Technique using 45 nm Technology

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Abstract: - With the advent of modern wireless communication technology and increasing requirement of high speed network, network life-time is becoming a major area of concern. The need of network power management is gaining attention with the high data network in place and is making a paradigm shift towards green communication. Hence embedding the RF energy harvesting (EH) capability in a wireless network is becoming inevitable. To make RF EH a reality a high frequency rectifier is indeed indispensable along with other circuits in the system. The RF energy needs to be harvested from the available sources in the ambience. It is also seen that the current generation of RF sources radiates at a very low signal power. So, to successfully convert and store this energy, the rectifier must not only be able to provide a sufficiently higher percentage conversion ratio (PCE) but also be able to cater it at a lower range of signal power. This paper presents the design and analysis of a simplified 3-transistor high frequency rectifier. A threshold voltage compensation technique is also incorporated and it achieves a PCE upto 85% at -2dBm in its single stage implementation. This is observed to be one of the highest in-class efficiency as compared to recently reported designs. From the frequency response it is seen to exhibit wide band performance spanning almost all popular wireless bands. The dynamic power dissipation (DPD) is calculated to be 6.25pW at -2dB, whereas the leakage power (LP) is observed to be zero.

Key-Words: -Energy Harvesting, PCE, Transmission Gate, Dynamic Power Dissipation, Leakage Power

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1 Introduction

Modern wireless communication is able to cater the need of high speed data network. Also the demand for higher data rate and seamless connectivity is ever increasing. But with the enhancement of data rate, communication networks tend to become power hungry. Also to successfully install a wireless network in a hard to reach location, power turns out to be the main concern. Hence power management and network life-time are becoming a major areas to be explored. Energy harvesting (EH) is a primary focus area in all such upcoming communication networks. It enables the network to become self-sustaining in physical and virtual modes [1]. Lately, artificial means are receiving greater importance in providing support towards energy harvesting applications. In this regard, network topology, deployment and device design play important roles [1][2][3]. RF EH is a major domain in EH field as multiple RF sources are available in the ambience for harvesting.

An EH design is formed by a rectifier or a charge pump. Several design challenges are faced while designing such a rectifier. Such challenges are identified as high frequency compatibility, low power dissipation, lesser silicon area etc. But the enhancement of the power conversion efficiency (PCE) at lower input power is the most important criteria which the designer must address while formulating an efficient circuit design. A Cross coupled bridge rectifier with differential RF input is reported that provides low on state current and negligible leakage current and thus offers a better PCE[4]. An Ultra High Frequency (UHF) rectification unit based on voltage doubler is also designed with the technique of internal voltage cancellation to facilitate a zero-threshold transistor. They have claimed to achieve a good with reduced area [5]. A very widely used structure in EH is the

Dickson charge pump. Several modifications to the basic structure have been proposed by several designers for specific applications achieving different efficiencies. The Dickson charge pump has been modified to reduce the leakage current with linear regulator and thereby total power consumption can be reduced [6]. Another Dickson charge pump based rectifier with improved performance in two configurations are presented which works in GSM band with a satisfactory PCE [7]. Also dynamic threshold reduction technique based CMOS rectifier has been designed with the use of a clamper to reduce the effective threshold voltage and increase the sensitivity and hence achieving a high PCE [8]. A coplanar waveguide based compact RF rectifier has been proposed in [9], which claims to achieve a peak PCE of 74.8% at 10dBm in the frequency range of 0.1 to 2.5GHz. The structure is cascaded to get a higher output voltage. A low temperature coefficient bandgap voltage reference along with a high efficiency rectifier is reported in [10]. A curvature compensation technique is also proposed and the final PCE of 87.2% is achieved.A low power CMOS full bridge rectifier with four transistors at 130 nm technology is presented in [11]. An AC-DC rectifier, an impedance matching network and a DC-DC converter with maximum power point tracking system is designed which is observed to attain a peak efficiency of 5%.

This paper presents the design and analysis of a simplified 3-transistor high frequency rectifier. A threshold voltage compensation technique is also incorporated and it achieves a PCE upto 85% at -2dBm in its single stage implementation. This is observed to be one of the highest in-class efficiency as compared to recently reported designs. From the frequency response it is seen to exhibit wide band performance spanning almost all popular wireless bands. The dynamic power dissipation (DPD) is calculated to be 6.25pW at -2dB, whereas the leakage power (LP) is observed to be zero.

The remaining of the paper is organized as follows. Section II deals with the proposed design with explanation of the functionality, Section III deals with simulation results and discussion and Section IV includes the concluding remark.

2 Proposed Threshold Voltage Compensated 3-Transistor High Frequency Rectifier

The basic unit of a RF EH consists of a matching unit, a rectifier and a power management unit. This paper is exploring a successful design of a high frequency rectifier. While designing a rectifier the main challenge is to make the circuit work at a low input power. The circuit is subjected to a varying low power signal and when the input voltage falls below threshold voltage value of the nMOS, the rectification from the positive cycle stops.

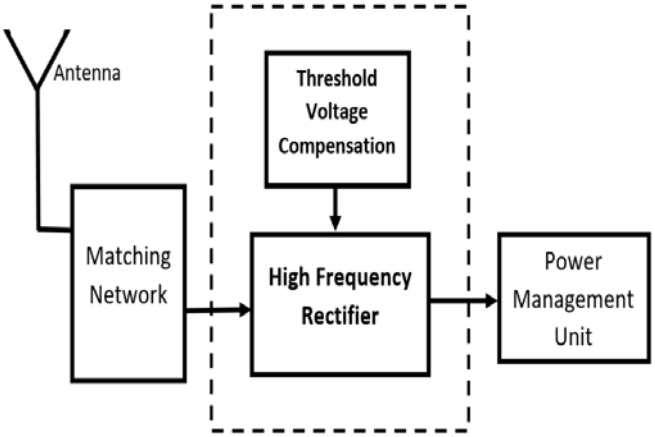

Figure 1: The Block diagram of Proposed RF EH system

Similarly in the negative cycle when the input voltage exceeds the threshold voltage of the pMOS, the rectification cannot happen. This makes the circuit to suffer in terms of the PCE. Hence some threshold voltage compensation technique is required. This will increase the time duration of rectification and thereby contribute towards the betterment of the PCE. The basic block diagram of the proposed system is shown in Fig. 1.

The concept of the proposed design is derived by observing the characteristics of a transmission gate (TG). The TG is a known technology and it finds its application in many CMOS based circuits. It is established that the nMOS pass transistor can pass the negative logic successfully with less propagation time. Again the pMOS pass transistor is known for efficient transfer of positive logic at less propagation time. This makes the TG a well suited candidate for such situations where the circuit needs to deal with both the voltage levels. Another important aspect of TG is that it can generate a sufficiently higher on state current for both the input

levels. This feature is attractive as far as the rectifier design is concerned.

The proposed design of rectifier presented here is a simplified version of the TG based rectifier reported in [12]. The circuit is designed to work with a randomly varying input signal. As the input voltage remains in the positive cycle, the nMOS, which is diode connected will be ON and the TG will allow the current to flow through. When the input goes negative the pMOS in the TG, which is also diode connected makes an open path for the current to flow. The current generated in both the cycles of operation will flow through the diode connected nMOS at the output stage, which is responsible for making the current flow to the output capacitor unidirectional. Thus the rectified output voltage is appeared across the capacitor. But it is observed that the output generated yields a lower PCE than that expected. This is due to the fact that the transistors enter the cut-off states as the value of the RF input signal falls below threshold voltage value of the respective transistor. This makes a threshold voltage compensation technique necessary. This paper proposes a very simple threshold voltage compensation technique with the use of a capacitor at the gate of each transistors as shown in Fig. 2. The capacitor gets charged and retain some charge at every cycle. When the RF input voltage falls below a certain level, the transistor gets a voltage backing at least for some time duration. As the negative terminal of the capacitor connected to the gate of the pMOS, it prevents the pMOS to go to cut-off for some time even when the RF input voltage exceeds the pMOS threshold voltage. This will effectively compensate the threshold voltage and allow the circuit to operate at a wider time period which will in turn enhance the output current and thus the PCE. The proposed 3-transistor rectifier is shown in Fig. 2.

Let us consider the input RF voltage be $V_{in}(t)$, the capacitance connected to the gate of the nMOS be C_c and total resistance at the charging path be R_c. When the input voltage is high the capacitor gets charged and the voltage developed across the capacitor shall be

$$V_c=V_{in}(t)[1-e^{-t/RcCc}] \quad \ldots\ldots\ldots(1)$$

When the input voltage $V_{in}(t)$ falls to a low value, the voltage V_c appeared at the nMOS gate and thereby maintains a sufficiently higher value until it gets discharged below the threshold voltage value. Similarly, in the negative cycle, it protects the pMOS to gets off until the negative voltage exceeds the threshold voltage value. This is a simple way by which we can extend the time of the rectification process and thereby enhance the PCE.

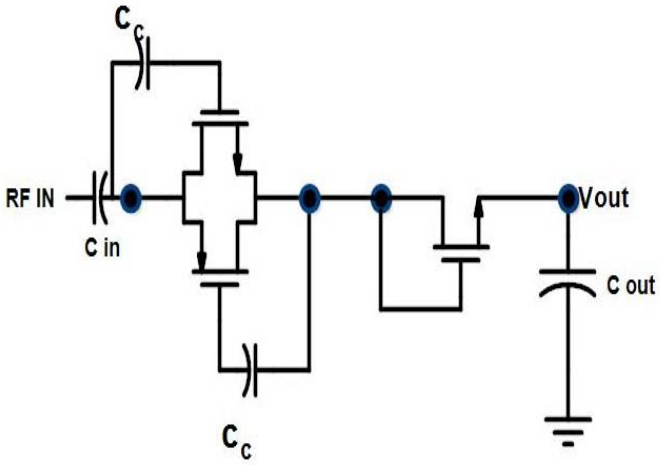

Figure 2: Proposed 3-transitor rectifier with threshold voltage compensation

In a TG structure when input is positive; the pMOS will be initially saturated and then shall switch to non-saturation state while the nMOS will be in saturation state. If we consider the I_{Dn} and I_{Dp} be the current through the nMOS and the pMOS of the TG respectively and V(t) be the RF signal voltage, also I_{Do} be the current through the nMOS of the output stage then the total output current is

$I_{Do}= I_{Dn}$ for positive cycle and $I_{Do}= I_{Dp}$ for the negative cycle of the operation .....(1)

As described in [12], the PCE can be calculated as

$$PCE = (P_{out} / P_{in})*100\% \quad \ldots\ldots\ldots (2)$$

Here the I_{Dn} and I_{Dp} will increase due to the enhancement of rectification time period which will further increase I_{Do}. This makes the charging current at the C_{out} to rise and a higher P_{out} can be obtained. This will lead to the enhancement of PCE. Hence the threshold voltage compensation technique is significant.

3 Results and Discussion

In this section, the results obtained from the experiments are presented and discussed.

Transistor sizing and aspect ratio is a very important aspect in the design for better performance. By using the optimization techniques as reported in [12] the aspect ratio of both the nMOS and the pMOS are tailored as follows. The optimization is done to ensure an optimum power dissipation.

Table 1: Aspect Ratios of both nMOS and pMOS devices

L_n	W_n	L_p	W_p
45nm	150nm	65nm	150nm

The proper rectification a nd the lev el of the output DC voltage can be validated by observing the transient response. The transient resp onse of the circuit is done at 2dB is shown in Fig. 3.The output voltage observed is 823 mV at 2dB input power with threshold voltage compensation.

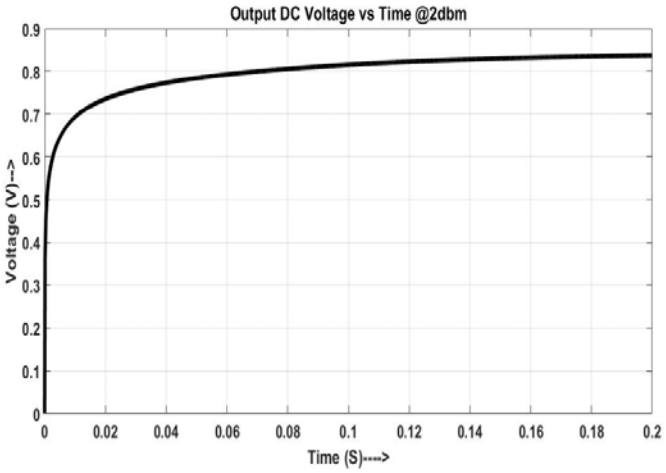

Figure 3: Output Transient DC Voltage

The output voltage and current values are dependent on the circuit components like C_{in} and C_{out} and the performance of the circuit with respect to these valyes needs to be studied. The DC output voltages and currents obtained are plotted with a range input capacitance. Both the ou tput voltage and output current are seen to show a decline with the increase in the value of input capacitances. This is depicted in Fig. 4

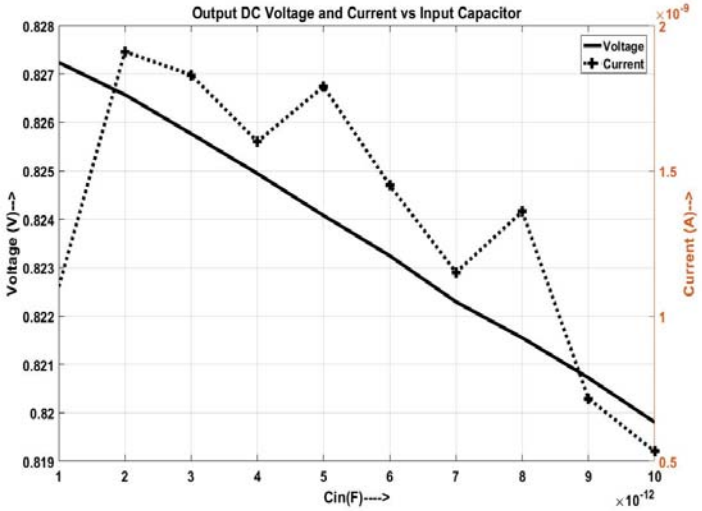

Figure 4: Output DC voltage and current vs C_{in}

The DC outp ut voltage and current are plotted with different value of th e output capacitan ce which is shown in Fig. 5. The voltage value sho ws a gradual decline whereas and current shows almost steady value with the increase in output capacitance.

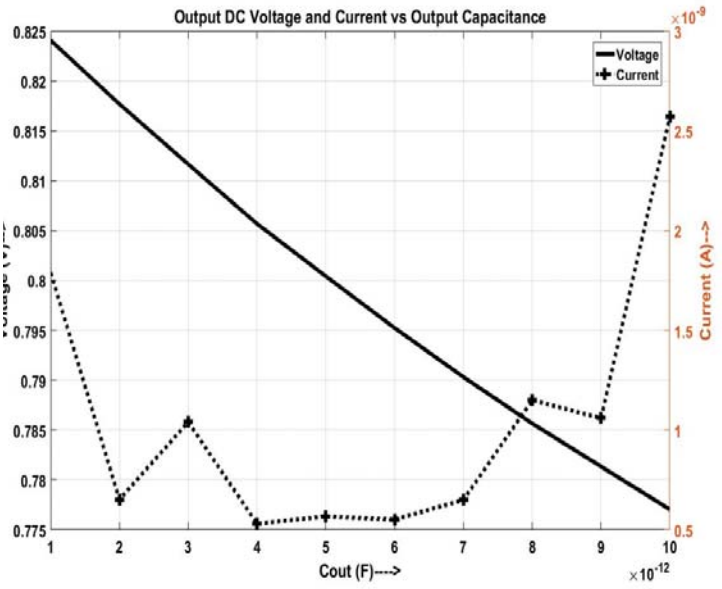

Figure 5: Output DC voltage and current vs C_{out}

As the sizing of the both the nMOS and pMOS will have an im pact on the output, hence th e output DC voltage and current value are plotted across length and width of both the devices. This is shown in Figs. 6, 7, 8 and 9.

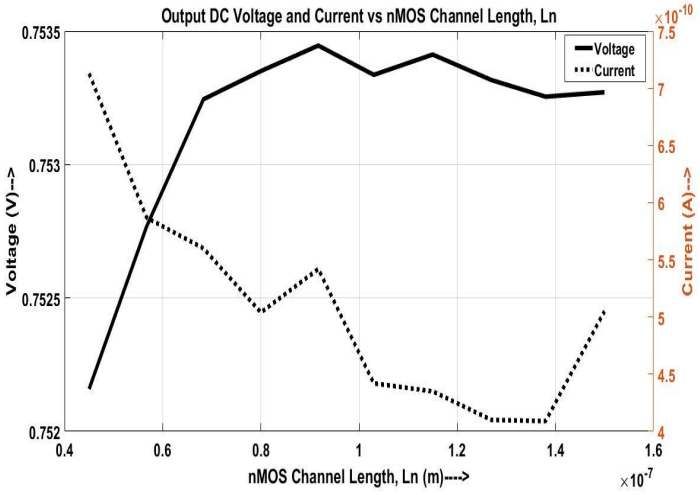

Figure 6: Output DC voltage and current vs L_n

Fig. 6 shown the output voltage and current wih respect to the nMOS channel length (L_n). Here the DC voltage is seen to increase while the current is in decline. This is expected as more channel length

increases channel resistance and decreases the current value. Similarly the output DC voltage and current is plotted across the nMOS width (W_n). Both the voltage and the current is seen to increase with the width. As broadening the device channel draws more current hence this nature is reflected here.

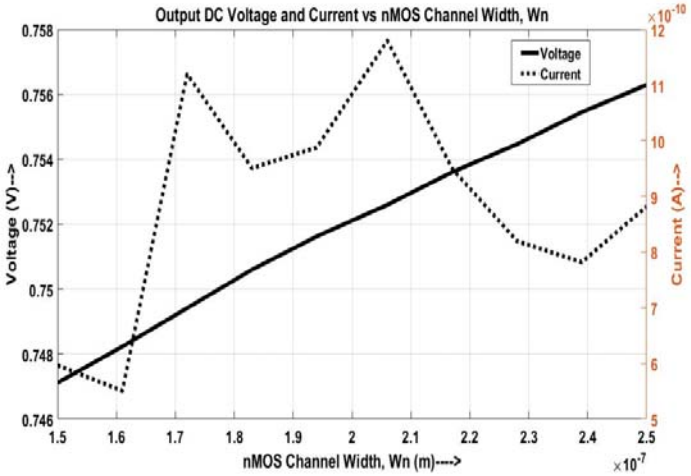

Figure 7: Output DC voltage and current vs W_n

The change in the output DC voltage and current across the pMOS channel length (L_p) and channel width (W_p) is depicted in Figs. 8 and 9. The DC voltage increases but the current decreases with L_p. While both the DC voltage and current increases with W_p.

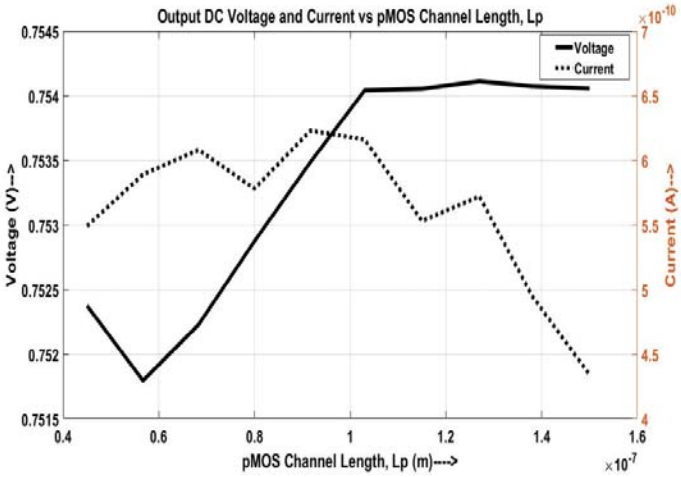

Figure 8: Output DC voltage and current vs L_p

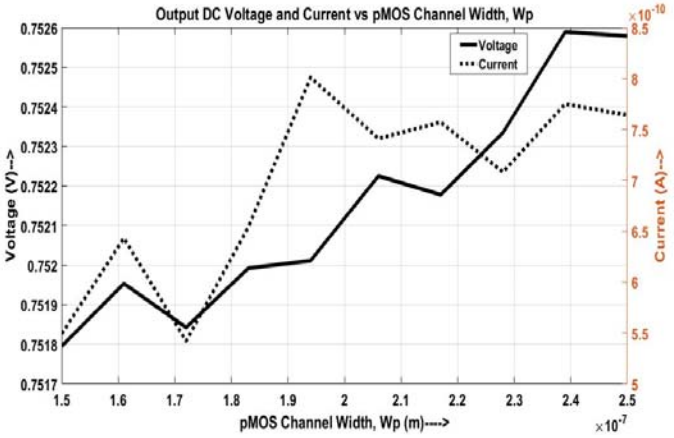

Figure 9: Output DC voltage and current vs W_p

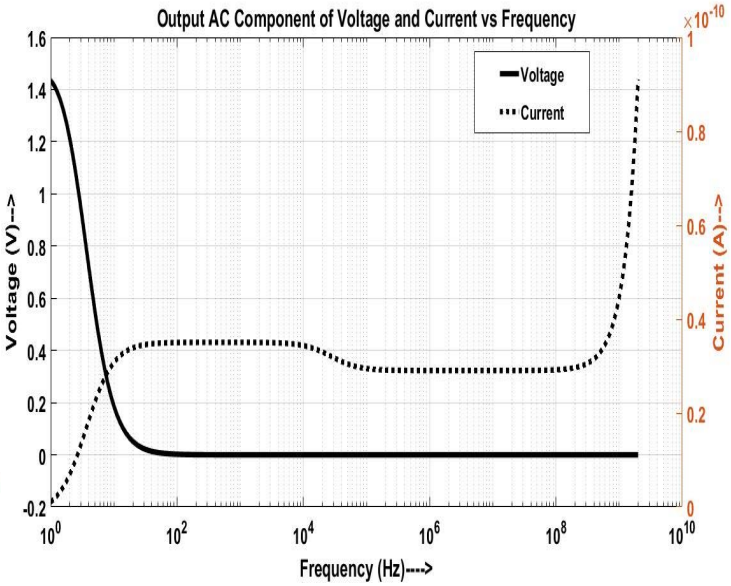

Figure 10: Output AC components of voltage and current vs frequency

The frequency response of the circuit is also simulated which clearly shows that the circuit is suitable to be operated at a wideband covering almost all popularly available commercial bands. The output AC component of voltage and current of the design with respect to frequency is presented in Fig. 10. It is seen that over a wide frequency range the AC components of output is negligible which proves its suitability for wideband operations.

Also the temperature profile of the circuits are evaluated which clearly indicates the temperature stability in terms of both voltage and current. This is shown in Fig. 11.

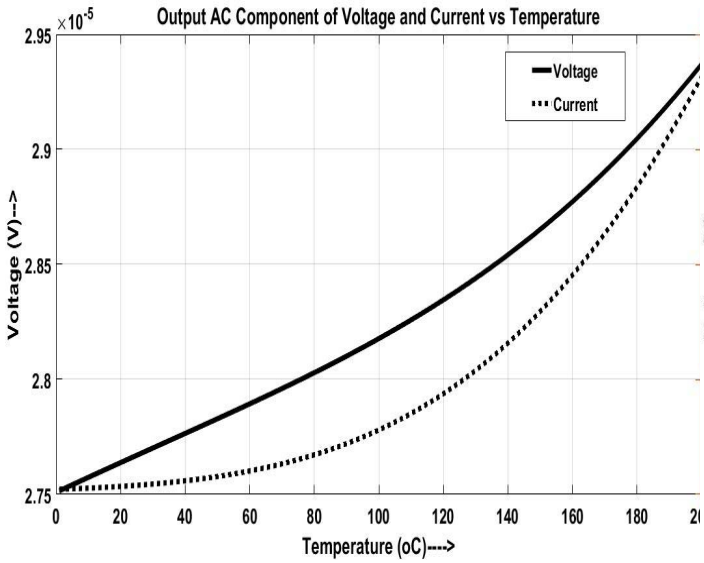

Figure 11: Output AC components of voltage and current vs Temperature

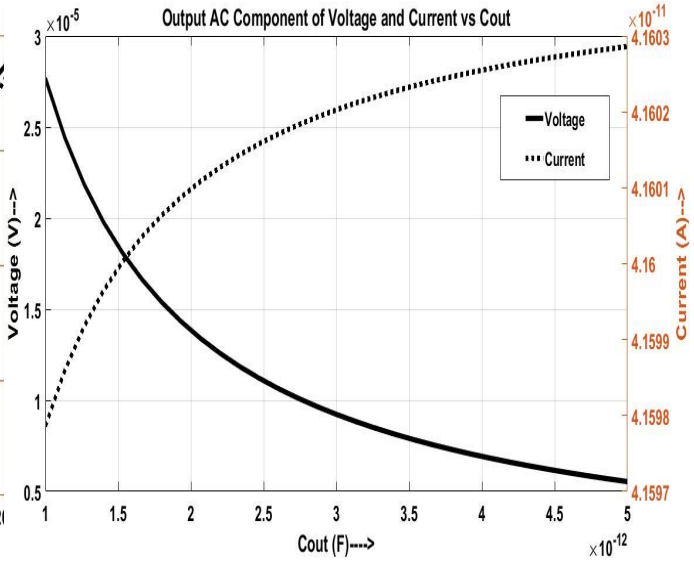

Figure 13: Output AC components of voltage and current vs C_{out}

The variation of output AC components of voltage and current with respect to input capacitance and output capacitance is also analyzed. Fig. 12 depicts the variation of output AC voltage and current with C_{in}, which indicates a minor change in both the parameter with increase in C_{in}. Also as the C_{out} increases, the AC component of voltage falls whereas the AC component of current marginally increases. This is presented in Fig. 13.

The output DC voltage and current with the change in the input power needs to be analysed and is presented in Fig. 14. This shows that both the voltage and current increases with increase in input power, which is expected as increase in input power would definitely increase the output power.

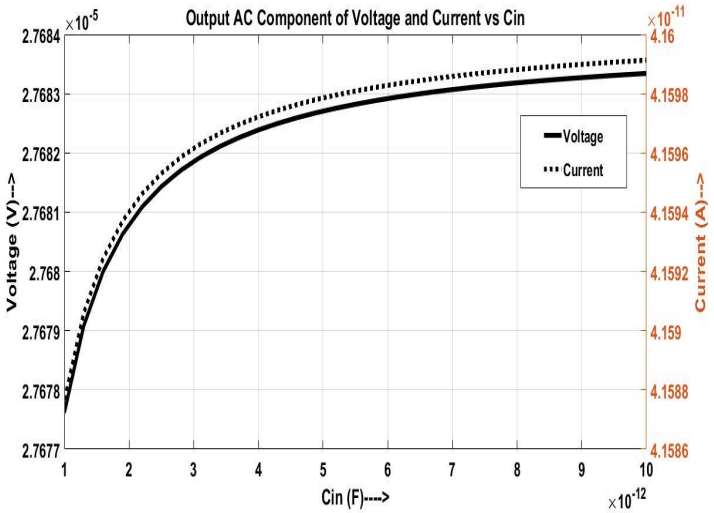

Figure 12: Output AC components of voltage and current vs C_{in}

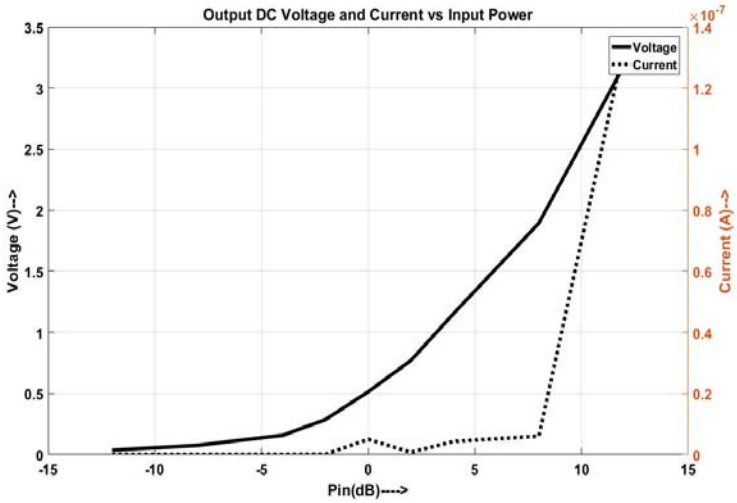

Figure 14: Output DC voltage and current vs P_{in}

As the PCE of the circuit is the major and significant performance parameter, it is evaluated and presented in Fig. 15. The PCE obtained are 90% and 85% at 2db and -2db respectively. For higher input power, power gain is also observed. This clearly shows the efficacy of the design particularly at low input power applications.

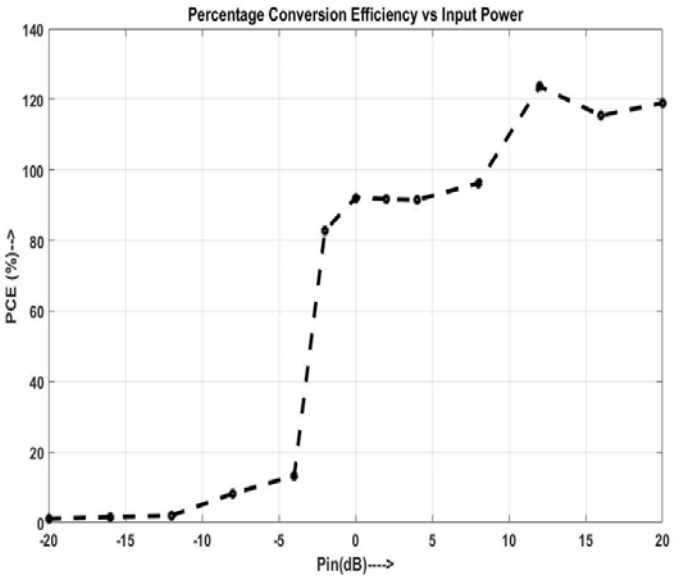

Figure 15: PCE vs P_{in} for the circuit

The DPD at -2dBm is plotted across the output voltage and is shown in Fig. 16. The instantaneous DPD is seen to change with the value of output voltage

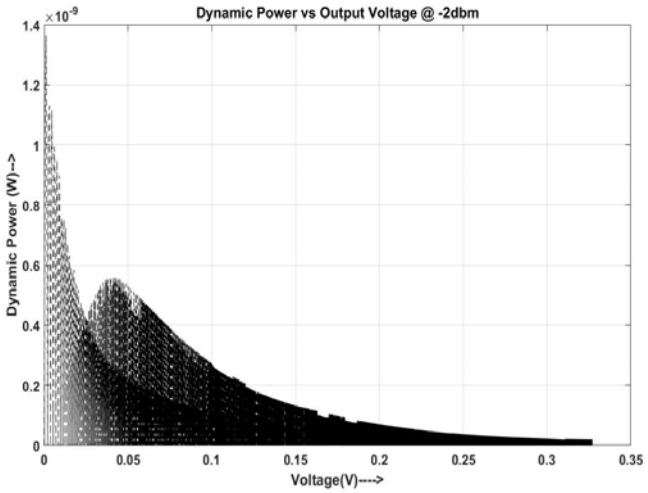

Figure 15: DPD vs output voltage at -2dbm

The key parameters of both the circuit are presented in Table 2. This shows that the design is capable to function at lower input power efficiently with significantly low power dissipation and zero leakage power. Though the single stage output DC voltage is less but this can easily be enhanced by having a cascaded structure. In[21] you will find some other studies about CMOS.

Table 2: Key parameters of the circuit

Parameters	Input Power	
	@2dB	@-2dB
O/P Voltage	823 mV	286mV
PCE	90%	85%
DPD	23.2pW	6.25pW
LP	0	0

The results obtained are compared with a few recently reported works. This clearly depicts that the designs presented here provides the best single class efficiency with minimum number of MOS devices. This is shown in Table 3.

Table 3: Comparative Analysis with recent works

Work	Comparison with the reported works					
	Technology	*Stage*	*Frequency (MHz)*	*Input Power (dbm)*	*Output Voltage (V)*	*Max PCE (%)*
[13]	Schottky Diode	1	868	10	-	48
[14]	Schottky Diode	1	900	-10	0.66	40
[15]	Schottky Diode	2	868	-10	0.649	44
[16]	Schottky Diode in 0.35 µm CMOS	5	900	-14.8	1.5	36
[17]	TSMC 0.18 µm	8	925	-21.2	0.78	43
[4]	0.18 µm CMOS	1, Diff	953	-12.5	0.62	67
[18]	TSMC 90 nm CMOS	5, Diff	868	-17	1.62	40
[19]	65 nm CMOS	5	900	18	6	31
[7]	65 nm CMOS	2	953	-15	0.402	56
[12]	45 nm CMOS	1	953	-2	0.485	80
This work	45 nm CMOS	1	953, 1800	-2	0.286	85

4 Conclusion

The 3-transistor rectifier presented here is a improved structure implemented with threshold voltage compensation technique, which can also be viewed as a simplification to the TG based design in [12]. This rectifier is also demonstrated to be suitable over a wide band of frequencies spanning almost all commercially available frequency bands. The PCEs achieved at 2db and -2dB are 90% and 85% respectively. By comparing with the recently reported works, it can be stated to be sufficiently

higher at low input power. This proves the efficacy of the design for low power RF energy harvesting and makes a potential candidate for facilitating self-sustainability to a communication system, particularly as part of a green communication set-up. As the circuit works successfully with only 3-transistors and only few components, hence the area efficiency can be said to be another striking feature of the design. This also makes the design a design cost-effective. The DPD and LP are also evaluated and presented in the Table 2, which shows that the circuit provides a significantly low DPD and zero LP. A significantly low DPD means the circuit is feasible to be implemented in a power aware set-up. Again a zero LP indicates almost zero power loss. Finally, the design can be said to be significant in considerations to the following parameters viz higher PCE at a low input power, wide frequency range compatibility, only 3 numbers of transistors, very low power dissipation and zero leakage power. This proposed concept of the design may be extended to make the system capable provide high PCE at even lower input power. The multistage implementation of the circuit can provide a higher output voltage, which is another required dimension to be explored.

References:

[1] S. Ulukus, A. Yener, E. Erkip, O. Simeone, M. Zorzi, P. Grover, and K. Huang, '*Energy Harvesting Wireless Communications: A Review of Recent Advances*', IEEE Journal of Selected Areas in Comm., vol.33, no.3, pp-360-381, 2015

[2] S. Sudevalayam and P. Kulkarni., "*Energy harvesting sensor nodes: Survey and implications*", IEEE Comm. Surveys Tutorials, vol.13, no. 3, pp-443–461,2011.

[3] J. Rabaey, M. J. Ammer, J. L. Silva, D. Patel, and S. Roundy. "*PicoRadio Supports Ad Hoc Ultra-Low Power Wireless Networking*", IEEE Computer, vol.33, pp-42–48, 2000.

[4] K. Kotani, A. Sasaki and T. Ito, "*High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs*", IEEE Jornal of Solid-State Circuits, vol. 44, no.11, 2009.

[5] M. L Matia et al, " *A comparision of High-Efficiency UHF RFID Rectifier Using Internal Voltage Compensation and Zero-Threshold-Voltage MOSFETs*", 2014 IEEE 5th Latin American Symposium on Circuits and Systems, 2014.

[6] H. Lin, H. Cao, Z. Chen, W. C. Chan, W. K. Lee and M. Zhang, " *Leakage Current Elimination for Dickson Charge Pump with a Linear Regulator*", ELSEVIER Microelectronics Journal, vol. 64, pp. 29-34, 2017.

[7] M. Taghdosi, L. Albasha, N. A. Quadir, Y. A. Rahama and N. Qaddoumi, "*High Efficiency Energy Harvesters in 65nm Process for Autonomous IoT Sensor Applications*", IEEE Access, vol. 6, pp-2397-2408, 2018.

[8] M. M. Mohamed et al., "*High-Efficiency CMOS RF-to-DC Rectifier Based on Dynamic Threshold Reduction Technique for Wireless Charging Applications*", IEEE Access, vol. 6, Pp-46826-46831, 2018.

[9] M. M. Mansour and H. Kanaya, "*High-Efficient Broadband CPW RF Rectifier for Wireless Energy Harvesting*", IEEE Microwave and Wireless Components Letters, vol: 29 , no: 4 , pp-288-290, 2019.

[10] S. Yuh Lee, Z. Xian Liao and C. Hung Lee, "*Energy-Harvesting Circuits With a High-EfficiencyRectifier and a Low Temperature Coefficient Bandgap Voltage Reference*", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 27, no. 8, pp-1760-1767, 2019.

[11] T. Oh, O. Hassan, S. Shamsir and S. K. Islam, "*Low-Power RF Energy Harvester Circuit Design for Wearable Medical Applications*", United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), USA, 2019.

[12] M. P. Sarma, K. K. Sarma, N. E Mastorakis, "*Design of a TG Based High Frequency Rectifier at 45 nm for RF Energy Harvesting Application*", 2nd IEEE European Conference on Electrical Engineering and Computer Science (EECS), pp-52-523, Athens, Greece, 20-22 Dec. 2018.

[13] D. Allane, G. A. Vera, Y. Duroc, R. Touhami, and S. Tedjini, '' *Harmonic Power Harvesting System for Passive RFID Sensor Tags*'', IEEE Transaction on Microwave Theory Technology, vol. 64, no. 7, pp. 2347–2356, Jul. 2016.

[14] D. Masotti, A. Costanzo, P. Francia, M. Filippi, and A. Romani, ''*A Load modulated rectifier for RF Micro-power Harvesting with Start-up Strategies*'', IEEE Transaction on Microwave Theory Technology, vol. 62, no. 4, pp. 994–1004, Apr. 2014.

[15] D. Assimonis, S.-N. Daskalakis, and A. Bletsas, ''*Sensitive and Efficient RF Harvesting Supply for Batteryless Backscatter Sensor Networks*'' IEEE Transaction on Microwave Theory Technology, vol. 64 , no. 4, pp. 1327–1338, Apr. 2016

[16] J. W. Lee and B. Lee, " *A Long-range UHF-band Passive RFID Tag IC Based on High-Q Design Approach*" IEEE Transactions on Industrial Electronics, vol. 56, no. 7, pp. 2308–2316, Jul. 2009.

[17] C.-Y. Yao and W.-C. Hsia, "*A–21.2 -dBm Dual-channel UHF Passive CMOS RFID Tag Design*", IEEE Transaction on Circuits and Sy stems I, Reg. Papers, vol. 6 1, no. 4, pp. 1269–1279, Apr. 2014

[18] M. Stoopm an, S. Key rouz, H. J . Visser, K. Philips, and W. A. Serdijn, " *Co-design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters*," IEEE Journal on Solid-State Circuits, vol. 49, no. 3,pp. 622–634, Mar. 2014

[19] C.-H. T sai, I.-N. Liao, C. Pakasiri, H.-C. Pan, and Y.-J. Wang, " *A Wideband 20 mW UHF Rectifier in CMOS*", IEEE Microwave and Wireless Component Letters.,vol. 25, no. 6, pp. 388–390, Jun. 2015.

[20] H. Kim and I. Kwon, "*Design of High-Efficiency CMOS Rectifier with Low Reverse Leakage for RF Energy Harvesting*", Electronics Letters, vol. 55 No. 8 pp. 446–448, 2019.

[21] Yogita Gajare, Arti Khaparde , Design and Simulation of First Order One Bit Sigma Delta ADC in 180nm CMOS Technology *WSEAS Transactions on Electronics,* pp.1-7, Vol.9, 2018