A Comparative Study of 6T and 8T SRAM Cell With Improved Read and Write Margins in 130 nm CMOS Technology

RAM MURTI RAWAT, VINOD KUMAR
Department of Computer Science and Engineering
Delhi Technological University
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Bawana Road, Delhi-110042
INDIA

Abstract: - This paper examines the factors that affect the Static Noise Margin (SNM) of a Static Random Access memories which focus on optimizing Read and Write operation of 8T SRAM cell which is better than 6T SRAM cell Using Swing Restoration for Dual Node Voltage. The read and Write time and improve Stability. New 8T SRAM technique on the circuit or architecture level is required. In this paper Comparative Analysis of 6T and 8T SRAM Cells with Improved Read and Write Margin is done for 130 nm Technology with Cadence Virtuoso schematics Tool.

Key-Words: - SRAM, Swing Restoration Logic, Dual Node Voltage, Low Power, Read and Write margin

Received: September 2, 2019 . Revised: January 24, 2020. Accepted: February 2, 2020. Published: February 10, 2020

1 Introduction

Low power Static Random Access Memories have become a critical component of many VLSI chips. This is especial consideration for microprocessors where the on chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory [P. Barnes 2010, S. Hesley, et.al, 2009]. one of the major issues in the design of an SRAM cell in stability. The cell stability determines the sensitivity of the memory to process tolerances and operating conditions.

The stability of Static Random access memory cell in the presence of DC noise is measured by the static noise margin (SNM). Static Noise Margin is the amount of voltage noise required at the output nodes to flip the state of the cell. This can be obtained using the voltage transfer characteristic (VTC) of the two cross coupled inverters of the SRAM cell [6].

Figure 1 illustrates the schematic of a 6 transistor SRAM cell for simulating the static noise margin. The sources Vn are the noise sources at the state nodes of the cell [6].

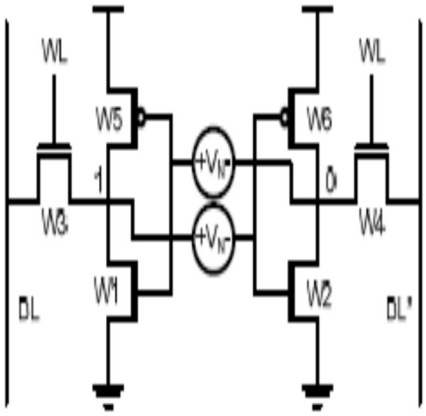

Fig.1 Schematic of a 6T SRAM bit cell with noise voltage sources for measuring SNM [6].

The cross-coupled inverters maintain a bi-stable state and their output nodes retain the data stored in the cell. However, as the noise Vn increases, the stability of the cell degrades because of the fluctuations at the node voltages. The Static Noise Margin quantifies the allowed levels of these noise voltages and thus the ability of these inverters to retain their state in the presence of noise.

The goal of this paper is to determine the effect of several circuit parameters on the SNM of the 6T SRAM cell designed in 180 nm CMOS process technology and compare it with the model derived in [6].

The SNM of the SRAM Cell When in standby or retain mode, read operation, and write operation. The SNM of the SRAM cell is obtained by plotting the VTCs of the Two cross-coupled inverters. The VTC of one of the inverters is flipped with respect to the line y = x in order to form a "butterfly curve". The SNM is the side of the smaller square that can be fitted inside the "eye" of the graph as shown in Figure1 [6].

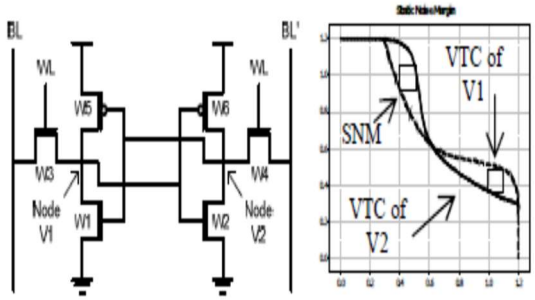

Fig.2 Schematic of a 6T SRAM bit cell and sample SNM-the side of the largest square fitted inside the graph [6].

This Paper is organized as follows: the characteristics of 6T SRAM cell are described are represented in section 2. In section 3, Proposed 8T SRAM cell is described. In section 4, Standard 8T SRAM cell is described. Section 5 includes the simulation results which give comparison of different parameters of 6T and 8T SRAM cells. section 6, DC analysis and section 7 conclusion the work.

2 Six Transistor SRAM Cell

In a conventional 6T SRAM cell, the data storage nodes are directly accessed through the bit-line access transistors during read operations, as shown in Fig.3. While reading, the storage node voltages are disturbed between cross-coupled inverter pair and bit lines. The BL and BLB are the bit lines and WL is the word line. The access transistors are controlled by WL (word line) to perform the operation of read and write operation. Bit lines act as input and output nodes. During a read operation, bit lines transfer the data from SRAM cells to a sense amplifier. Based on the technology the minimum length of the transistors is 180nm [1].

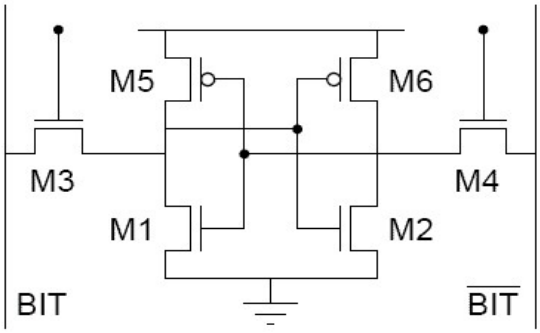

Fig.3 6T SRAM Cell [1].

3 Proposed 8T SRAM Cell

This is proposed SRAM, Dual Voltage with Swing Restoration Logic Perform node voltage in Hold, read and write operation and other parameters like Delay, Stability, are used in Fig.4. Comparison between Low power 6T SRAM and proposed 8T SRAM Cell designs is done. The comparison results revels that read, write and hold mode operation for 8T SRAM cell is better than 6T SRAM cell. This is because higher noise margin are obtained which ensure good write ability for the bit-cell [5].

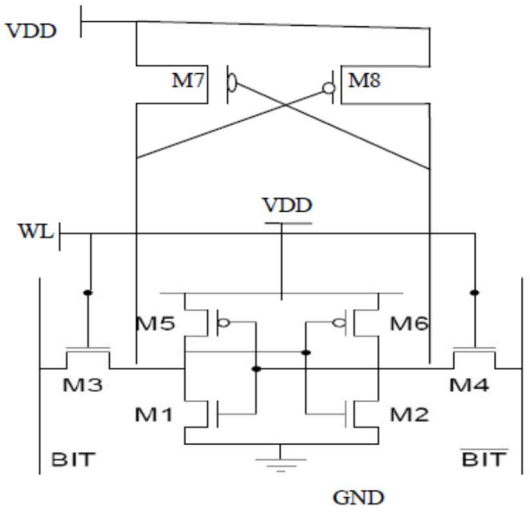

Fig.4 Proposed 8T SRAM Cell [5].

4 Standard 8T SRAM Cell

The standard 8T-SRAM Cell in shown in Fig.5. As it is Seen, read and write cycles use different wordlines and bitlines. Note that the standard 8T SRAM cell uses a single-ended read scheme which reduces the swing of bitlines. The 8T-SRAM cell

provides significantly improved RSNM (similar to Hold Static Noise Margin (HSNM) of the standard 6T-SRAM cell) with similar access time, write time, and write margin [7] [8].

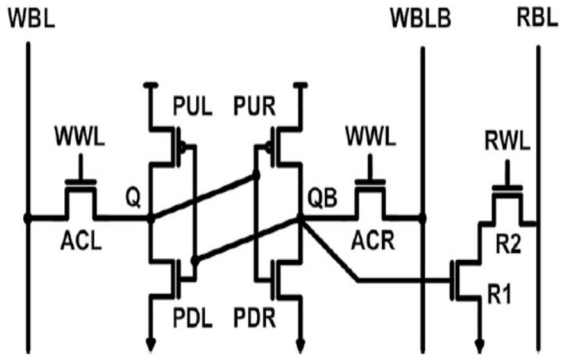

Fig.5 STANDARD 8T-SRAM CELL [7][8].

5 Simulation and Results

Analysis of proposed 8T SRAM cell in terms of write ability, read stability and hold static noise has been carried out in this section. These results are compared with standard 6T and 8T SRAM cell. The circuit is characterized by using the 130 nm Technology with the supply voltage of 1.2 volt.

5.1 Hold Stability

Static noise margin (SNM) is the most common approach to measure hold stability and read stability of the cell. Hold stability is calculated when the SRAM cell is in hold state.

In hold state the word lines are off, so the cell is totally disconnected from the bit lines. SNM defines the largest noise that can be imposed to the storage nodes before flipping the content of the cell. Fig.6, 7 and 8 shows the hold static noise margin of 6T, Proposed 8T and standard 8T SRAM cells respectively.

5.2 Read Stability

The Read stability is measured by read static noise margin (RSNM) in SRAM Cell. In the proposed 8T SRAM cell due to storing nodes isolation we get better RSNM comparable to conventional 6T SRAM and standard 8T SRAM Cells. Fig. 9, 10 and 11 represents the read stability of 6T SRAM and proposed 8T and standard 8T SRAM cells respectively.

5.3 Write Stability

The Write stability is measured by write static noise margin (WSNM). In the proposed 8T SRAM cell due to storing nodes isolation we get better WSNM comparable to conventional 6T SRAM and standard 8T SRAM Cells. Fig. 12, 13 and 14 represents the write stability of 6T SRAM and proposed 8T and standard 8T SRAM cells respectively.

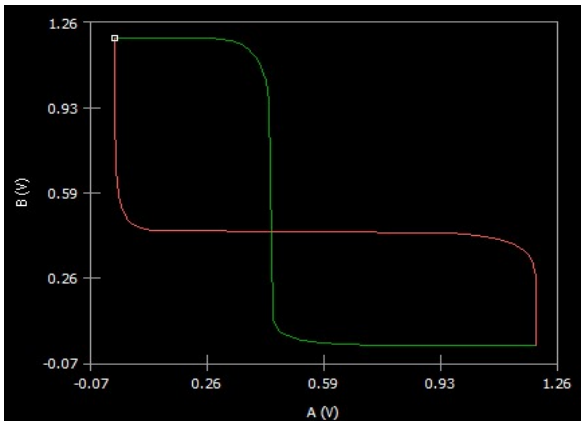

Fig.6 HSNM 6T SRAM CELL

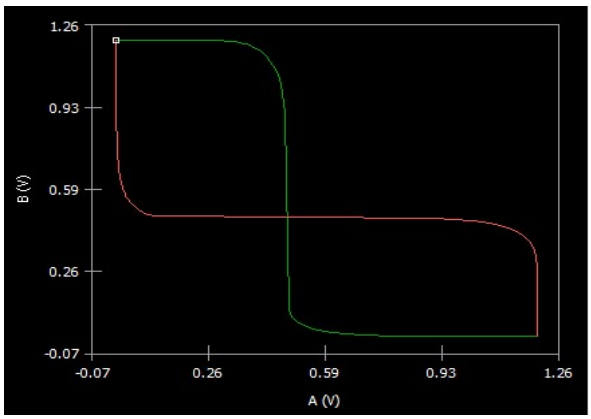

Fig.7 HSNM PROPOSED 8T SRAM CELL

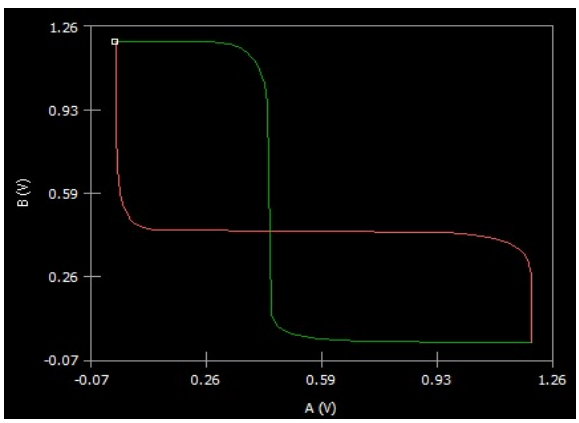

Fig.8 HSNM STANDARD 8T SRAM CELL

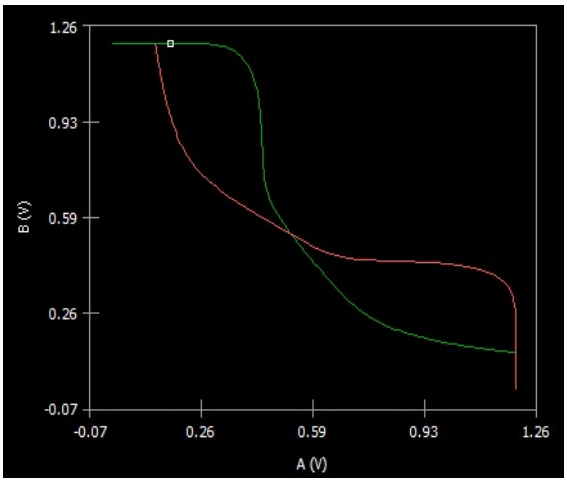

Fig.9 RSNM 6T SRAM CELL

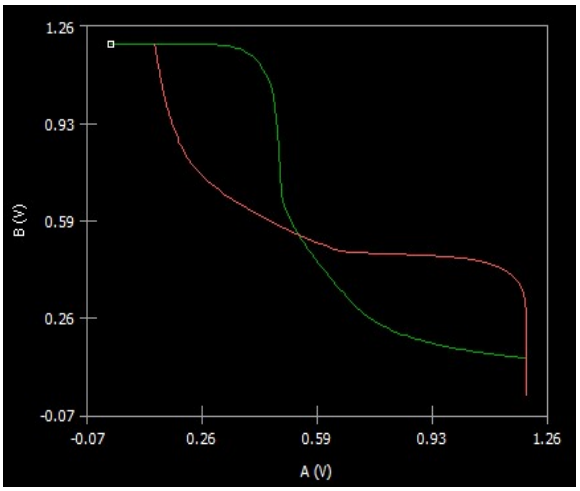

Fig.10 RSNM PROPOSED 8T SRAM CELL

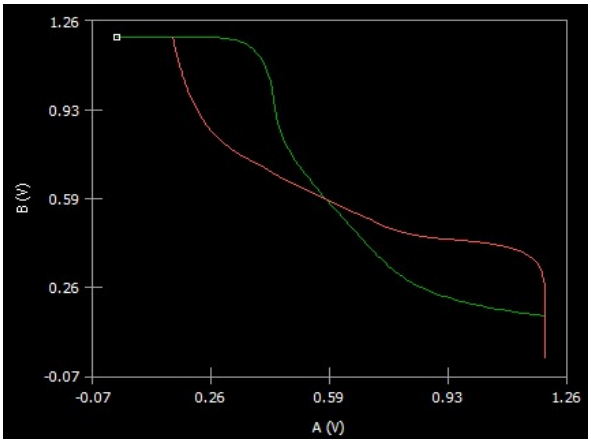

Fig.11 RSNM STANDARD 8T SRAM CELL

5.3.1 Write Trip Point

Write trip point is the measure of write ability of the cell. It shows how difficult it is to the storing nodes of the cell.

The bit-line voltage is swept from 0 to Vdd, and the flipping of the cell, when Q and Q bar flip their their content is captured. The value of bit-line voltage at the crossing point of internal storage nodes Q and QB bar represents write trip point.

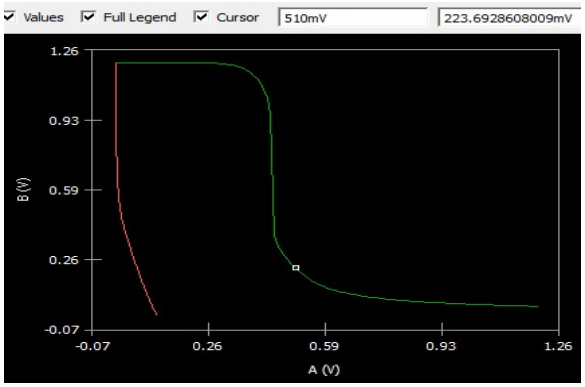

Fig.12 6T SRAM Write Trip Point

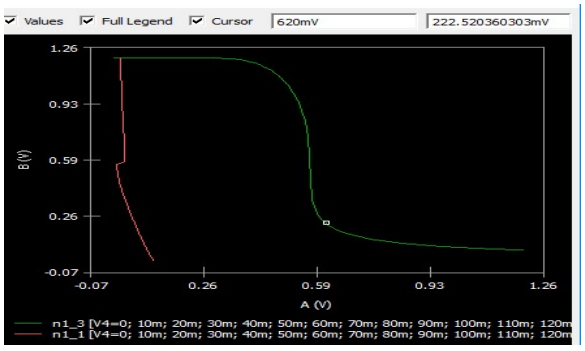

Fig.13 PROPOSED 8T SRAM Write Trip Point

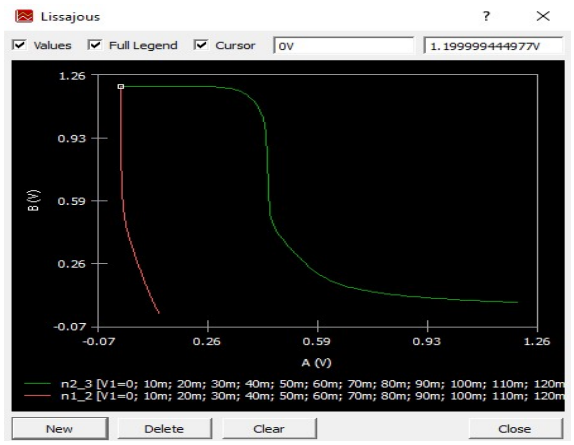

Fig.14 STANDARD 8T SRAM Write Trip Point

6 D.C. Analysis

6.1 Six Transistor SRAM Cell

6.1.1 Six Transistor SRAM Cell Output

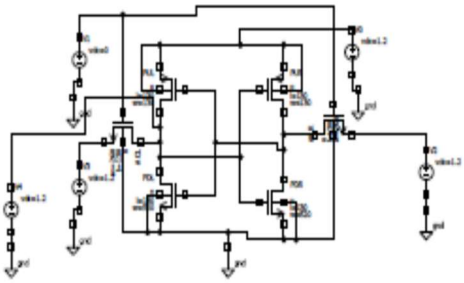

Fig.15 6T SRAM Cell

6.1.2 Six Transistor SRAM Cell DC Analysis

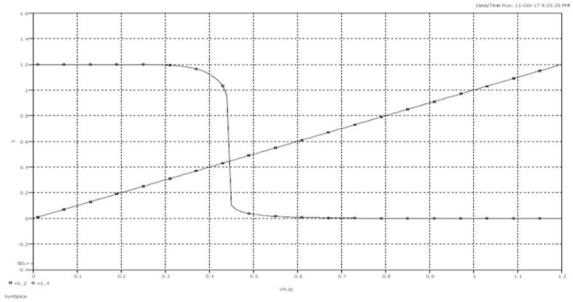

Fig.16 6T SRAM Cell DC Analysis

6.2 Proposed Eight Transistor SRAM Cell

6.2.1 Proposed Eight Transistor SRAM Cell Output

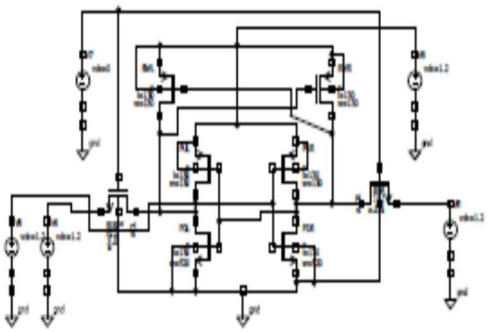

Fig.17 PROPOSED 8T SRAM Cell

6.2.2 Proposed Eight Transistor SRAM Cell DC Analysis

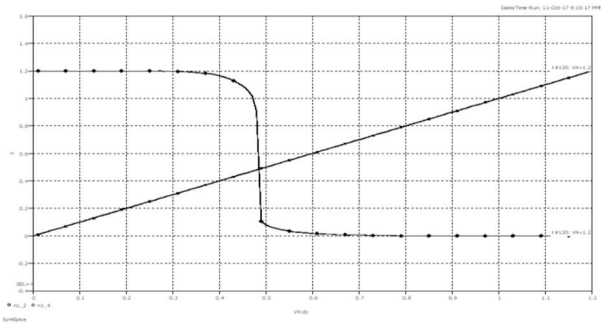

Fig. 18 PROPOSED 8T SRAM CELL DC Analysis

6.3 Standard Eight Transistor SRAM Cell

6.3.1 Standard Eight Transistor SRAM Cell Output

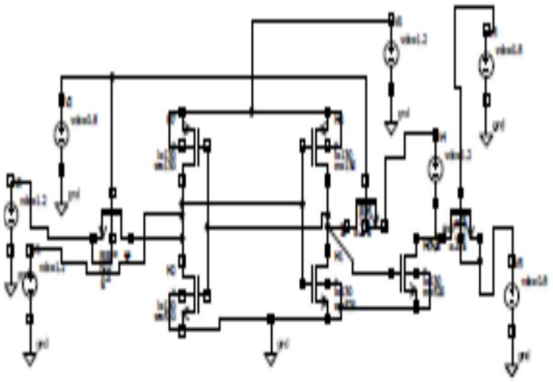

Fig.19 STANDARD 8T SRAM CELL

6.3.2 Standard Eight Transistor SRAM Cell DC Analysis

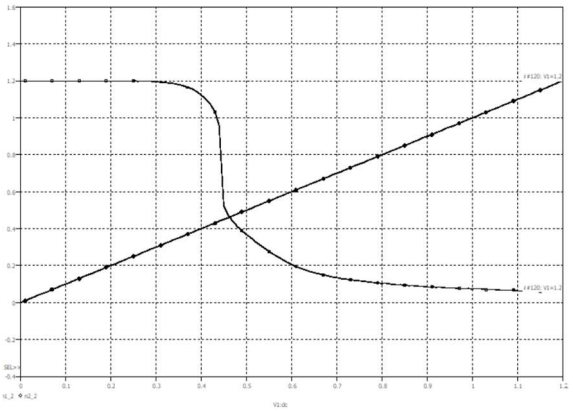

Fig.20 STANDARD 8T SRAM CELL DC Analysis

7 Conclusion

A low power and swing node restoration Static Random Access memory logic circuit technique is presented in the paper. In this paper comparative analysis of 6T and 8T SRAM cells in 130 nm Technology is also presented.

This is the proposed SRAM cell and Dual node voltage with Swing Restoration logic perform D.C. analysis Hold mode operation. D.C. analysis HOLD operation good noise margin proposed 8T SRAM cell is better than 6T SRAM and STANDARD 8T SRAM Cells.

This conclusion is good for power consumption is low. Then PROPOSED 8T SRAM Cell Write mode is power analysis is better Then 6T SRAM and STANDARD 8T SRAM Cells. Then speed is higher for proposed 8T SRAM Cell.

References:

[1] Seevinck, "Static-Noise Margin Analysis of MOS SRAM Cells,"IEEE Journal of Solid-State Circuits, SC-22,5 (Oct. 1987),748-754.
[2] H.L. yeger et al, "Domino circuit Topology", U.S. Patent 6784695, Aug. 31,2004.
[3] A.S. Sedra and K.C. Smith Microelectronic circuits, Fourth Edition, new York: oxford,1988.
[4] S.M. Kang and Leblebici, CMOS Digital Integrated circuits, Analysis and Design, Second Edition, Mc Graw-Hill,1999.
[5] R. M. Rawat, A Novel Low power and Swing Restoration SRAM Logic Circuit Technique, March 2018, International Journal of Engineering and Technical Research V7(02).
[6] A. Pavlov and Manoj sachdev, CMOS SRAM Circuit Design and parametric Test in Nano-scaled Technologies. Springer 2008.
[7] Calhoun, B.H., Chandrakasan, A.P.: Static noise margin variation for sub-threshold SRAM in 65 nm CMOS. IEEE J. Solid-state Circuits 41, 1673-1679 (2006).
[8] Farshad , 8T-SRAM Cell with improved read and write margins in 65 nm CMOS Technology,IFIP AICT 464,PP.95-109,2015.
[9] Sedra/ Smith, Microelectronic Circuit, chapter 15, 6th edition.
[10] Wai-Kai-Chen, Memory, Microprocessor an ASIC, 2003.
[11] Tegze P. Haraszti, CMOS Memory Circuits, Kluwer Publication, 2002.
[12] David Money Harris & Sarah L. Harris, Digital Design and Computer Architecture.
[13] Mohammed Sharifkhani, Design and Analysis of low power Sram, thesis report, Waterloo University, Canada.
[14] Prof. Etienna Sicard and Asst Prof. Sonia Delmas Bendhia, INSA Electronic Engineering School of Toulouse, France, Advanced CMOS Cell Design.
[15] Randall L. Geiger, Phillip E. Allen and Noel R. Strider, VLSI Design Techniques for Analog and Digital Circuits.
[16] R. Jacob Baker, Harry W. Li and David E. Boyce, CMOS Circuit Design, Layout and Simulation.
[17] Neil Weste, CMOS VLSI Design: A Circuit and System Perspective, International Edition.