Modeling and Analysis of Battery Discharge Regulator used in Satellites

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Abstract: - Avionics battery discharge regulator which derives power from battery and delivers power to load plays an important role in power conditioning unit. With the merits of high efficiency, stable transfer function and continuous input and output current, non-isolated weinberg converter is suitable for avionics battery discharge regulator. Improved peak current control strategy is put forward in order to achieve high current sharing accuracy and reliability. Based on the small signal model of three-module non-isolated weinberg converter system, the current and voltage controllers are designed. The system with the designed controllers operates stably in any operating conditions and achieves an excellent transient response and current sharing accuracy.

Key-Words: - Weinberg, BDR, Modeling, Peak-current mode control, Current sharing

1 Introduction

Power conditioning unit (PCU) is used to balance the power among each unit and keep the bus voltage constant. According to the bus voltage, PCU is separated into three categories: 28V, 42V and 100V. Avionics battery discharge regulator (BDR) which discharges power from battery and delivers power to load plays an important role in PCU. Non-isolated weinberg converter (NIWC) is suitable for battery discharge regulator due to the merits of high efficiency, no RHP zeroes and continuous input and output current.

For the past few years, many scholars have done research on NIWC. Lei has deduced the small signal model of NIWC[1-2]. Ejea-Marti J established small signal model based on peak current control and analyzed the stability under small duty cycle[3-5]. However, small signal model and controller design method of parallel NIWC system haven't been analyzed.

In order to achieve high current sharing accuracy and reliability, this paper proposed improved peak current control strategy. Based on the 42V-level PCU, small signal model and controller design method of three-module NIWC system under current continuous mode (CCM) are proposed in this paper.

2 Operating Principle

The NIWC is shown in Fig.1. By controlling Q_1 and Q_2 properly, couple inductor L_{couple} and

transformer T make the input and output current continuous. The input damping filter which consists of L_f, C_{f1}, C_{f2}, and R_f smoothes the input current, which makes current sampling convenient and the battery service life long. Maset E. have introduced the operating principle of NIWC[6-7].
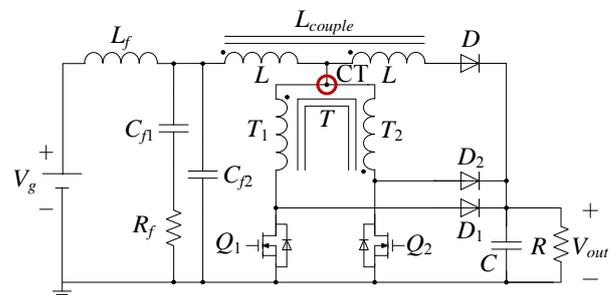
Fig. 1 Non-isolated Weinberg Converter (NIWC)
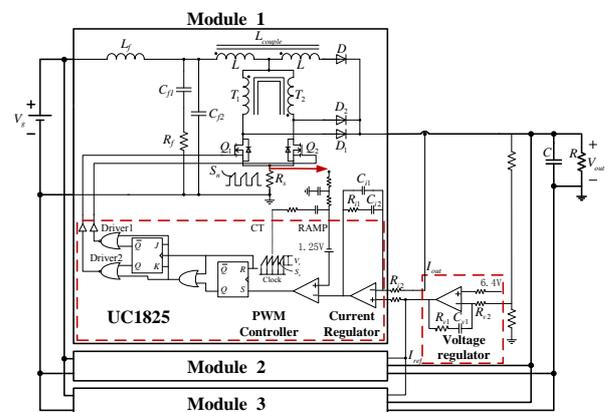
Fig. 2 Three-module NIWC system under peak current control

Considering the efficiency and reliability, three NIWCs in parallel supply power to main bus at rated condition 1200W. The control strategy should keep the bus voltage constant at 42V and the current sharing error lower than 1%.

Control diagram of three-module NIWC system is shown in Fig. 2. In order to avoid the saturation of the transformer and enhance the current sharing accuracy and reliability, improved peak current control strategy which contains voltage loop, average current loop and peak current loop is proposed. The voltage loop whose output is the reference of average current loop stabilizes the bus voltage. The average current loop enhances current sharing accuracy significantly. Improved peak current control strategy is suitable for the system-level applications which focus on the current sharing accuracy and integrity.

3 Power Stage Model

The input filter which is designed according to middlebrook theorem can be neglected in small signal model[8]. According to the state space averaging method, The power stage model of three-module NIWC system can be easily established, as shown in Fig.3. Supposing the duty cycle disturbance of each module is equal, the inductor is divided by three, which is different from power stage model of single-module[9]. From Fig.3, the transfer functions are obtained. It should be noted that the power stage model is based on the current continuous mode (CCM).

$$
\begin{cases}
G_{ig}(s) = \dfrac{\hat{i}_{out}(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0} = \dfrac{(1+D)(sC+1/R)}{4LCs^2/3 + 4Ls/3R + 1} \\[4mm]
G_{vd}(s) = \dfrac{\hat{v}_{out}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0} = \dfrac{V_g}{4CLs^2/3 + 4Ls/3R + 1} \\[4mm]
G_{id}(s) = \dfrac{\hat{i}_{out}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0} = \dfrac{V_g(RCs+1)}{4RLCs^2/3 + 4Ls/3 + R} \\[4mm]
G_{vg}(s) = \dfrac{\hat{v}_{out}(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0} = \dfrac{1+D}{4CLs^2/3 + 4Ls/3R + 1}
\end{cases}
\quad (1)
$$
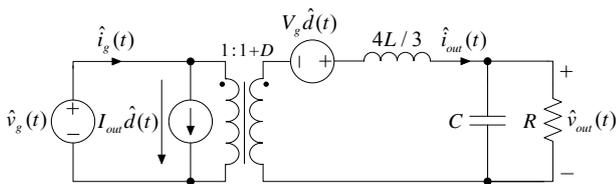
Fig. 3 Power stage model of three-module NIWC system

Three-module NIWC system is equivalent as buck converter whose inductance is 4L/3 in view of transfer function $G_{vd}(s)$. So NIWC is easy to design . because the transfer functions don't have RHP zeroes.

4 Small Signal Model Of System

The disturbance of duty cycle $\hat{d}(t)$ can be expressed by [10]

$$
\hat{d}(t) = F_m[\hat{i}_c(t) - \hat{i}_{out}(t) - F_g \hat{v}_g(t) - F_v \hat{v}_{out}(t)] \quad (2)
$$

Where $F_m = 1/M_a T_s$, $F_g = (D^2 + 2D - 1)T_s/8L$, $F_v = (1-2D)T_s/8L$. $\hat{i}_c(t)$ is control current, D is the sum of the duty circle of Q_1 and Q_2, T_s is half of the period of Q_1. M_a is the slope of the saw-tooth wave which is used for slope compensation.

According to Eq.2, the small signal model of three-module NIWC system is proposed in Fig.4. The sampling coefficients of peak current and average current are divided by three, which is different from small signal model of single-module. F_g and F_v can be neglected due to the small current ripple and $\hat{v}_{in}(t)$ also can be neglected. With this simplification, small signal model of the system is constructed in Fig.5.
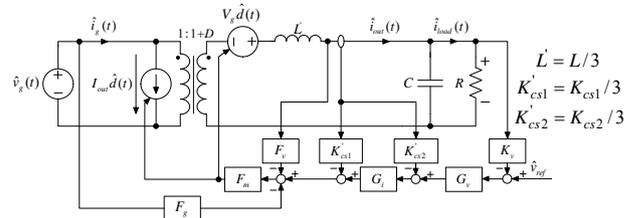
Fig. 4 Small signal model of three-module NIWC system
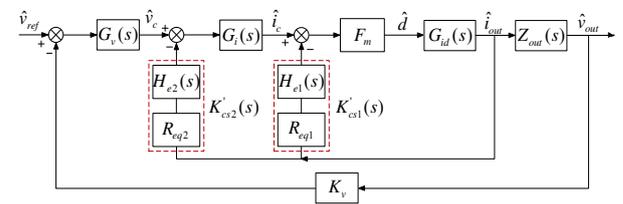
Fig. 5 Modified small signal model of the system

The transfer functions indicated in Fig.5 are defined as follows:

$G_v(s)$: error amplifier of voltage loop
$G_i(s)$: error amplifier of average current loop
R_{eq1}: sampling coefficient of peak current
R_{eq2}: sampling coefficient of average current
$K_v(s)$: sampling coefficient of output voltage

F_m: current modulator gain

$G_{id}(s)$: transfer function of $\hat{i}_{out}(s)$ to $\hat{d}(s)$

$Z_{out}(s)$: output impedance function

$H_{e1}(s)$: transfer function describing the sampled-data effect for peak current

$H_{e2}(s)$: transfer function describing the sampled-data effect for average current

The time delay and disability at half of the equivalent efficiency reflect in small signal model by introducing $H_{e1}(s)$ and $H_{e2}(s)$ [11].

$$H_{e1}(s) = H_{e2}(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \qquad (3)$$

Where $\omega_n = \pi / T_s$, $Q_z = -2 / \pi$.

5 Converter Design

The controller should be designed to satisfy the performance requirements as follows:

- Gain margin is higher than 10dB,
- Phase margin is higher than 60°,
- Close-loop output impedance is lower than 50mΩ.

When input voltage is 26V and output current is 30A, the controller is harder to design than other conditions, so the controller is designed under this condition. Specifications of the system are described in Tab.1.

Tab.1 System parameters

Input voltage(V_{in})	26V~38V
Output current (I_{out})	0A~30A
Output voltage (V_{out})	42V
Switching frequency (f)	100kHz
Output capacitor (C)	2mF
Self inductance of couple inductor (L)	20uH
sampling coefficient of output voltage (K_v)	6.4/42
sampling coefficient of average current (R_{eq2})	0.0587
sampling coefficient of peak current (R_{eq1})	0.333

5.1 Current Controller Design

The control object of average current loop is

$$A_{peak}(s) = \frac{\hat{i}_{out}}{\hat{i}_c} = \frac{F_m G_{id}(s)}{1 + F_m G_{id}(s) K_{cs1}'(s)} \qquad (4)$$

The loop gain of average current loop is

$$T_i(s) = G_i(s) A_{peak}(s) K_{cs2}'(s) \qquad (5)$$

The uncompensated loop gain of current loop $T_{io}(s)$ with unity compensator gain $G_i(s)$ is depicted in Fig.6, from which it can be seen that the cut-off frequency is 19.4 kHz, the gain margin is 9.9dB and the phase margin is 92.1°. The DC gain of $T_{io}(s)$ at low frequency isn't high enough to reduce the stable error, so a low-frequency zero should be added to enhance the DC gain. $|T_{io}(j\omega)|_{dB}$ at high frequencies is higher than 0, which will amplify the high-frequency noise. So high-frequency zeros should be added to improve the anti-interference ability. Based on the analysis above, single zero double poles compensator is chosen as current regulator. The current regulator, represented in Fig.2, is

$$G_i(s) = \frac{K_i(1 + s / \omega_{zi})}{s(1 + s / \omega_{pi})} \qquad (6)$$

Where $K_i = 1 / R_{i2}(C_{i1} + C_{i2})$, $\omega_{zi} = 1 / R_{i1} C_{i2}$, $\omega_{pi} = (C_{i1} + C_{i2}) / R_{i1} C_{i1} C_{i2}$.

The parameters are $R_{i1} = 8k\Omega$, $R_{i2} = 10k\Omega$, $C_{i1} = 240pF$, $C_{i2} = 50nF$.

The compensated loop gain of current loop $T_i(s)$ is also shown in Fig.6. For $T_i(s)$, the cut-off frequency is 14.45kHz, the gain margin is 12.3dB and the phase margin is 91.5°.

5.2 Voltage Controller Design

The control object of voltage loop is

$$A_i(s) = \frac{\hat{v}_{out}}{\hat{v}_c} = \frac{G_i(s) A_{peak}(s) Z_{out}(s)}{1 + G_i(s) A_{peak}(s) K_{cs2}'(s)} \qquad (7)$$

The loop gain of voltage loop is

$$T_v(s) = G_v(s) A_i(s) K_v \qquad (8)$$

The uncompensated loop gain of voltage loop $T_{vo}(s)$ with unity compensator gain $G_v(s)$ is depicted in Fig.7. In order to satisfy that the cut-off frequency of the voltage loop should be lower than that of current loop, the cut-off frequency of $T_v(s)$ is designed to be 1kHz. In Fig.7, the Amplitude-frequency Curve of $T_{vo}(s)$ is lower than 0dB, which means that the system is unstable. In order to enhance the DC gain and stability, single zero single pole compensator is chosen as voltage regulator. The voltage regulator, represented in Fig.2, is

$$G_v(s) = \frac{K_v(1 + s / \omega_{zv})}{s} \qquad (9)$$

Where $K_v = 1/R_{v2}C_{v1}$, $\omega_{zv} = 1/R_{v1}C_{v1}$.

The gain of $T_{vo}(s)$ at 1kHz is -25.5dB. The cut-off frequency of $T_v(s)$ is designed to be 1kHz, so $20\log(|R_{v1}/R_{v2}|)=25.5$dB. If $R_{v2}=10$ $k\Omega$, then $R_{v1}\approx300$ $k\Omega$. The zero frequency of voltage regulator is designed to be 100Hz, so $C_{v1}\approx5.4$ nF.

The compensated loop gain of voltage loop $T_v(s)$ is also shown in Fig.7. For $T_v(s)$, the cut-off frequency is 1kHz, the gain margin is 35.5dB and the phase margin is 84.7°, which satisfies the requirements.
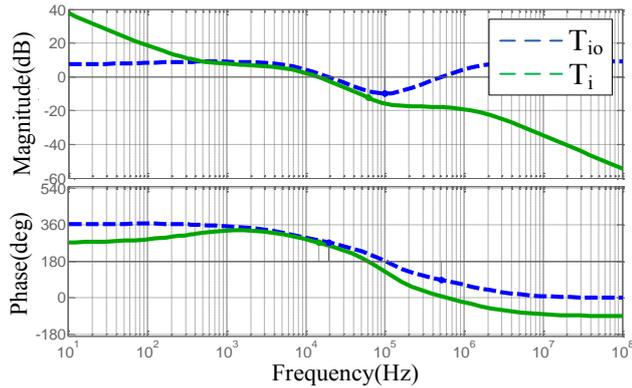
Fig. 6 Bode plot of current loop gain $T_i(s)$ and $T_{io}(s)$
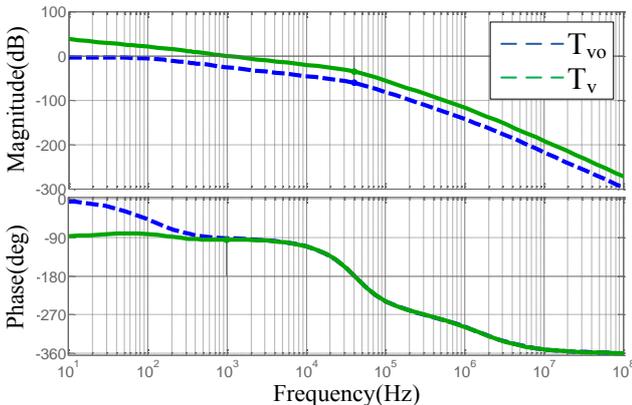
Fig. 7 Bode plot of voltage loop gain T_v(s) and T_{vo}(s)

5.3 Analysis of Closed-loop output impedance
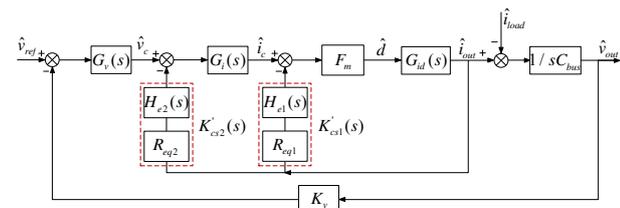
Fig. 8 The system small signal model of output impedance
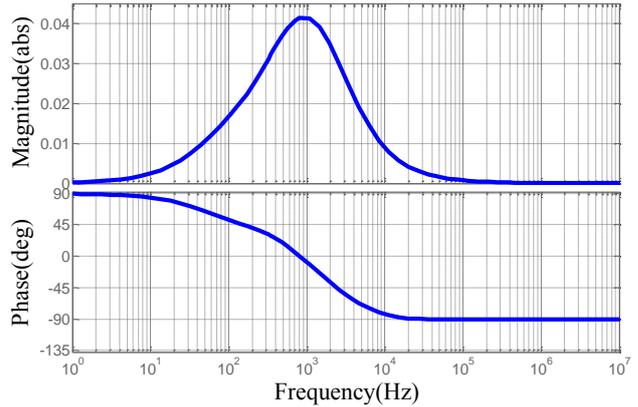
Fig. 9 Bode plot of output impedance

By introducing the disturbance of load current $\hat{i}_{load}(s)$, the small signal model of close-loop output impedance is shown in Fig.8. The transfer function of close-loop output impedance is

$$Z_{out}(s) = -\frac{\hat{v}_{out}(s)}{\hat{i}_{load}(s)}$$

$$= \frac{\dfrac{1}{C_{bus}s}}{1+\dfrac{K_vG_v(s)G_i(s)F_mG_{id}(s)}{C_{bus}s(1+F_mG_{id}(s)K'_{cs1}(s)+G_i(s)F_mG_{id}(s)K'_{cs2}(s))}}$$

(10)

In Fig.9, the maximum output impedance is 41.4$m\Omega$, which satisfies the requirements. So NIWC has good load adjustment rate.

6 Experimental Confirmation

Fig.10 Experimental platform of three-module NIWC system

A 1200W prototype has been built based on a 2 layer power PCB to confirm the superiority of improved peak current control strategy and the rationality of controller design, as shown in Fig.10.

Fig.11 shows drive signal, voltage of CT, DS voltage of MOSFET and primary current of couple

inductor when the input voltage is 32V. Under any conditions, the bus voltage is stable at 42V.
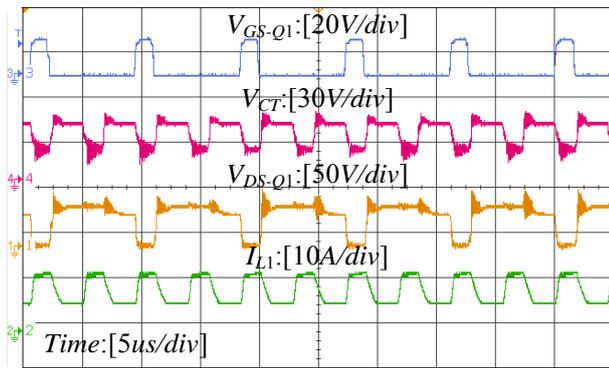
Fig.11 Key waveforms of NIWC

When the input voltage is 32V, Tab.2 represents the current sharing performance without current sharing strategy, table 3 shows the current sharing performance with peak current control strategy and table 4 exhibits the current sharing performance with improved peak current control strategy. The current sharing error is calculated according to Eq.11.

$$CS_{error}\% = \frac{\max[abs(I_i - \sum_{k=1}^{n} I_k / n)]}{\sum_{k=1}^{n} I_k / n} \qquad (11)$$

Where $\sum_{k=1}^{n} I_k / n$ is the average output current, $\max[abs(I_i - \sum_{k=1}^{n} I_k / n)]$ is the maximum difference between the output current of each module and average output current.

Tab.2 Current sharing performance without current sharing control strategy

$I_1(A)$	$I_2(A)$	$I_3(A)$	$CS_{error}\%$
2.892	1.851	1.228	45.3%
5.123	3.376	2.595	38.5%
6.983	5.345	3.681	31.02%
8.565	7.252	5.248	25.25%
10.372	8.651	6.985	19.64%
11.389	9.475	8.152	17.75%

Tab.3 Current sharing performance with peak current control strategy

$I_1(A)$	$I_2(A)$	$I_3(A)$	$CS_{error}\%$
2.332	2.023	1.679	16.52%
3.921	3.825	3.291	10.55%
5.875	5.328	4.805	10.1%
7.561	6.936	6.484	8.11%
9.413	8.541	8.174	8.08%
10.353	9.451	9.212	7.04%

Tab.4 Current sharing performance with improved peak current control strategy

$I_1(A)$	$I_2(A)$	$I_3(A)$	$CS_{error}\%$
2.018	2.003	1.999	0.56%
3.682	3.651	3.687	0.608%
5.371	5.323	5.316	0.643%
7.031	7.015	6.934	0.848%
8.701	8.674	8.645	0.327%
9.69	9.665	9.641	0.255%

From Tab.2, 3, and 4, the conclusions can be drawn as:
- The current sharing performance without current sharing strategy is the worst.
- The current sharing performance with peak current control strategy is better, but still can't satisfy the command 1%.
- The current sharing performance with improved peak current control strategy satisfies the command 1% under any conditions.

The conclusions above demonstrate the superiority of improved peak current control strategy.
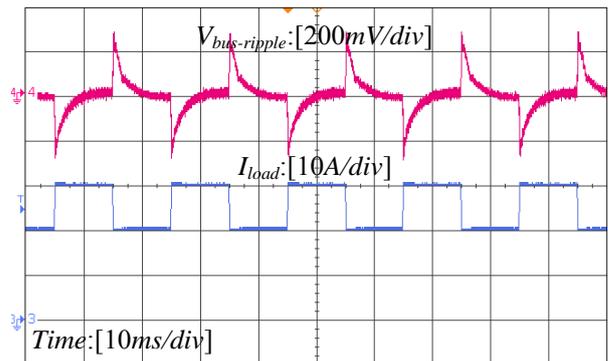
Fig.12 Transient response for load changes from 20A to 30A

Fig. 12 shows the transient response of the output voltage when the load changes 10A (20A to 30A). The output voltage approaches to normal in about 6.2ms with a little overshoot, and the peak-to-peak ripple of output voltage is 0.57V. Fig. 13 shows the transient response of the output current for each module when the load changes 10A (20A to 30A).

From Fig.12 and Fig.13, we can find that the system gains an excellent transient response and current sharing accuracy under improved peak current control strategy.
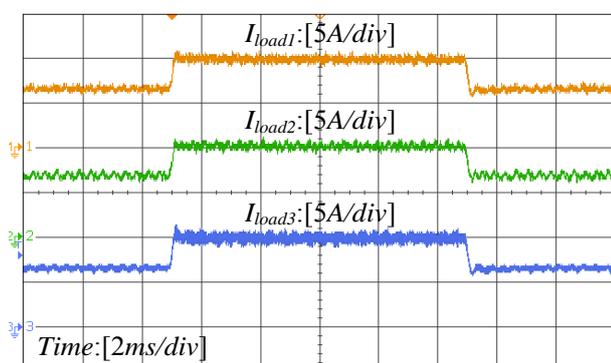
Fig.13 Transient current sharing performance for load changes from 20A to 30A

7 Conclusion

Based on three-module NIWC system, the power stage model is deduced. Improved peak current control strategy is employed to avoid the saturation of the transformer and enhance the current sharing accuracy and reliability. The current and voltage controllers are designed on the small signal model. Finally, The experimental results are given to verify that the system gains an excellent transient response and current sharing accuracy under improved peak current control strategy by a 1200W prototype. The current sharing strategy is suitable for the system-level application which requests more on the current sharing accuracy and integrity.

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