A Novel Capacitor Bank for Linearized and Wide-band VCO

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Abstract: A novel capacitor bank is proposed to implement a wide-band $CMOS$ voltage-controlled oscillator(VCO) with linearized tuning characteristics. Taking advantage of the Ohms law, the tuning voltage is replaced by the product of the current and resistance, which provides one more freedom degree for tuning than the conventional VCO. This novel voltage equivalent capacitance array($VECA$) is clearly different from that of the conventional VCO, which is made up of only a group of varactors, a resistance array and a current source array. The resistance array and the current source array are controlled by four-bits digital signals which provide a group of bias voltages on varactors that can be equivalent to a capacitor array. Using this method, the capacitances can be set accurately and conveniently to adjust the frequency for the linearized coarse tuning. For the fine tuning, an analog control voltage is added to the bias voltage on varactors by using current superposition technology. Simulation results show that the tuning gain(K_{VCO}) curves of the VCO is in little difference as the different digital signals vary, K_{VCO} is in the range from -214 to $-137MHz/V$ across the tuning range of $5 - 5.85GHz$, and the frequency step is $166MHz$. The proposed VCO has a better coarse tuning characteristic compared against the conventional VCO while dissipating $4.43mA$ from a $1.8V$ supply.

Key–Words: voltage-controlled oscillator(VCO), wideband, linearized, capacitor bank

1 Introduction

Full integrated phase-lock loop(PLL) is a key component of the radio frequency (RF) system, which provides an accurate, pure and steady local oscillator signal for frequency conversion during the communication. RF signals are down converted to a low intermediate frequency(IF) signals in the receiver mixed by the local oscillator signal, same as the IF signals are up converted to RF signals in the transmitter. The core of the conventional voltage-controlled oscillator(VCO) , which is the most important component of PLL, is made up of a capacitor and an inductor. To expand the tuning range, the VCO employs digital signals to control the switching capacitor array for the coarse tuning, and an analog signal on varactors for the fine tuning. The conventional VCO is binary-weighted and its tuning characteristic increases nonlinearly, as shown in Fig. 1, when the number of the switches that turn on increases, the stepped frequency and the tuning gain K_{VCO} will decrease, as shown in Fig. 2. The tuning characteristic deteriorates, which influences the performances of PLL, such as lock-time, spectrum purity and stability.

Many studies have been devoted to optimize the tuning characteristic of the VCO, the technology mostly employed for the coarse tuning is the structure including a switching capacitor array and a varactor array[1]. The switching capacitor array sets the value of the stepped frequency for the coarse tuning and the varactor array compensates the fine tuning characteristic. But both arrays occupy a large area, and the capacitances of the switching capacitor array are not able to be set precisely. There are some methods for the fine tuning characteristic, such as partial tuning voltage technique, the varactor array with different biasing, diode varactors, the variable current source and so on. The partial tuning voltage technique[2] is that the input voltage is reduced proportionally to be the real tuning voltage, so that the range of the tuning voltage shrinks and the linearity is better by sacrificing the tuning gain. Using the Fourier transformation, the varactor array with different biasing[3, 4, 5, 6] is employed to get a linear $f - V$ characteristic. A varactor array which occupies more areas and an extra biasing circuit are needed. Although diode varactor[7] has a

more linear tuning characteristic, but the range of the capacitance is small, which limits the tuning range. To get the same capacitance, the diode varactor occupies a larger area than the $MOSFET$ varactor.The VCO with variable current source array[8, 9] can adjust the K_{VCO} by changing the DC current, which costs more DC power than the conventional VCO. A linear $f-V$ characteristic can be achieved with the frequency feedback[10].

In this paper, a novel capacitor bank structure is proposed to implement a wide-band $CMOS$ voltage-controlled oscillator(VCO) with linearized coarse tuning characteristics. As shown in Fig. 3, this novel voltage equivalent capacitance array($VECA$) consists of a group of varactors, a resistance array and a current source array. The tuning voltage can be presented by the product of the current and resistance, which provides two tuning parameters to adjust the K_{VCO} flexibly. Controlled by four-bits digital signals, the resistance array and the currentsource array provide a group of the bias voltages on varactors that can be equivalent to a capacitor array ,which can set the capacitances precisely and conveniently to adjust the stepped frequency for the linearized coarse tuning. The resistance array is employed to get the same tuning characteristic by different digital signals. For the fine tuning, an analog control voltage is added to the bias voltage on varactors by the technology of current superposition and the area can be saved by using one group of varactors in common. This VCO has much better tuning linearity performance which is useful in PLL applications.

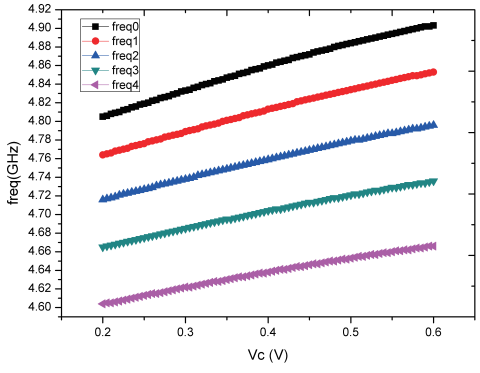

Figure 1: The tuning characteristic of the conventional VCO

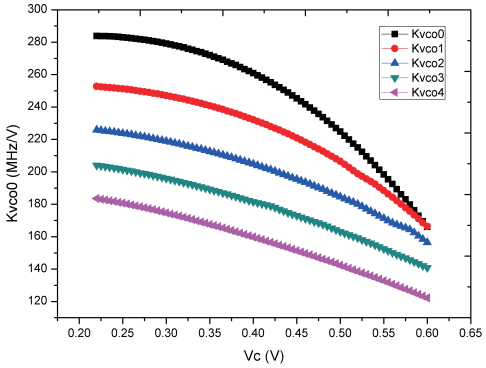

Figure 2: The tuning gain of the conventional VCO

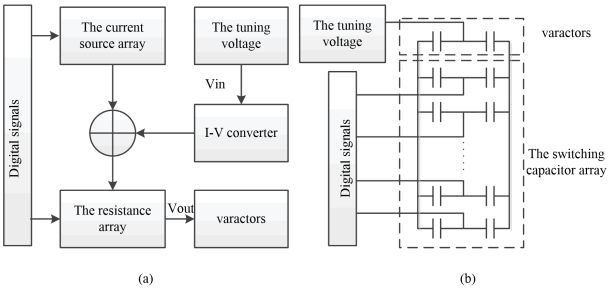

Figure 3: (a) The voltage equivalent capacitance array($VECA$) (b) The conventional switching capacitor array

2 Basic theory of the VCO

2.1 The operating principle of the VCO

As shown in Fig. 4, the negative resistance generator of the conventional VCO is composed of the $NMOS$ cross-coupled pair($M1-M2$), the $PMOS$ cross-coupled pair($M3-M4$) or both of them, and forms the core of the VCO with the capacitor and the inductor. $PMOS(M5)$ is used as the top current source which provides the bias current. As a matter of fact, the capacitor and the inductor contribute the real part of the impedance. The equivalent circuit of the $VCOs$ core is shown in Fig. 5, where L is the inductor and C is the capacitor which form the core, G_P is the equivalent parallel resistance of the core, $-G$ is the negative resistance which is generated by the complementary cross-coupled pairs($M1-M4$). To meet the start-up conditions, G should be larger than three times of G_P.

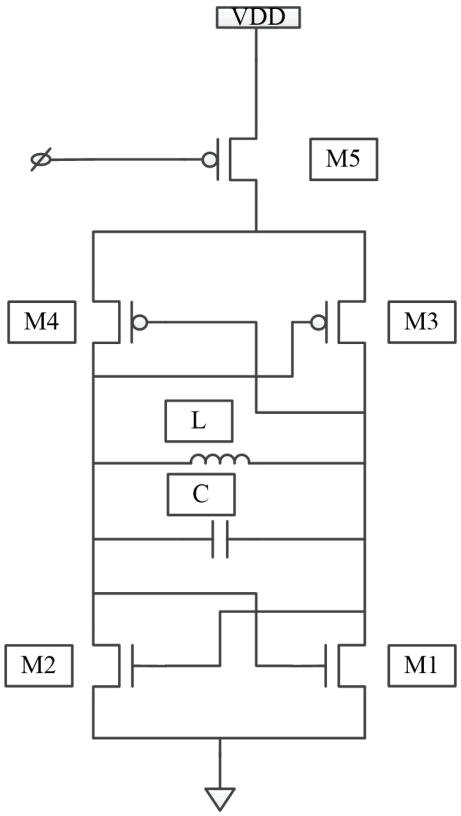

Figure 4: The circuit schematic of the conventional VCO

2.2 The coarse tuning characteristic

The formula of the total equivalent capacitance is expressed by

$$C_{total} = C + n \cdot C_{unit} + C_{var} \tag{1}$$

The oscillation frequency is derived as follows:

$$f = \frac{1}{2\pi\sqrt{LC_{total}}} = \frac{1}{2\pi\sqrt{L(C + n \cdot C_{unit} + C_{var})}} \tag{2}$$

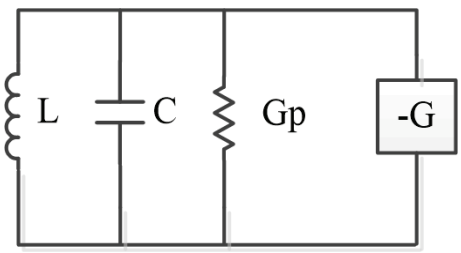

Figure 5: The schematic diagram of the VCO core

where C is the equivalent parallel capacitance, C_{unit} is the unit capacitance of the capacitor array, C_{var} is the capacitance of the varactors and n is the number of the switches with turning on. Because there is only one group of varactors in this circuit, so that n is the number of the digital signals with high level. On condition that $C_{total} \propto (n + A)^{-2}$ where A is positive, the oscillation frequency is proportional to n, then the coarse tuning characteristic is linear.

Because of the limit of the unit capacitance of the capacitor array, it is difficult to meet the condition of $C_{total} \propto (n + A)^{-2}$ accurately. In case that the capacitance range of the capacitor array is small, a small unit capacitance is necessary. $VECA$ uses a group of the bias voltages on varactors to replace the capacitor array, so the values of the bias voltages are set for the coarse tuning instead of the capacitance of the capacitor array. Due to the continuity of the voltage, there is no lower limit of the unit capacitance, so by setting the values of the voltages with different digital signals, the real capacitances are able to be set more conveniently than the switching capacitor array of the conventional VCO.

The capacitance range of the $VECA$ is less than

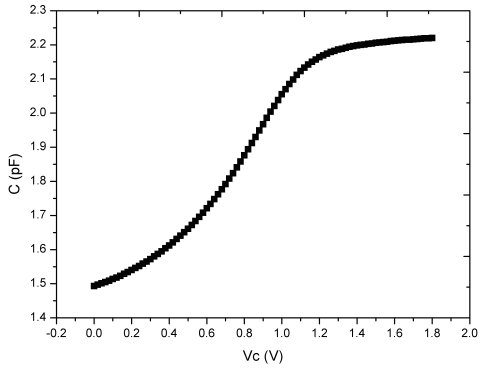

Figure 6: The $C - V$ characteristic of the $NMOS$ varactor

the switching capacitor array with the same area. Considering the practical application, the range will be even smaller.

The tuning gain is derived as below:

$$K_{VCO} = \frac{-1}{4\pi\sqrt{L}} \cdot \frac{\frac{dC_{var}}{dV}}{(C + n \cdot C_{unit} + C_{var})^{1.5}} \tag{3}$$

$$C_{total} = C + n \cdot C_{unit} + C_{var} \propto (n + A)^{-2} \tag{4}$$

$$C_{total} = \frac{B}{(n + A)^2} \tag{5}$$

$$K_{VCO} = \frac{-1}{4\pi \cdot B^{1.5}\sqrt{L}} \cdot (n+A)^3 \cdot \frac{dC_{var}}{dV} \quad (6)$$

Putting (5) into (3), so K_{VCO} is shown in (6).(6) shows that K_{VCO} changes nonlinearly with n, and a reverse change of the $\frac{dC_{var}}{dV}$ is needed to cancel the effect of the n, so that K_{VCO} is independent of n. In other words, the coarse tuning is linear across the whole tuning range. The relation between $\frac{dC_{var}}{dV}$ and n is shown as follows:

$$\frac{dC_{var}}{dV} \propto (n+A)^{-3} \quad (7)$$

Because of the nonlinear $C-V$ characteristic of $NMOS$ varactors, additional handling is needed. The conventional VCO has only two freedom degrees for the tuning characteristic, the number of the capacitors and the tuning voltage. By the Ohms law, the tuning voltage is replaced by the product of the current and resistance, which increases a freedom degree.

$$V_{ctl} = I_{total} \cdot R = R \cdot (I_d + I_v) \quad (8)$$

$$\frac{dC_{var}}{dV} = g_m \cdot R \cdot \frac{dC}{dV}|_n \propto (n+A)^{-3} \quad (9)$$

$$K_{VCO} = \frac{-(n+A)^3}{4\pi \cdot B^{1.5}\sqrt{L}} \cdot g_m \cdot R \cdot \frac{dC}{dV}|_n \quad (10)$$

Where $\frac{dC}{dV}|_n$ is a set of constants with different n, I_d is the bias current provided by the current source array, I_v is the tuning current, which can be ignored in case that I_v is far lower than I_d. g_m is the transconductance of the input MOS transistor.

As shown in Fig. 7, This phenomenon that $\frac{dC}{dV}$ increases monotonically with V_c at first, when $Vc = 0.9V$, $\frac{dC}{dV}$ reaches the maximum and then decreases monotonically with Vc after which will influence the selection of the resistance array. Enough redundancy is necessary for the $PMOS$ constant-current sources to work in the saturation region, otherwise the $PMOS$ constant-current sources will work in the linearization region, which changes the ratio of the current mirror, so that the front part where the voltage is low in Fig. 7 is chosen for linear current copy. This selection needs larger $NMOS$ varactors because the capacitance is limited.

2.3 The fine tuning characteristic

A nonlinear relation can be approximated as a linear one with a small variation range, so to get a same range of the capacitance, a large $NMOS$ varactor has a more linear fine tuning characteristic than a small one. The tuning voltage which is scaled down is added to the voltage on varactors by the technology of current superposition. The proposed VCO has a linear tuning characteristic and saves areas at the same time.

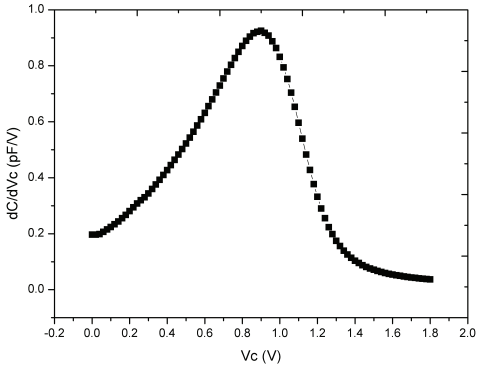

Figure 7: The curve of $\frac{dC}{dV}$

3 The proposed VCO

Fig. 8(a) is the block diagram of the proposed VCO. As shown in Fig. 8(a), the right part is the core of the VCO and the left is the $VECA$. The resistance array adjusts K_{VCO} by different digital signals. For the fine tuning, an analog control voltage is added to the bias voltage on varactors by the technology of current superposition. Different from the conventional switching capacitor array, $VECA$ expands the tuning range by changing the bias voltages controlled by different digital signals, instead of the extra capacitors.

The first step of the design is to determine the capacitances by different digital signals and the bias voltage on the varactors by Fig. 6. Fig. 6 shows that the relation of voltage and capacitance is nonlinear, so that the values of the voltage need to be gained from Fig. 6. As usual, the capacitances with different n need to be counted at first:

$$C_{max} = \frac{B}{(n+A)^2} \quad (11)$$

$$C_{min} = \frac{B}{(n+A)^2} \quad (12)$$

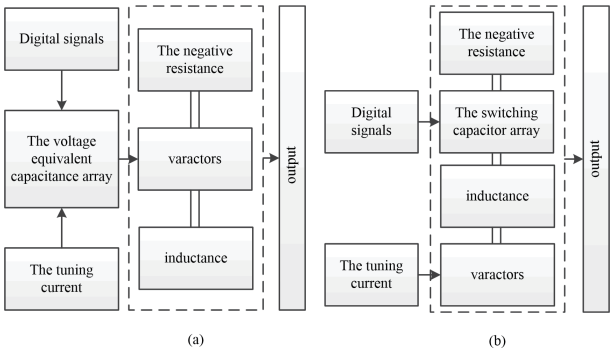

Figure 8: (a)The block diagram of the proposed VCO (b)The block diagram of the conventional VCO

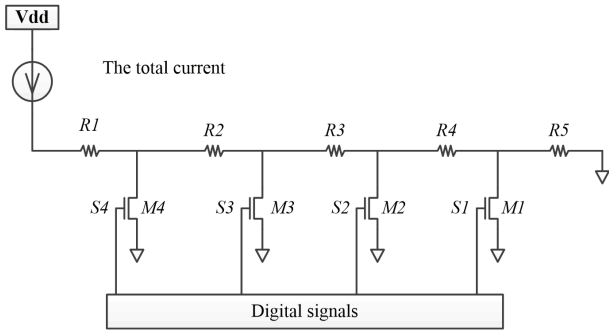

Figure 9: The circuit schematic of the resistance array

Where A and B are constant, C_{max} and C_{min} are the maximal and the minimal capacitance, respectively. Putting A and B into (5), the capacitances by different n are known, and after that, the bias voltages which need to be provided by the resistance array and the current source array can be observed in Fig. 6. The second step is to build the core circuit of the VCO. The circuit schematic of the proposed VCO is the same as that in Fig. 4.

3.1 The resistance array

The third step is to build the resistance array of the $VECA$. (9) shows that K_{VCO} is proportional to the resistance, so the resistance array can be used to make up the differences of K_{VCO} by different n. As shown in (6), C_{total} decreases and K_{VCO} increases when n increases. The small n needs a large resistance to enhance K_{VCO}. Considering the monotonic increasing $\frac{dC}{dV}|_n$, the resistance reduces more obviously as n increases.

As show in Fig. 9 when $S1-S4$ become high level in a row, $NM1-NM4$ turn on and $R5-R2$ are shorted successively, so the equivalent resistance reduces. Because the voltages have been determined, so that the resistance array decides the current and the power dissipation. Considering the influence of the $NM1-NM4$, $R1-R5$ need fine adjustments to meet the requirements for the equivalent resistance of the resistance array. In this design $R1-R5$ is 1300Ω. 130Ω. 120Ω. 220Ω and 480Ω respectively.

3.2 The current source array

The fourth step is to build the current source array of the $VECA$. The resistance array adjusts the K_{VCO} by different digital signals and the stepped frequency is controlled by the bias voltages on varactors. So a current source array is necessary to provide the bias voltages together with the resistance array and should be set carefully to get a constant stepped frequency.

The sum of the bias current and the tuning current are deduced in (8). Because the assumption that I_v is far below I_d fails sometime, so that the bias currents are determined together with the tuning current and the center currents have to meet the requirement of the formula (8) and (9). As shown in Fig. 10, each branch current is copied from the reference current(I_{ref}) by the current mirrors. Tuning off $PMOS$ $PM1-PM4$ in sequence and the current provided by the current source array reduces by n increasing. When all switching $PMOS$ turn on, n is zero and the bias current of the current source array is maximum. At this point, the bias voltage is $0.97V$ and the resistance of the resistance array is 2250Ω, so the bias current is $0.43mA$. The tuning current which decides the tuning range for each n is set by the width-length ratio of $PM5$, the assumption that $\frac{dC}{dV}|_n$ is a group of constants will fail in formula (9) when the tuning current becomes so big, which deteriorates the linearity of the tuning characteristic.

3.3 The circuit schematic of the proposed VCO

The last step of this design is to integrate all the parts together. Fig. 11 is the circuit schematic of the proposed VCO.As shown in Fig. 11, the left part is the $VECA$. The resistance array controlled by four-bits digital signals adjusts K_{VCO} and provides the bias voltages on varactors which is equivalent to the switching capacitor array. The right part is the core of the VCO charged by a negative resistance generator and a top $PMOS$ current source. Compares with the conventional VCO, the proposed VCO has only one group of varactors and replaces the capacitor

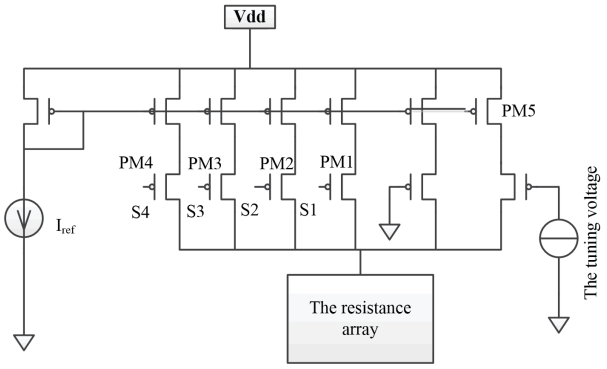

Figure 10: The circuit schematic of the current source array

array with the $VECA$ shown in Fig. 11. Due to the continuity of the voltage, the difference between the capacitances by adjacent n has no lower limit in theory. The tuning voltage is converted into the tuning current by the input $PMOS$ transistor. As the first stage of the proposed VCO, the input $PMOS$ transistor has a big influence on the linearity of the whole VCO.

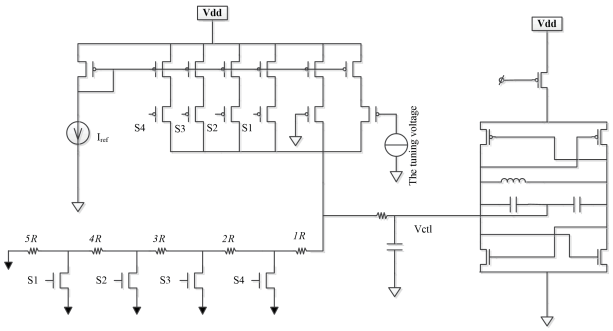

Figure 11: The circuit schematic of the proposed VCO

4 Simulation results

R is a group of constants in (8) with different digital signals. The relationship between V_{in} and I_v has to be linear for linearized fine tuning characteristic. As shown in Fig. 12 the stepped voltage of V_{ctl} on varactors varies, while the stepped frequency in Fig. 14 do not change because of $\frac{dC}{dV}|_n$.Due to the channel-length modulation, the curves of V_{ctl} on varactors are not parallel each other. When n increases, the bias voltage on varactors decreases and drain-source voltage of $PMOS$ increases, so

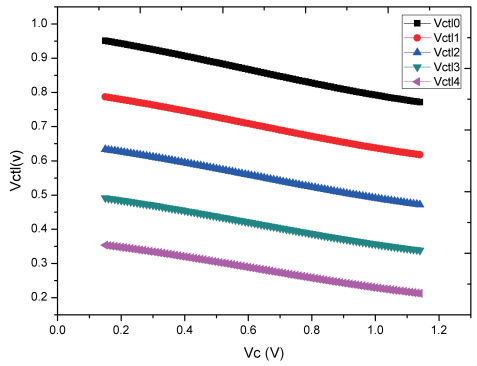

Figure 12: The voltage on varactors

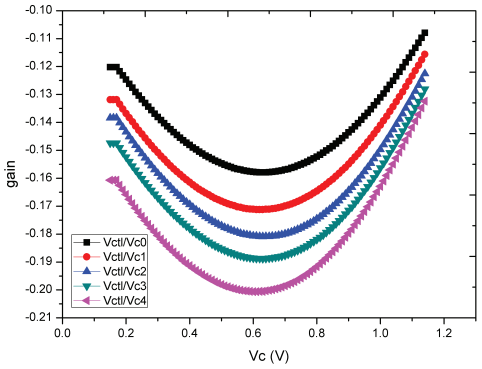

Figure 13: The gain of the $VECA$

the current becomes larger, which will deteriorates the tuning characteristic, which needs to adjust the resistance array to cancel this effect. Fig. 13 shows that the gain of the left part of the proposed VCO decreases monotonically in the first and increases monotonically later. Because n, R and $\frac{dC}{dV}|_n$ are all constants in (10) with the same digital signals, so the transconductance of the input transistor leads to the variation of the gain, which deteriorates the fine tuning characteristic seriously. More unfortunately, the effect can only be weaken by using $PMOS$ input transistor with larger width to length ratio and a smaller input voltage.

The curves of the tuning characteristic of the proposed VCO are shown in Fig. 14. The tuning range is $5-5.85GHz$ and the stepped frequency is $166MHz$. The curves of the fine tuning characteristic are in parallel with each other and the K_{VCO} in Fig. 15 is the same with different digital signals, which show that the resistance array compensates the differences

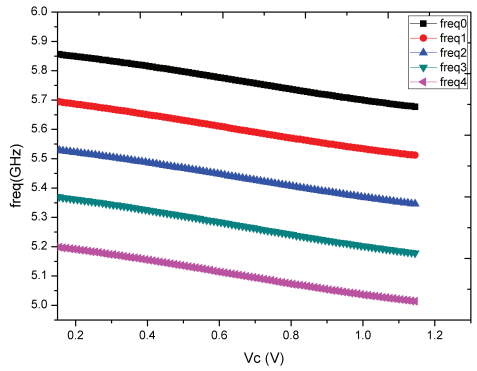

Figure 14: The tuning characteristic of the proposed VCO

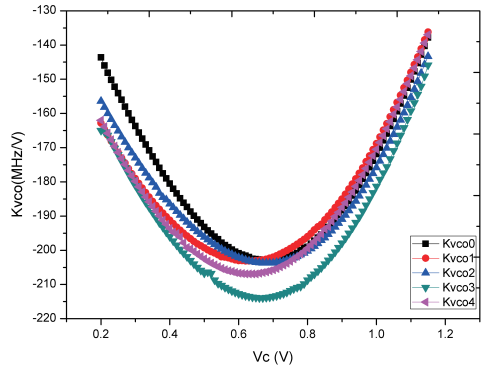

Figure 15: The tuning gain of the proposed VCO

of the K_{VCO} with different digital signals to get a linearized tuning characteristic. K_{VCO} with different digital signals is shown in Fig. 15. K_{VCO} ranges from -214 to $-137MHz/V$.Some previous works are summarized in Table 1, in which FoM represents the widely used VCO figure-of-merit given by

$$FoM = L(\triangle f) + 20\log(\frac{f_{osc}}{\triangle f}) + 10\log(\frac{P_{diss}}{1mW}) \quad (13)$$

where L is the phase noise,$\triangle f$ is the offset frequency, f_{osc} is the oscillation frequency, and P_{diss} is the power dissipation of the VCO.

5 Conclusion

A novel capacitor bank structure is proposed to implement a wide-band $CMOSVCO$ with linearized tuning characteristics. This novel capacitor bank structure($VECA$) is made up of only a group of varactors, a resistance array and a current source array. Taking advantage of the Ohms law, the tuning voltage is replaced by the product of the current and resistance, which provides one more freedom degree to adjust the K_{VCO} by digital signals. The resistance array and the current source array provide a group of the bias voltages on varactors to be equivalent to a capacitor array, which can set the capacitances accurately and conveniently. The resistance array is employed to adjust the tuning characteristic. For the fine tuning, an analog control voltage is added to the bias voltage on varactors by the technology of current superposition. The tuning range is $5 - 5.85GHz$ and K_{VCO} ranges from -214 to $-137MHz/V$. This VCO is simulated and designed in $0.18um$ $CMOS$, and dissipates $4.43mA$ from a $1.8V$ supply. The validity and feasibility of the theory have been verified by the simulation results.

Acknowledgments

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Table 1: PERFORMANCE COMPARISON WITH OTHER WIDE-BAND $VCOs$

Ref	[11]	$Thiswork$
$F_{osc}[GHz]$	6.0	5.5
$\triangle K_{VCO}[\%]$	57.5	22
Tuning range[%]	5.1	15.7
Phase noise[dBc/Hz]	-115.2@1M	-112.2@1M
Power Diss[mW]	12.5	8.0
FoM[dBc/Hz]	-179.8	-177.5
Tec[nm]	130	180