Small Area DAC using SC Integrator for SAR ADC

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Abstract: - A successive approximation register(SAR) analog-to-digital converter(ADC) is widely used because of its relatively short conversion time and small size. However, a SAR ADC requires a DAC of the same resolution, resulting in a larger area. To solve this problem, a DAC that does not increase in area as resolution increases is needed. This paper presents SAR ADC and DAC using Switched Capacitor(SC) integrator. This DAC 's area is independent of resolution and ADC is no need to a sample and hold circuit because it uses an SC integrator. The operation of this ADC is similar to a charge-redistribution based SAR ADC. The reference voltage is generated by charge redistribution of the SC integrator input capacitor and the reference capacitor, and the DAC voltage is generated by accumulating the generated voltage on the output capacitor of the SC integrator. The proposed SAR ADC was designed using TSMC 0.18μm CMOS high voltage technology, occupies on chip area of 0.316mm^2. At 5V supply and 100kS/s, the simulated SNDR and ENOB are 53.7dB and 8.63bit. Considering the good DNL, a higher resolution ADC can be designed with the same area.

Key-Words: - Analog-to-digital converter, Successive approximation register, Switched Capacitor integrator, SAR ADC, Digital-to-Analog converter, Charge-redistribution based SAR ADC, Sample and Hold circuit

1 Introduction

With the recent increase in the Internet of things(IOT) market, the demand for sensors and ADCs is increasing. Among the many ADCs, a successive approximation register(SAR) analog-to-digital converter(ADC) is widely used because of its relatively short conversion time and small size. Because of the a few analog blocks, charge-redistribution based SAR ADCs are preferred. This ADC uses a capacitor array to generate the DAC voltage. The total capacitance of the capacitor array is proportional to the square of the resolution. Therefore, large area and large charge current are required. The charge current is provided by the input source, not by the supply. For this reason, the issue of reducing the size of capacitor array is actively researched. A common solution is to design a high-resolution DAC using two low-resolution DACs [1][2]. To solve this problem, this paper proposed a SAR ADC using a Switched Capacitor(SC) integrator DAC. The operation of this ADC is similar to a charge-redistribution based SAR ADC. But DAC's area is independent of resolution. Section 2 introduce the conventional charge-redistribution based SAR ADC. Section 3 describes the structure of proposed ADC and its operation. Section 4 shows the simulation result.

2 Conventional SAR ADC

Fig. 1 is conventional charge-redistribution based SAR ADC. N is the resolution of the ADC. Fig. 2 is the equivalent circuit of the capacitor When the capacitor array operates as a DAC in Fig. 1. The voltage change of the capacitor can be derived as

$$\Delta V_2 = -\frac{(2^n - 2^k)C}{(2^n - 2^k)C + 2^k C}(V_{REF} - V_{CM}) \quad (1)$$

$$\Delta V_1 = \frac{2^k C}{2^n C}(V_{REF} - V_{CM}) \quad (2)$$

This ADC requires a DAC with the equal resolution. To generate the DAC voltage, k of eq. (2) must be a natural number from 1 to n-1. The capacitor weight is a resolution power of two. If the resolution is high, a lot of capacitors are needed. Therefore, the circuit requires a large area and large current for capacitor charging and discharging [2][3].

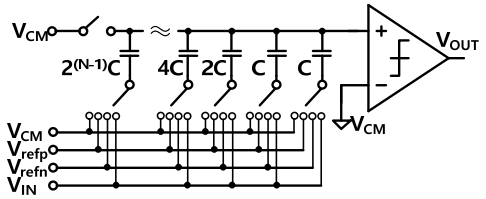

Fig. 1 Charge-redistribution based SAR ADC

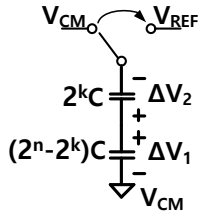

Fig. 2 The equivalent circuit of the capacitor

3 Proposed SAR ADC

Fig. 2 shows a schematic of basic non-inverting SC integrator [4][5].

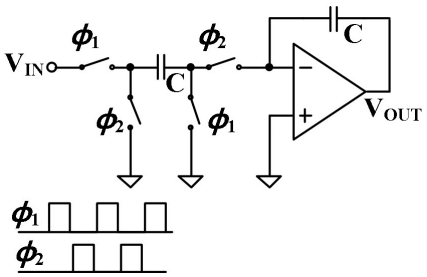

Fig. 3 Non-inverting SC integrator

Output voltage of Fig. 3 can be calculated as

$$V_{OUT} = V_{IN} + z^{-1}V_{OUT} \quad (3)$$

Eq. (3) means that the SC integrator can store the analog voltage, and this function can be used to make the DAC.

3.1 Single-ended SC integrator DAC

The DAC can be designed by modifying Fig. 3. Fig. 4 is a schematic of a DAC. C_1 and C_2 are used to generate the reference voltage, and the DAC voltage is generated by accumulating the reference voltage at C_{OUT}. All capacitors have the same capacitance. Fig. 5 shows the operation of DAC at each switch cycle.

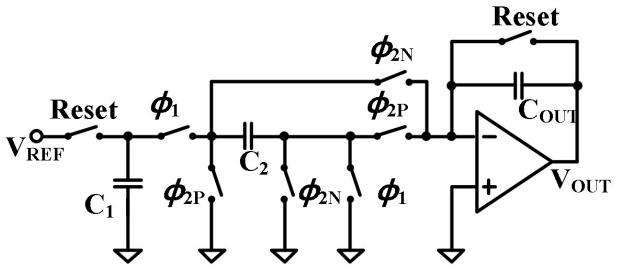

Fig. 4 Single-ended SC integrator DAC

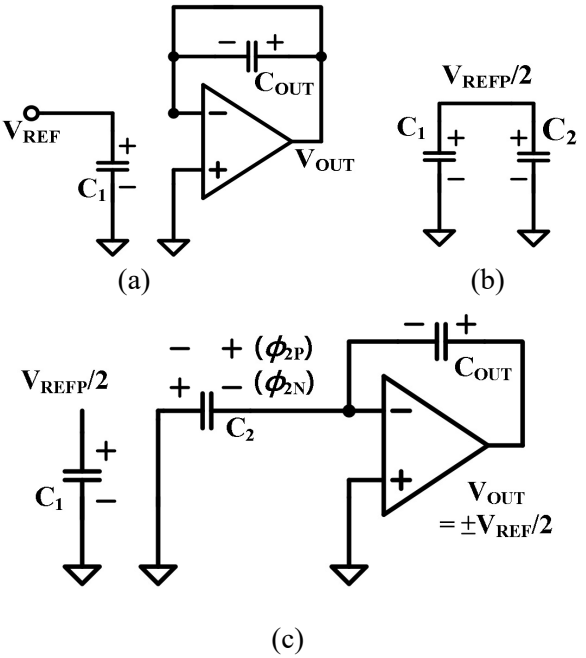

Fig. 5 (a) Reset. (b) $\emptyset_1$ is on. (c) $\emptyset_2$ is on.

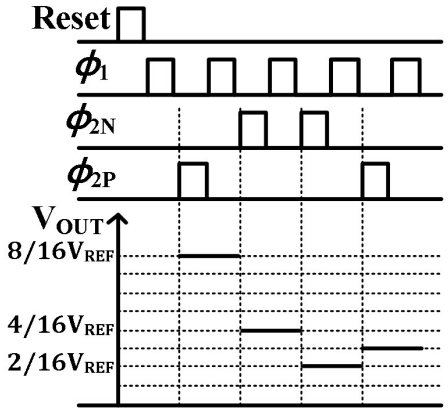

Fig. 6 Waveform of SC integrator DAC

When the reset switch is turned on at Fig. 4, C_1 is charged to reference voltage and C_{OUT} is discharged.

$$V_{C1,RESET} = V_{REF} \quad (4)$$

$$V_{COUT,RESET} = 0 \quad (5)$$

When $\emptyset_1$ is turned on, the charge of C_1 moves to C_2 and the potentials of the C_1 and C_2 become equal.

$$V_{C1,\emptyset1} = V_{C2,\emptyset1} = \frac{V_{REF}}{2} \quad (6)$$

When $\emptyset_2$ is turned on, C_1 is floated, and the charge of C_2 moves to C_{OUT}. The potential of C_2 becomes 0V and V_{OUT} becomes half of the reference voltage. Single-ended DAC requires switches to rotate

ㄴ direction of C2. The direction of C2 determines whether to add or subtract the voltage.

$$V_{C1,Ø2} = \frac{V_{REF}}{2} \quad (7)$$

$$V_{C2,Ø2} = 0 \quad (8)$$

$$V_{COUT,Ø2P} = \frac{V_{REF}}{2} \quad (9)$$

$$V_{COUT,Ø2N} = -\frac{V_{REF}}{2} \quad (10)$$

The DAC voltage can be generated by repeatedly switching the $Ø_1$ and $Ø_2$. Fig. 6 shows the operating waveform of the DAC in Fig. 4.

3.2 Fully differential SC integrator ADC

Fig. 7 shows the Fully differential ADC. The C_{INN}, C_{INP}, C_{DACP} and C_{DACN} have the same capacitance.

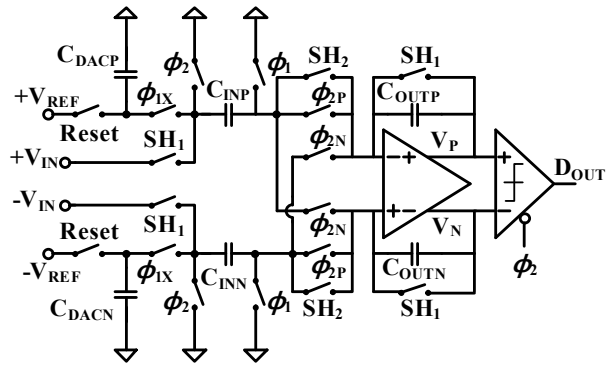

Fig. 7 Fully differential SC integrator ADC

The SAR ADC can be designed by adding a comparator to the DAC. The comparator converts an analog input voltage to a 1-bit. If V_P is higher than V_N, the quantization bit is high and $Ø_{2N}$ is turned on at the next $Ø_2$ cycle. If V_P is less than V_N, the quantization bit is low and $Ø_{2P}$ is turned on at the next $Ø_2$ cycle. $Ø_1$ and $Ø_2$ are non-overlapping clocks and 1-bit quantization can be processed for one clock.

The input voltage range of the ADC is limited by the output range of the OPAMP. Because the SC integrator is used as the sample and hold circuit. By reducing the gain, the sample and holder circuit can be used within the linear output range of the OPAMP. The SC integrator gain can be derived as

$$Gain = \frac{C_{IN}}{C_{OUT}} \quad (11)$$

Fig. 8 shows control clock for ADC in Fig. 7.

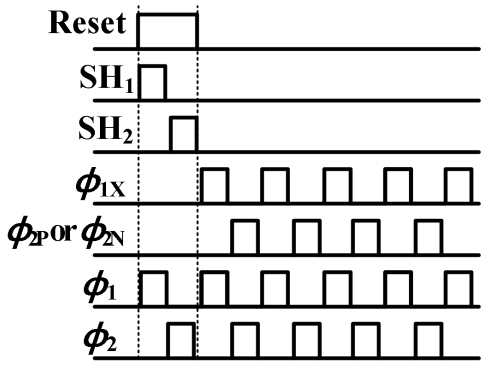

Fig. 8 Control clock for Fully differential ADC

In the SH_1, SH_2, and Reset cycle, the analog input is sampled, and the reference voltage is stored.

$$V_{CDACP,\mathrm{RESET}} = +V_{REF} \quad (12)$$

$$V_{CDACN,\mathrm{RESET}} = -V_{REF} \quad (13)$$

$$V_{COUTP,\mathrm{SH2}} = +AV_{IN} \quad (14)$$

$$V_{COUTN,\mathrm{SH2}} = -AV_{IN} \quad (15)$$

In the $Ø_{1x}$ cycle, the reference voltage is generated by C_{DAC} and C_{IN}. When the i-th bit is converted, the voltage of the C_{IN} and C_{DAC} can be derived as

$$V_{CDACP,Ø1x} = V_{CINP,Ø1x} = +\frac{V_{REF}}{2^i} \quad (16)$$

$$V_{CDACP,Ø1x} = V_{CINP,Ø1x} = -\frac{V_{REF}}{2^i} \quad (17)$$

In the $Ø_{2P}$ or $Ø_{2N}$ cycle, the DAC voltage is generated by transferring the charge of C_{IN} to C_{OUT}.

$$V_{CINP,Ø2} = V_{CINN,Ø2} = 0 \quad (18)$$

$$V_{COUTP,Ø2P} = z^{-1}V_{COUTP,Ø2} - A\frac{V_{REF}}{2^i} \quad (19)$$

$$V_{COUTN,Ø2P} = z^{-1}V_{COUTN,Ø2} + A\frac{V_{REF}}{2^i} \quad (20)$$

$$V_{COUTP,Ø2N} = z^{-1}V_{COUTP,Ø2} + A\frac{V_{REF}}{2^i} \quad (21)$$

$$V_{COUTN,Ø2N} = z^{-1}V_{COUTN,Ø2} - A\frac{V_{REF}}{2^i} \quad (22)$$

Fig. 9 shows the flowchart of Fully differential ADC.

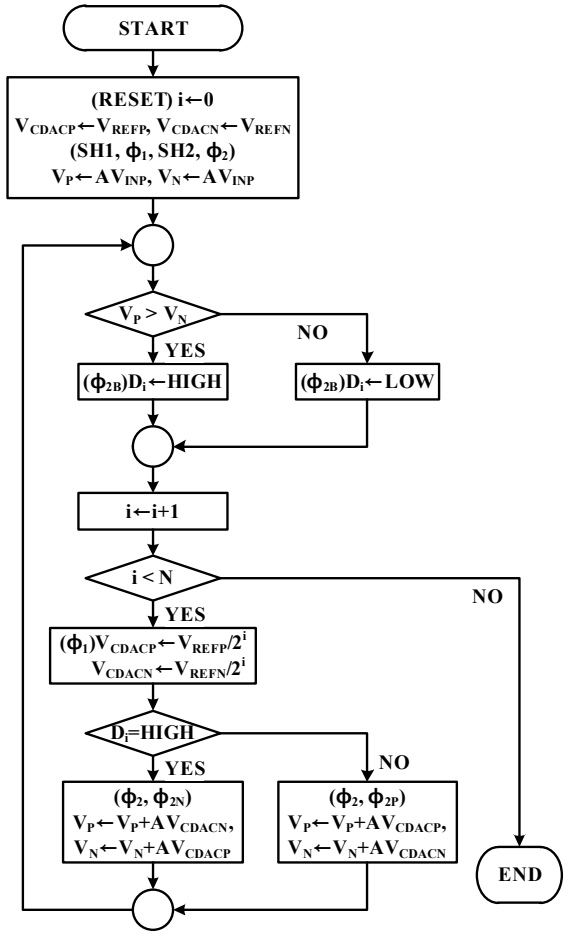

Fig. 9 Flowchart of fully differential ADC

4 Simulation Result

The proposed SAR ADC was designed using TSMC 0.18μm CMOS high voltage technology with 5V Supply voltage. At 5V supply voltage, input voltage range is 0V to 5V. The capacitance of C_{IN} is 2pF and C_{OUT} is 2.5pF. The sampling rate is 100kS/s and the simulation input signal is 10kHz, $5V_{PP}$ sinewave. Fig. 10 and Fig. 11 show the fully-differential OPAMP and Dynamic comparator[6] used in this ADC.

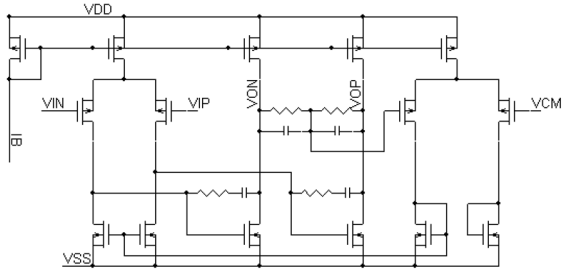

Fig. 10 Scheme of fully-differential OPAMP

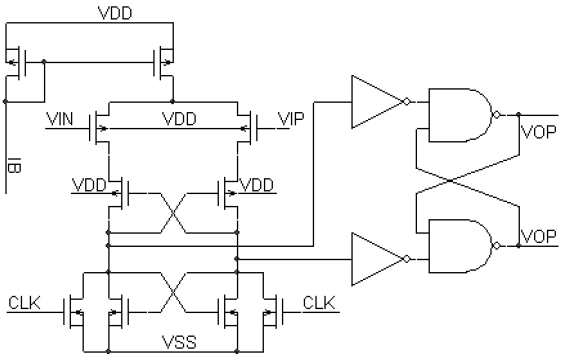

Fig. 11 Dynamic comparator

Fig. 13asdasdshows the FFT spectrum of the ADC output. The second harmonic is small becuase of the fully differential opamp. The difference between the third harmonic and the input signal is -67.5dB. The simulated SNDR and ENOB are 53.7dB and 8.63bit. Fig. 12 shows the simulated DNL of the proposed ADC. Peak DNL is -0.01LSB to +0.052LSB. Table 1 summarizes the performance of the proposed SAR ADC and compares the proposed ADC with other SAR ADC[7][8].

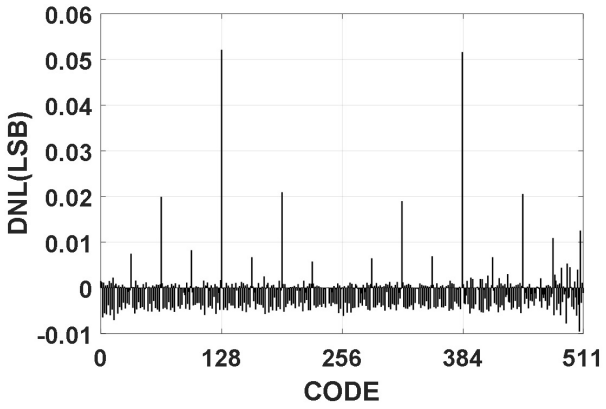

Fig. 12 Simulated DNL

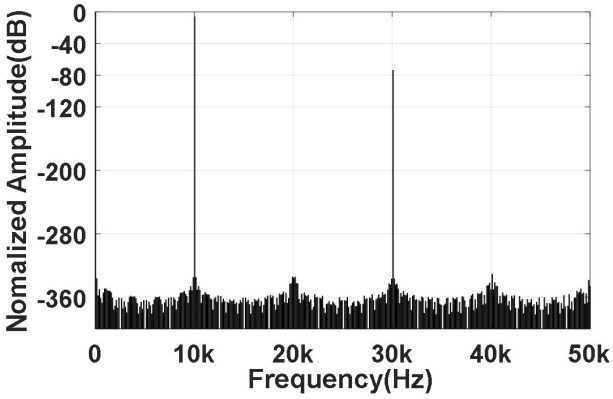

Fig. 13 Simulated FFT spectrum

Table 1 Performance of proposed SAR ADC

	This Works	[7]	[8]
Technology[μm]	0.18	0.18	0.18
Resolution[Bit]	9	8	8
Sampling frequency[MHz]	0.1	20	20
Supply voltage[V]	5	1.8	1.8
Input Voltage range[V]	0 ~ 5	0 ~ 1.8	
DNL[LSB]	-0.010/ + 0.052	-0.55/ +0.68	0.81
SNDR[dB]	53.7	43.2	44.5
ENOB[Bit]	8.63	6.88	7.21
POWER comsumption[mW]	2.035	2.36	0.588
Chip area(mm^2)	0.316	0.105	0.176

5 Conclusion

This paper has presented SAR ADC using switched capacitor integrator DAC. The ADC consumes 2.035mW at the sampling rate of 100kS/s. The simulated SNDR and ENOB are 53.7dB and 8.63bit. The total capacitance is 13pF. Because The proposed SAR ADC does not increase in area with increasing resolution, this ADC is advantageous for high resolution ADC design. Considering the simulated DNL, a higher resolution ADC can be designed with the same area.

Acknowledgment

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