Exponential Step-up/Step-down Type Switched-Capacitor Power Supply with Variable Conversion Ratio

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Abstract: - In this paper, a switched-capacitor(SC) power supply which can obtain exponential conversion ratios $J^{\pm K}$ is proposed (J and K are integer). The conversion ratio can be varied between J^{-K} and J^{+K} by shifting the clock phase of each switch. Concerning the general proposed circuit, the ideal step-up ratio is analyzed changing J and K at no-load, and HSPICE simulations are performed under the J=2 and J=3 types. As a result, (1) at no-load, J=3 type can obtain the highest step-up voltage ratio with the same number of elements, (2) under the load, J=2 type can obtain the highest power conversion efficiency with the same chip-size and the same turn-on/turn-off time of each switch. Furthermore, the inrush current can be decreased by changing conversion ratio at start-up.

Key-Words: - switched-capacitor power supply, exponential step-up/step-down, DC-DC converter, small-sized and lightweight, inrush current

1 Introduction

An existing power conversion circuit converts an input voltage into a high frequency rectangular wave (or a sinusoidal wave, only resonance converter) by a switching circuit, and outputs using a smoothing LC circuit. The output voltage is regulated by controlling a duty ratio or a switching frequency of the switching circuit. Although this method is obtained a high power conversion efficiency, deleterious magnetic flux is generated since a high frequency current flows in a magnetic component such as an inductor or a transformer. It is difficult to block the magnetic flux by a shield. Therefore, the power supply and a signal processing circuit needs to be spaced apart slightly for preventing the noise. On the other hand, switched-capacitor(SC) power supplies do not contain any magnetic component and convert an input voltage by changing the connections of capacitors at high speed. The first SC power supply is presented in 1932 as the Cockcroft-Walton circuit (CW) for a high-voltage generator of a nuclear reaction experiment device[1]. Until semiconductor switches are developed in the 1980s, SC circuits were not utilized as a small and lightweight power supply. After high speed and low on-resistance power MOSFET's are marketed in 1990s, various topologies for the SC power supply have been proposed[2]~[8]. Among others, a digital-selecting type proposed in recent years and its 2 times conversion ratio can obtain higher total conversion ratio with the small number of elements [5]~[7].

In this paper, an exponential step-up/step-down type SC expanding the digital-selecting type is proposed. The proposed circuits can obtain at most/least $J^{\pm K}$ times conversion ratio (J and K are integer). The conventional digital-selecting type has the structure that $2^{\pm 1}$ times conversion circuit block connected in cascade K stages. On the other hand, the proposed circuits have the $J^{\pm 1}$ times conversion circuit block per one stage. Therefore, the proposed circuits have the various conversion ratios by changing the combination of J and K. In section **2**, the value of J which can obtain the ideal maximum step-up ratio with the same number of elements is analyzed at no-load. In section **3**, HSPICE simulation results are shown and compared with characteristics of the ideal analysis.

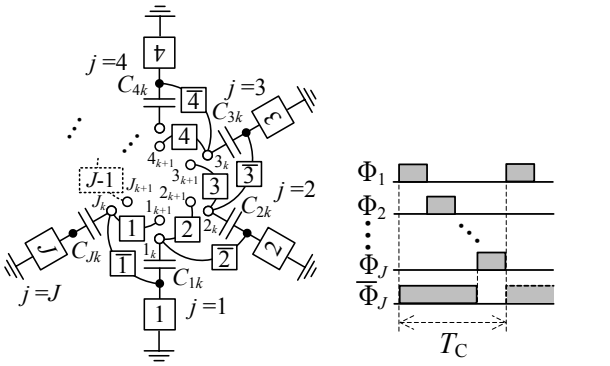
In general, SC converters flow a large inrush current at start-up since multiple capacitors are charged at the same time. This inrush current causes deterioration of circuit elements and affect external devices. The proposed circuit can reduce the inrush current because the number of charged/discharged capacitors can be varied without changing circuit configurations.

In section **3**, it is confirmed by simulations that the inrush current can be reduced at start-up by changing conversion ratio, as compared with that of the fixed step-up ratio.

2 Proposed Circuit

2.1 In general case (J^K times step-up)

Figure 1(a) shows the proposed circuit of k stages (k=1,2$\cdots K$). Table 1 shows the meanings of each symbol. The square symbols 1~J in this figure indicate switches. They are driven by the non-overlapping J phase clocks Φ_1~Φ_J as shown in Fig.1(b). Also, $\overline{j}$ (j=1~J) are driven by $\overline{\Phi_j}$ clocks. Figure 2 is the general structure of the proposed circuit consisted of circuit block of Fig.1 connected in cascade. Furthermore, Fig.3 shows the instantaneous equivalent circuit of Fig.1(a) while the clock Φ_j is in a high level. The capacitor $C_{j,k}$ is charged up to $V_{j,k}$ in a steady-state, since the upper node of $C_{j,k}$ is connected to the output voltage of the former stage and the lower node is connected to the ground. This state is repeated for Φ_1~Φ_J and each capacitor $C_{j,k}$ in the same circuit block (same k) is charged up to the same voltage $V_{j,k}$ in a steady-state. At the same time, all capacitors are connected in series and output to each output node j_{k+1}. Therefore, the output voltage is $JV_{j,k}$. Since the step-up ratio per one stage is J times and K stages circuit blocks are connected in cascade, the exponential J^K times step-up ratio can be obtained.



(a)Circuit block SC$_k$ (b)driving clock

Fig.1 Proposed circuit of stage k.

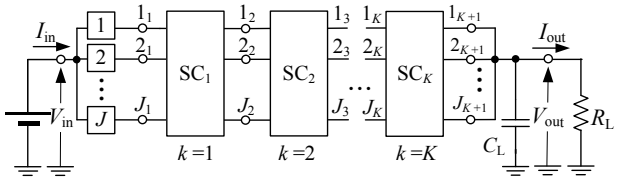


Fig.2 General structure of proposed circuit.

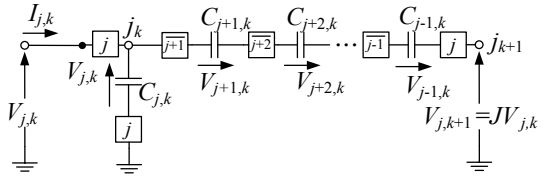


Fig.3 Instantaneous equivalent circuit in state j.

2.2 2^K step-up type (2^3 times step-up)

Figure 4 shows the proposed circuit with J=2, K=3. In this figure, the switches 1, 2 are driven by the two phase non-overlapping clocks Φ_1 and Φ_2, respectively. Figures 5(a) and (b) are the instantaneous equivalent circuits in each state. During the state 1, the capacitor C_{11} is connected to the DC input voltage V_{in} and charged up to V_{in}. Similarly, during the state 2, C_{21} is charged up to V_{in}. In each state, capacitors C_{12} and C_{22} of the stage 2 are charged by the series connection of C_{11} and C_{21} of the first stage. Consequently, the charged voltage of C_{12} and C_{22} is $2V_{\text{in}}$. Thus the step-up ratio per stage is 2. In Fig.4, since the number of the circuit block K is 3, the step-up ratio m is 2^3(=8). This circuit is also named the digital-selecting type since each capacitor is charged by the ratio of each binary digit weight [7].

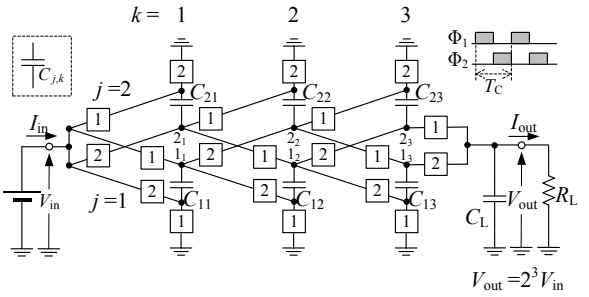
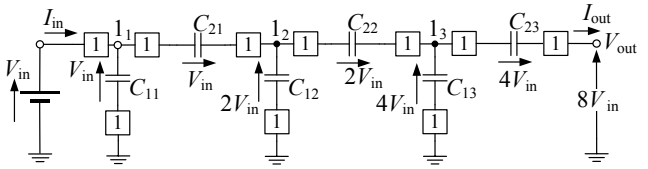
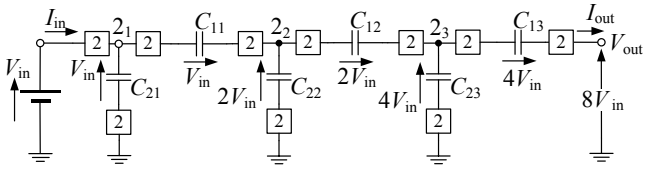


Fig.4 2^K step-up type (J=2, K=3).



(a)State 1 (Φ_1 : high level)



(b)State 2 (Φ_2 : high level)

Fig 5 Instantaneous equivalent circuit of Fig.4.

Table 1 Meanings of symbols.

Symbols	Meanings
j	Order of capacitors in the same circuit block (j=1,2…J)
J	Number of capacitor per one stage
k	Order of circuit blocks (k=1~K)
K	Number of stages in cascade connected blocks

2.3 3^K step-up type (3^2 times step-up)

Figure 6 shows the proposed circuit with J=3, K=2. In this figure, the switches 1~3 are driven by the three phase non-overlapping clocks Φ_1~Φ_3, respectively. Figures 7(a) and (b) are the instantaneous equivalent circuits of k=1 during each state. During the states 1, 2, and 3, the capacitors C_{11}, C_{21}, and C_{31} are charged up to V_{in}, respectively. In the same time, all capacitors are connected in series and discharged to the output node j_2 in each state. The output voltage $V_{j,2}$ is equal to $3V_{\text{in}}$ and the number of blocks K is 2. Therefore, the step-up ratio m is 3^2(=9).

2.4 Method of varying conversion ratio

In this section, the operation of obtaining the general J^{-K}~J^{+K} times conversion ratio without changing the circuit configurations is explained. The values of r_k and s_k are the number of charged and discharged capacitors at the stage k, respectively. In the stage 1, since the r_k capacitors are charged in series by the input voltage V_{in}, each capacitor voltage is equal to V_{in}/r_k. In the same time, since the s_k capacitors are discharged in series to the next stage, the conversion ratio per one stage m_k is s_k / r_k(s_k, r_k : integer). Therefore, the total conversion ratio is expressed by the following equation.

$$m = \frac{s_1}{r_1}\frac{s_2}{r_2}\cdots\frac{s_K}{r_K} = \prod_{k=1}^{K}\frac{s_k}{r_k} \qquad (1)$$

Figure 8 shows the proposed circuit of the stage 1 and the general stage k. In these figures, the phase of each switch is indicated the equation expressed by s_k and r_k in each square. These values are repeated cyclically 1,2…J, when it is over J or below 1. In the stage 1 (k=1), in order to the series charge of the r_1 capacitors, the phase of the input switch $S_{j,0}$ is expressed by J+1-r_1. Similarly, the output switch $S_{j,1}$ in the stage 1 is expressed by J+1-s_1. The phases of the ground-switch $S_{jg,1}$ and the ring-switch $S_{jr,1}$ don't depend on s_1 and r_1 in the first stage. Also, the next ground-switch $S_{jg,k+1}$ and the output switch $S_{j,k+1}$ shift due to the former output s_{k-1} and the input r_k. That shift amount is expressed by the following equation.

$$p_k = \sum_{l=1}^{k-1}(s_l - r_{l+1}) \qquad (2)$$

As an example, Fig.9 shows the instantaneous equivalent circuit with J=3, K=2, r_1=1, s_1=3, r_2=2, s_2=1, p_2=s_1- r_2=1. As the stage 2 in these figures, the step-down voltage can be obtained by charging multiple capacitors in series. The proposed circuit can obtain the variable conversion ratio by shifting each clock phase. Therefore, the inrush current at start-up can be reduced by setting low conversion ratio at start-up so that the number of charging capacitors at the same time is reduced. The output voltage

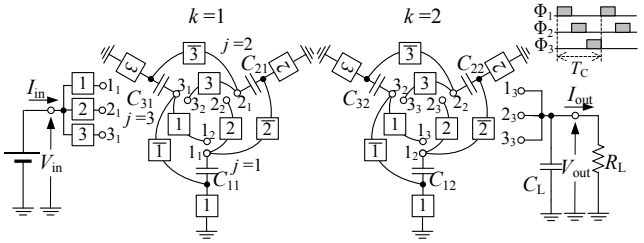
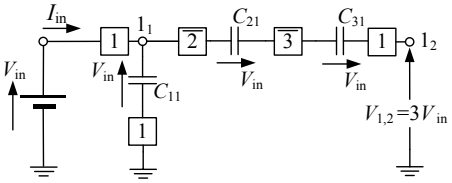
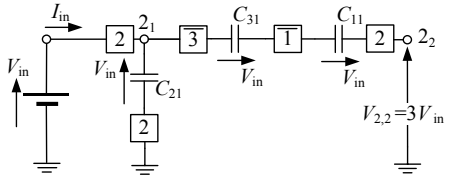


Fig 6 3^K step-up type (J=3, K=2).



(a)State 1 (Φ_1 : high level)



(b) State 2 (Φ_2 : high level)

Fig.7 Instantaneous equivalent circuit of k=1 in Fig.6.

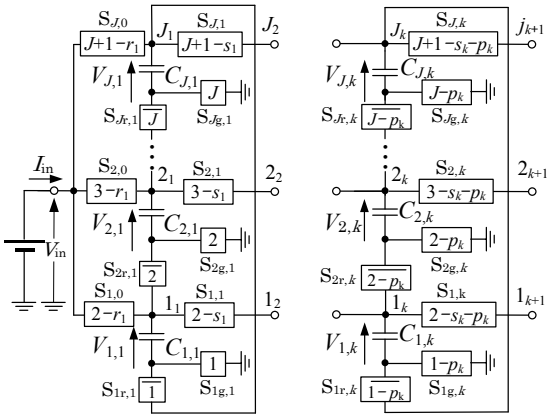
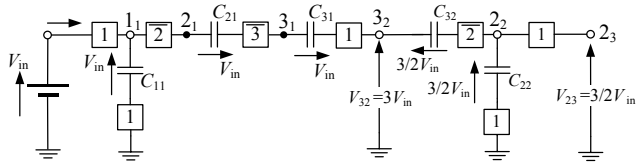
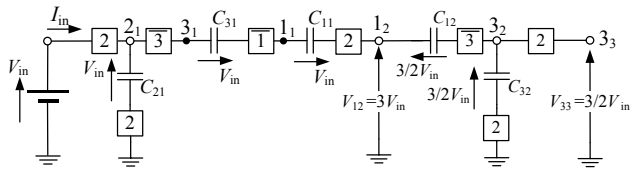


Fig.8 Expression of phase using s_k and r_k.



(a)state 1



(b)state 2

reaches maximum value by increasing the conversion ratio gradually.

2.5 Number of elements versus step-up ratio

In this section, the value of J which can obtain the maximum step-up ratio ($m = J^K$) with the same number of elements is analyzed by changing J and K. The ideal step-up ratio is compared at no-load and steady-state. Therefore, the on-resistance of each switch is ignored. From Figs.1 and 2, the ideal step-up ratio m, the number of capacitors N_C except for C_L, and the number of switches N_{SW} are expressed by the following equations, respectively.

$$m = J^K \quad (3)$$

$$N_C = JK \quad (4)$$

$$N_{SW} = 3JK + J = (3K+1)J \quad (5)$$

Since J capacitors are connected K stages, N_C is shown by Eq.(3). Also, since three switches are needed per one capacitor and the J input switches are connected the input voltage, N_{SW} is shown by Eq.(5). From Eq.(4), substitute $K=N_C/J$ into the Eq.(3) under the condition that N_C is constant.

$$m = J^K = J^{\frac{N_C}{J}} \quad (6)$$

Taking the logarithm of Eq.(6) in order to calculate the J when m becomes the maximum value at the same N_C.

$$\ln m = \ln\left(J^{\frac{N_C}{J}}\right) = \frac{N_C}{J}\ln J \quad (7)$$

Differentiating both sides by J,

$$\frac{dm}{dJ}\frac{1}{m} = -\frac{N_C}{J^2}\ln J + \frac{N_C}{J}\frac{1}{J}$$

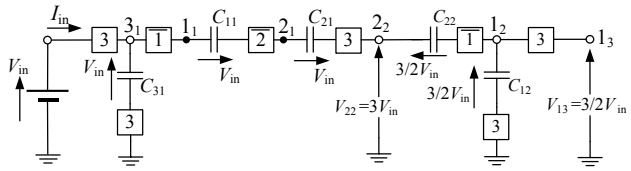
$$\frac{dm}{dJ}\frac{1}{J^{\frac{N_C}{J}}} = -\frac{N_C}{J^2}(1-\ln J)$$

$$\frac{dm}{dJ} = J^{\frac{N_C}{J}-2}(1-\ln J)\,. \quad (8)$$

At $dm/dJ=0$, since m becomes maximum value,

$$J = e = 2.718 \quad (9)$$

Figure 10 shows the characteristics of Eq.(6) when the value of J is continuous. From this figure, m becomes maximum at $J=e$ in spite of N_C. Furthermore, when N_C is increased, these curves become sharp. Figures 11 and 12 show the characteristics of the step-up ratio m versus the number of capacitors N_C and the number of switches N_{SW}, respectively. In these figures, J is an integer value practically. Both figures indicate that the step-up ratio of $J=3$ is maximum with the same number of elements since it is closest integer number to e.



(c)state 3

Fig.9 Instantaneous equivalent circuit

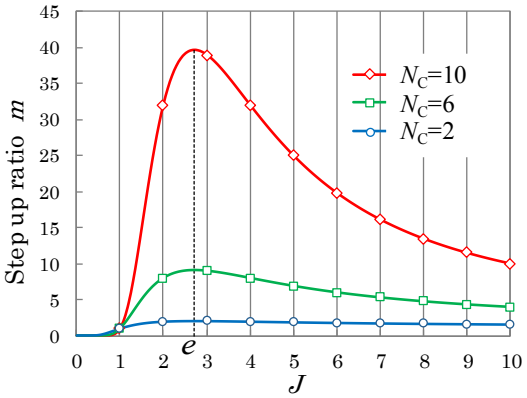


Fig.10 J versus step-up ratio.

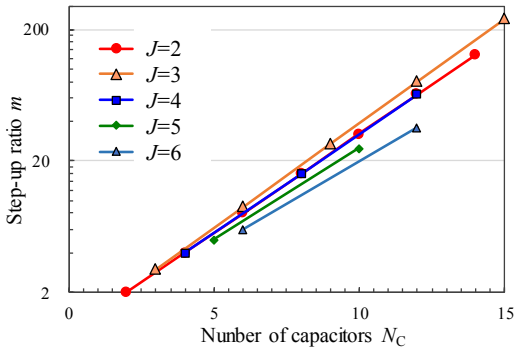


Fig.11 Number of capacitors versus step-up ratio.

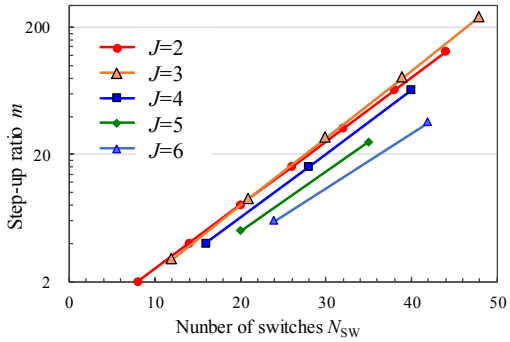


Fig.12 Number of switches versus step-up ratio.

3 HSPICE simulation

In this section, HSPICE simulations are performed in the case of $J=3$ and $J=2$ by considering the on-resistance of each switch. Table 2 shows the circuit parameters used simulations. The on-resistance

r_{on} is only considered for the switching elements. J=2 with K=3 (Fig.4) and J=3 with K=2 (Fig.6) are selected so that the number of capacitors are equal in each circuit. Moreover, the simulations of J=2 type are performed under the conditions A and B. In the condition A, the values of r_{on} and the clock frequency f_c are the same value as those of J=3, respectively. In the condition B, the chip-size and the minimum turn-on/turn-off time of each switch are equal to those of J=3, respectively. Since r_{on} is getting bigger when the number of switches increases on the same chip-size, the r_{on} of J=2 is slightly smaller than that of J=3 (20/21 $\approx$ 0.95 times). Moreover, when the minimum turn-on/turn-off time of each switch is same, f_c is 3/2 times that of J=3 since the clock period T_c of J=2 is 2/3 times.

3.1 Output voltage waveforms at start-up

Figure 13 shows the simulated output voltage waveforms at start-up under the condition that the input voltage V_{in} is 3.3V and no-load. These output voltages V_{out} in both J=2 and J=3 reach a steady-state about 300μs and are converted up to the ideal voltage ($J^K V_{in}$).

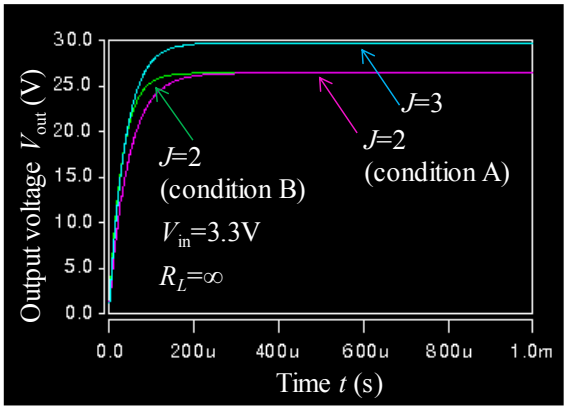


Fig.13 Simulated output voltage waveforms at start-up.

3.2 Output characteristics

Figures 14 and 15 show the characteristics of the power conversion efficiency η and the step-up ratio m, respectively when the output power P_{out} is increased to 30W by changing the load resistance R_L. From these figures, the power conversion efficiency of J=2 under the condition B is about 1.6% higher than that of J=3. Also, the step-up ratio of J=3 is about 10.4% higher than that of J=2 under the condition B. Therefore when the on-resistance of each switch and the clock frequency are equal in each circuit, J=3 has the highest efficiency similarly to the ideal analysis. However, in an actual circuit J=2 has the highest efficiency since the voltage ripple of each capacitor is reduced as the clock frequency is higher.

Table 2 Circuit parameters.

Compared circuit	J=3	J=2	
		ConditionA	ConditionB
Number of capacitors per stage J	3	2	2
Number of cascade stage K	2	3	3
Ideal step-up ratio m=J^K	9	8	8
Number of capacitors N_c	6	6	6
Number of switches N_{sw}	21	20	20
Input voltage V_{in}	3.3V	3.3V	3.3V
Maximum output voltage V_{out_m}	29.7V	26.4V	26.4V
Charge transfer capacitor C	10 μF	10 μF	10 μF
Smoothing capacitor C_L	10 μF	10 μF	10 μF
On-resistance r_{on} of switch	10mΩ	10mΩ	9.52mΩ
Clock frequency f_c	370kHz	370kHz	556kHz
Clock period T_c	2.7μs	2.7μs	1.8μs
Number of clock phase(=J)	3	2	2

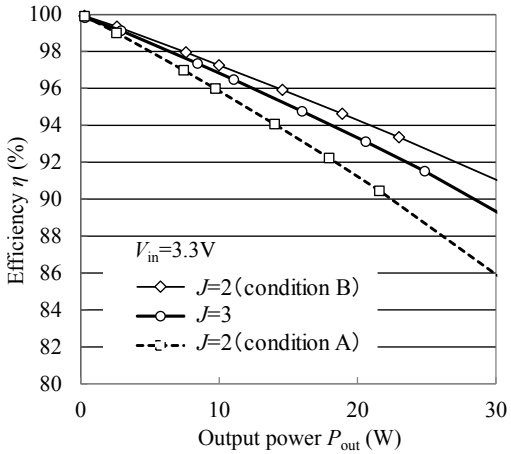


Fig.14 Output power versus efficiency.

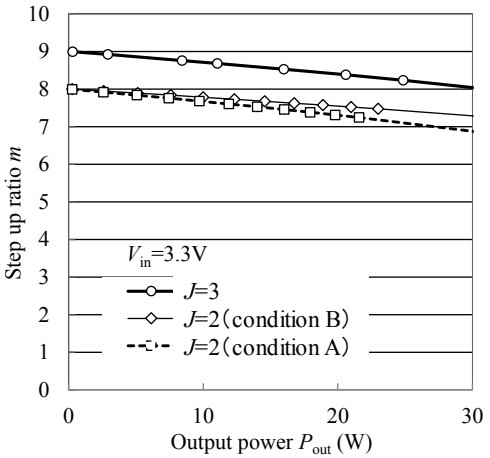


Fig.15 Output power versus step-up ratio.

3.3 Variation of output voltage at start-up

Figures 16 and 17 show the simulated output voltage waveforms and the inrush current waveforms at start-up, respectively under J=3, K=2 and the parameters of Table 2. The conversion ratio is varied 3^{-2}~3^{+2} times and compared with the fixed times step-up ratio 3^2. Table 3 shows variation of the conversion ratio

changing the number of the charging capacitors r_k and the discharging capacitors s_k at start-up. In this table, m_1 and m_2 are the conversion ratios in stage 1 and stage 2, respectively. The conversion ratio is changed per 50 clock periods as shown in this table. At first, m_2 is fixed to the minimum and m_1 is increased gradually from the minimum to the maximum. Next, m_2 is increased gradually. From Fig.17, the inrush current is reduced about 1/3 of the fixed step-up ratio.

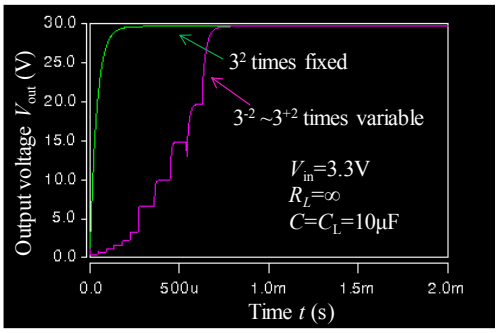


Fig.16 Simulated output voltage waveforms at start-up.

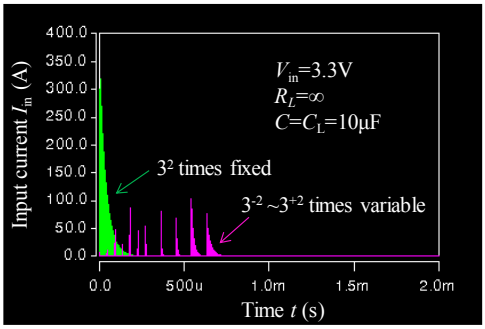


Fig.17 Simulated inrush current waveforms at start-up.

4 Conclusion

In this paper, an exponential step-up/step-down type switched-capacitor power supply is proposed. Furthermore, the ideal maximum step-up ratio is analyzed in general circuits and HSPICE simulations are performed under the 3^K step-up type and the 2^K step-up type. As a result, (1) at no-load simulation, the 3^K step-up type is obtained the highest step-up ratio when the same number of elements, (2) under the load simulation, the 2^K step-up type has the highest power conversion efficiency under the same chip-size and the same turn-on/turn-off time of each switch. Consequently, under a light load, the 3^K step-up type is the optimum since the step-up ratio is the highest with small drop of the efficiency.

Concerning the proposed circuit of the $3^{\pm K}$ type, the inrush current at start-up can be reduced 1/3 by controlling the conversion ratio. In the future, experiment results will be compared with the simulated results.

Table 3 Time variation of conversion ratio.

Time t	m_1	m_2	m=m_1m_2	r_1	s_1	r_2	s_2
0	0.33	0.33	0.11	3	1	3	1
50T_c	0.67	0.33	0.22	3	2	3	1
100T_c	1	0.33	0.33	2	2	3	1
150T_c	1.5	0.33	0.5	2	3	3	1
200T_c	2	0.33	0.67	1	2	3	1
250T_c	3	0.33	1	1	3	3	1
300T_c	3	0.67	2	1	3	3	2
350T_c	3	1	3	1	3	2	2
400T_c	3	1.5	4.5	1	3	2	3
450T_c	3	2	6	1	3	1	2
500T_c	3	3	9	1	3	1	3

References:

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