Charge Pump for Negative High Voltage Generation with Variable Voltage Gain

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Abstract: In this paper, a new cross-coupled charge pump for negative high voltage generation has been proposed. The problem of shoot-through current in the conventional cross-coupled charge pump is solved by a four clock phase scheme. By switching the power supply to each stage based on the supply voltage, a variable voltage gain is obtained. A complete analysis of the interaction between the power efficiency, area, and frequency are presented. The proposed cross-coupled charge pump has been designed to deliver $40\mu A$ with a wide supply range from 2.5V to 5.5V using $0.18\mu m$ high voltage LDMOS technology. In order to have a fixed output voltage within -15±3V, the voltage gain of the charge pump circuit is variable from -3X to -7X and is based on the supply voltage.

Key–Words: Charge pump, dc-dc converter, switched-capacitor power converter, voltage multiplier

1 Introduction

A charge pump circuit (also called switched capacitor DC-DC converter) create a higher voltage than that of the power supply or a negative voltage. Charge pumps have been widely used to generate high voltages in the nonvolatile memories. Among many approaches to the charge pump design, the switched capacitor circuits such as Dickson charge pump [1] are very popular, but the voltage drop across the diodes or diode-connected transistors is too lossy for high efficiency applications. As the alternative to Dickson charge pump circuits, cross-coupled switched capacitor DC-DC converters are more appropriate for battery-driven portable applications [2, 3, 4, 5]. Since the voltage gain for the cross-coupled architecture is higher than that of a Dickson charge pump, the number of stages needed to reach a specific output voltage is reduced. This reduces the parasitic capacitances introduced in the circuit. However, the conventional cross-coupled charge pump has a shoot-through current problem and a limited input voltage range. Therefore, in this letter, a new charge pump based on the cross-coupled charge pump has been proposed to solve the shoot-through current problem and to generate a high negative voltage with a wide supply voltage range. The proposed charge pump can be used to generate negative voltages for substrate bias for reducing leakage in digital designs. Moreover, the charge pump can improve the power efficiency and reduce area cost. The power efficiency and area taken by the charge pump is very important especially in battery-driven portable applications. In the proposed charge pump, the variable voltage gain is realized by switching the power supply to each power stage based on the supply voltage V_{DD}.

2 Proposed Cross-Coupled Charge Pump for Negative High Voltage Generation

An improved negative charge pump design based on cross-couple structure is shown in Figure 1 (a). The operation of the negative charge pump is as follows. Four clock signals have been used to avoid the shoot-through current. When $\Phi1=1$ and $\Phi2=0$, V_A is pushed up to 0V while V_B is pulled down to $-V_{DD}$. At the same time, M3 is turned off and M4 is turned on. As a result, the output voltage of the 1st stage will be pulled down to $-V_{DD}$. The gate voltage of M5 and M6 is grounded, which makes sure they are turned on separately only when V_A or V_B is pulled down to $-V_{DD}$.

The top plate of C2 is pushed up to V_{DD} when $\Phi1=1$ and pulled down to $-V_{DD}$ when $\Phi1=0$. The bottom plate of C2 is pushed up to $-V_{DD}$ and pulled down to $-3V_{DD}$ separately when the supply voltage of the second stage is Vout_1st. In this case, the voltage gain of the 2nd stage is -3X. Finally, if $V_{supply3}$=Vout_2nd, this negative charge pump can provide a maximum
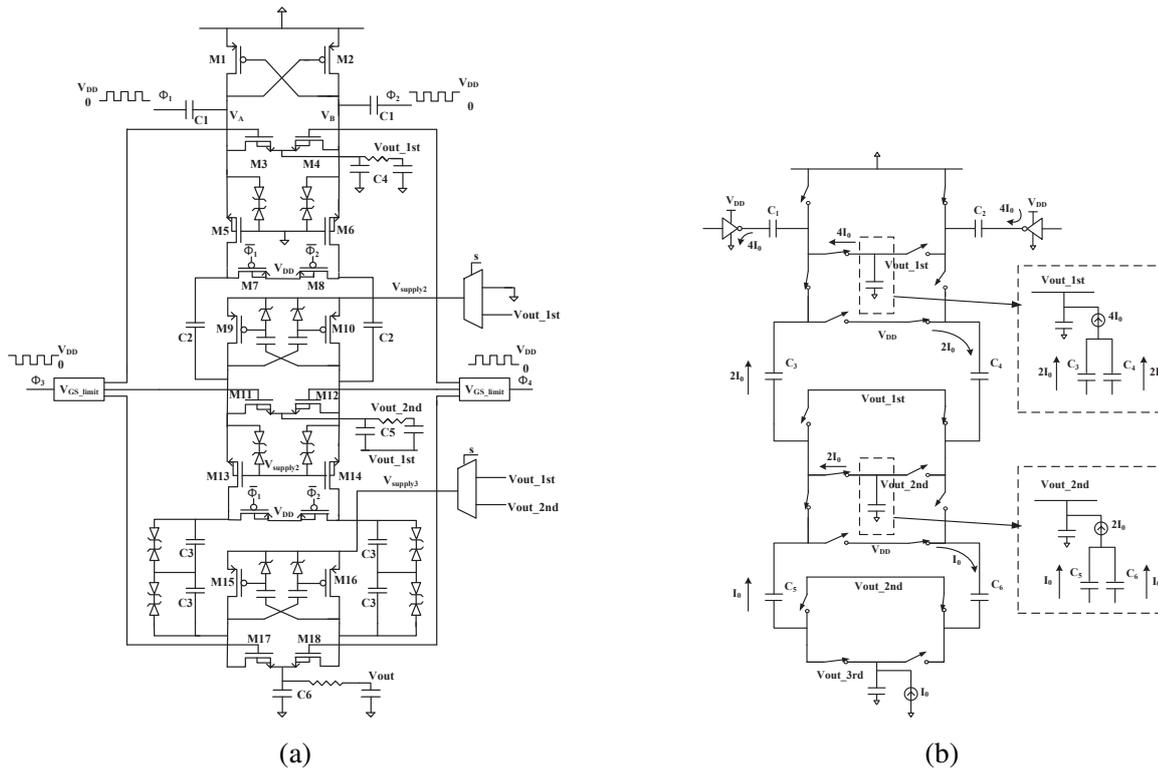
Figure 1: (a) Circuit topology of the proposed negative charge pump, (b) Simplified circuit topology.

voltage gain of -7X. By switching the supply voltage of the 2nd and 3rd stage, a variable conversion ratio can be realized. For process consideration, since the MIM cap can tolerate up to 8V across the pates, the bottom plate of C5 is connected to Vout_1st and capacitor C3 is replaced by two capacitors in series. Although fringing capacitance can be used here, it provides lower power efficiency due to high parasitic capacitance. The only fringing capacitance that can't be avoided is C6. By connecting the gate voltage of M13 and M14 to $V_{supply2}$ instead of Φ3 and Φ4, a larger V_{GS} is allowed, which reduces the RC delay. The charge pump circuit operates at a high-frequency level in order to increase their output power with in a reasonable size of total capacitance used for charge transfer. The operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

The non-overlapping clock phase Φ1 and Φ2 prevent shoot-through current from M1 and M2. However, if these two clock phases are applied to the gate voltage of M3 and M4, the shoot-through current occurs when both of them are at high voltage. This results in higher ripple voltage and power consumption. In order to avoid current flowing from C1 to the output while Φ1 is high, M3 should be turned off. The clock phase Φ3 and Φ4 have been generated. The negative delay is realized by adding a buffer between the in-

verter and the clock generator. As a result, M3 or M4 will be turned on only during the time V_A or V_B is pulled down. Since C2 is charged and discharged by clock phases of Φ1 or Φ2, the clock phases in the 2nd stage are the same as that in the 1st stage. There are two advantages here: First, the clock phases of M9 and M10 are still non-overlapping. Second, the clock phases of Φ3 and Φ4 can still be used to avoid shoot through current from V_{DD} to Vout_2^{nd}. This applies to the 3rd stage too. This means the four clock scheme is applicable to all the three stages in this charge pump circuit to avoid the shoot-through current.

3 Power, Area and Frequency Considerations

In order to optimize the circuit performance, the interaction among the power, area, and frequency has to be analyzed. Figure 1 (b) is the simplified diagram of the proposed negative charge pump circuit with the voltage gain of -7X. Each MOSFET has been replaced by a two-phase switch. For the cross-coupled structure, the charging and discharging status are switched every half period. For example, suppose the loading current is I_0, while the left half part of the circuit is being discharged by the load current, the right half part of the circuit is being charged from the power supply. In this

case, the average current flowing through C_5 equals to I_0. Simultaneously, C_6 is being charged by the same amount of average current I_0 in order to restore the charge that has been discharged during the previous half period. At the 2nd output stage, the equivalent load current is now $2I_0$, consisting of the discharging currents flowing through C_5 as well as the charging current flowing through C_6. The average current flowing through the capacitors C_3 and C_4 in the 2nd stage increases $2I_0$ too. Based on the same analysis, we can have the conclusion that the equivalent loading current at the 1st output stage is $4I_0$ and the current flowing through C_1 and C_2 is also $4I_0$.

Given the analysis above, the output voltage of the proposed negative charge pump circuit with loading current I_0 can be calculated as following:

$$V_{out\_3rd} = -7V_{DD} + 4I_0t/C_1 + 2I_0t/C_3 + I_0t/C_5$$
$$= -7V_{DD} + I_0t(4/C_1 + 2/C_2 + 1/C_5) \quad (1)$$

In order to analyze the power efficiency, the input and output power is also calculated. For the input power, there are three sources:

$$P_{in} = 4V_{DD}I_0 + 2V_{DD}I_0 + V_{DD}I_0 = 7V_{DD}I_0 \quad (2)$$

Given the output voltage V_{out_3rd} and load current I_{load}, the output power is:

$$P_{out} = <V_{out\_3rd}> *I_{load} = 7V_{DD}I_{load} - \frac{3I_0^2}{Cf} \quad (3)$$

Comparing Eqn.(2) and (3), the power is dissipated on the MOSFETs when the gate is switched on and off. The power efficiency can be calculated as follows:

$$PowerEfficiency = \frac{P_{out}}{P_{in}}$$
$$= \frac{7V_{DD}I_0 - \frac{3I_0^2}{Cf} - \frac{3\alpha I_0^2}{C_Cf} - \frac{3\beta I_0^2}{C_{MOS}f}}{7V_{DD}I_0 + (E_{C\_C} + E_{C\_MOS})f}$$
$$= \frac{7V_{DD}I_0f - 3(\frac{I_0^2}{C} + \frac{\alpha I_0^2}{C_c} + \frac{\beta I_0^2}{C_{MOS}})}{(E_{C\_C} + E_{C\_MOS})f^2 + 7V_{DD}I_0f} \quad (4)$$

where C_C and C_{MOS} are the parasitic capacitance of MIM capacitors and transistors, respectively. Also E_{C-C} and E_{C-MOS} are the corresponding energy consumption due to the voltage switch, which is constant within one period. The value of αI_0 and βI_0 represents the equivalent current flowing through the parasitic capacitors and is determined by the type of technology used.
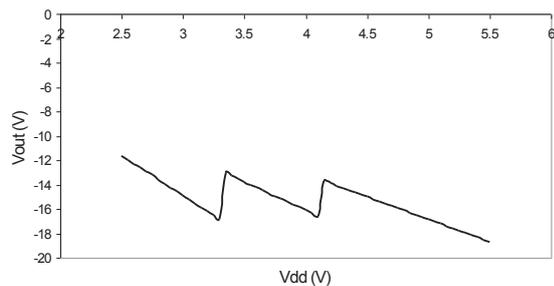
In Eqn.(4), the input power is larger than $7V_{DD}I_0$ since the charging current has to be larger than I_0 in order to restore the additional charge dissipated on the parasitic capacitors. The load current flowing through the capacitors will reduce the output voltage and is a source of power consumption. However, the voltage switch on the parasitic capacitors only consumes power and has no effect on output the voltage. While the frequency increases, the power efficiency increases first and then decreases, which means, for a given area, there always exists an optimized switching frequency that could provide a maximum power efficiency. When the area of capacitors increase to a certain value, the power efficiency starts to decrease since the parasitic capacitors from the MOS transistors dominates the power performance. The parameters of the charge pump circuit can be optimized by sweeping the frequency and area repeatedly until the maximum power efficiency is obtained.
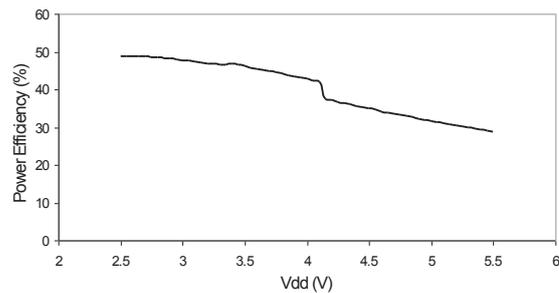
4 Simulation Results

The capacitors in the third stage should be replaced by two caps in series in order to avoid the use of fringing capacitors, which will increase the area by four times. Based on the analysis above, in order to have the maximum voltage gain, the capacitors from the stage should be resized as 4:2:1. As a result, the area cost of the two capacitors in series is acceptable since the last stage has the minimum capacitance. However, in order to reduce the parasitic capacitors, capacitors from the 1st to the 3rd are sized as 8:4:1 ratio.

Given the optimized parameters, the proposed charge pump circuit is simulated with 40uA load current at 1MHz operating frequency. Figure 2 (a) and (b) show the performance of the negative charge pump with the area of 0.5 mm^2 and supply voltage range from 2.5V to 5.5V. The output voltage is within -15±3V with variable voltage gains of -4X, -5X, and -7X separately. The power efficiency of the proposed negative charge pump circuit is from 30% to 50% which is lower than that of charge pumps using off-chip capacitors due to the high parasitic capacitance. In order to reduce the fabrication cost, the area is further reduced to 0.25 mm^2. In this case, the output voltage is within -14.5±3.5V and the power efficiency is from 18% to 38%.

Another important issue in charge pump operation is the operating frequency. Figure 2 (c) and (d) show the output voltage and efficiency as a function of operating frequency. The output voltage is inversely proportional to the switching frequency as shown in Figure 2(c) as expected in (2). The charge pump has a maximum efficiency of 50% at around 1MHz switch-

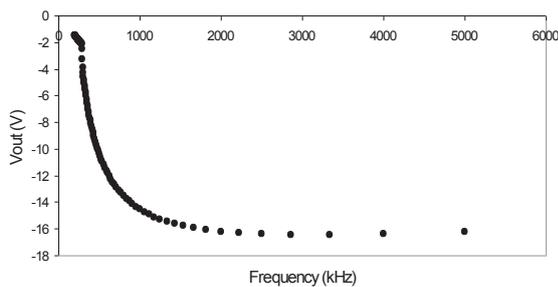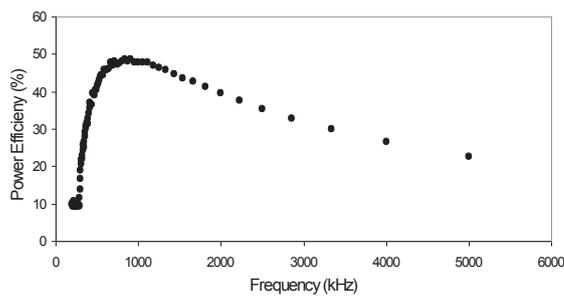(a) Output voltage vs. frequency

(b)Efficiency vs. frequency

(c) Output voltage vs. V_{DD} @ 0.5 mm^2

(d) Efficiency vs. V_{DD} @ 0.5 mm^2

Figure 2: (a) and (b) are the output voltage and Efficiency as a function of operating frequency @ 0.5 mm^2 area with $40\mu A$ load current and 3V power supply; (c) and (d) are the output voltage and efficiency of the negative charge pump circuit as a function of supply voltage with $40\mu A$ load current.

ing frequency as shown in Figure 2(d), which meets well with Eqn.(4). Considering both output voltage and efficiency, the optimized frequency of 1MHz is selected.

5   Conclusion

In this paper, a negative charge pump circuit with variable voltage gains is designed and implemented using $0.18\mu m$ high voltage LDMOS technology. The proposed charge pump circuit operates at 1MHz frequency with $40\mu A$ current load with a wide power supply range from 2.5V to 5.5V. The clock overlapping issue is resolved by a four clock phase scheme. In order to have a fixed output voltage within -15±3V, the voltage gain of the charge pump circuit is variable from -3X to -7X and is based on the supply voltage. Compared to the area size of 0.5 mm^2, power efficiency of the 0.25 mm^2 designed is reduced by 10% at the same voltage gain for lower area cost.

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