Composite Second Generation Current Conveyor Based Tunable MOS-C Quadrature Sinusoidal Oscillator Design and Comparative Performance Analysis

HASAN ÇİÇEKLİ, AHMET GÖKÇEN
Electrical and Electronics Engineering Dept.
Mustafa Kemal University
TURKEY
hcicekli@gmail.com, ahmetgkcn@gmail.com

Abstract:-In this paper, a new voltage mode tunable MOS-C quadrature sinusoidal oscillator circuit employing composite second-generation current conveyor (CCCII) is presented. The proposed topology employs two CCCII and four grounded components. CCCII is implemented by using two CCIIs as sub-circuit. This implementation technique makes it possible to employ the circuit by commercially available integrated circuits that can be used as current conveyor such as AD844. The validity of the proposed circuit is verified by PSPICE simulation program. Simulation is performed for both CMOS based CCCII using MOSIS 0.35 μm process parameters and AD844 based CCCII using the Spice Macromodel parameters of AD844. It is seen that the simulation results agree well with the theoretical analysis and the proposed circuit achieves a good THD performance. The resistors used in the circuit are implemented by using MOS transistors. So, the proposed circuit is fully integrable and oscillation frequency can be tuned by external MOS gate voltages. Also, a comparative performance analysis is performed for the two circuits employing CCII and CCCII which are belong to the same topology. It is stated that employing CCCII improve the circuit performance significantly when compared to the same topology employing CCII for both CMOS and AD844 based implementations.

Key-Words:-Analog integrated circuits, Current conveyors, MOS-C realization, Quadrature sinusoidal oscilltors.

1 Introduction

Quadrature sinusoidal oscillators find wide range of applications in telecommunication, signal processing, instrumentation, measurement and control systems and they can offer sinusoidal signals with 90° phase difference that is a requirement for some devices such as quadrature mixers, phase modulators and single-sideband generators [1]-[8]. For measurement purposes, quadrature sinusoidal oscillators are used as vector generators or selective voltmeters [9].

During recent years, several implementations of quadrature sinusoidal oscillators employing different high performance active building blocks such as current feedback operational amplifier(CFOA), different types of current conveyor, four terminal floating nullor (FTFN), current follower, current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) and operational transresistance amplifier (OTRA) have been reported [4]-[24]. However, there is one or more drawbacks of these reported circuits such as excessive use of the passive elements, especially the external resistors, use of multiple-output active elements that makes the circuits more complicated, use of floating capacitor, which is not convenient for integration and the lack of electronic adjustment of the oscillation frequency. The aim of this work is to present a new CCCII based tuneable MOS-C quadrature sinusoidal oscillator circuit, realize it by using two different implementation of CCCII and to do a comparative performance analysis to see how the CCCII based circuits have improved performance when compared to the same topology employing CCII. The features of the proposed circuit are as follows:

a) The capacitors and resistors used in the circuit are all grounded.
b) Resistors are implemented by MOS transistors, so the circuit is suitable for integration.
c) Electronic adjustment of the oscillation frequency.
d) Providing good characteristic with lower distortion than the oscillator circuit employing CCII.
e) Using only two active elements with single outputs.
f) Possibility to adjust the oscillation frequency without affecting the oscillation condition.
g) Possibility to employ the circuit by using commercially available AD844.

In the open literature we have found, among the voltage mode quadrature sinusoidal oscillator circuits, none of them employs CCCII and have the whole features shown above.

The outline of this paper is as follows: In section 2, the circuit description of CCCII is given. Also, the implementation technique of CCCII by using two CCIIs is schematically expressed. Proposed circuit topology is given in section 3. In section 4, MOS-C realization of the proposed circuit is presented.

Simulation results, output waveforms and THD values of the presented circuit are given in section 5 for both CMOS and AD844 based implementation of CCCII. The comparative performance analysis of the two circuits separately employing CCII and CCCII as active element, is also done in this step. Finally, the conclusion is given in section 6.

2 Circuit Description of CCCII

The current conveyor is still emerging as one of the most important current-mode active building block and different types of current conveyor enable the researchers to design multipurpose circuits to be used in analog signal processing. The composite second generation current conveyor is a three terminal building block and it's schematic symbol is as shown in Fig. 1.

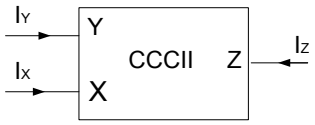


Fig. 1. The schematic symbol of CCCII

The defining equation of CCCII can be given as

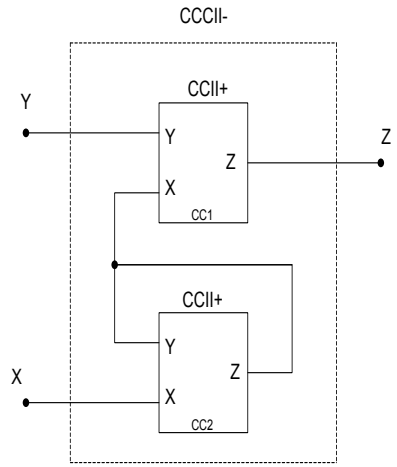
$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

The positive sign at the third row applies to the CCCII+, whereas the negative sign applies to the CCCII-.

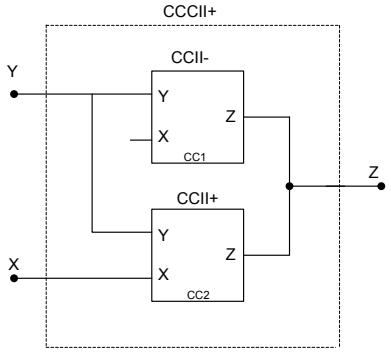
CCCII can be constructed of two second generation current conveyors as shown in Fig.2 [25]. It is a useful technique to improve the performance of the current conveyor by either lowering the x-terminal impedance or enhancing the y-terminal admittance. This provides the CCCII based circuits have better output characteristics when compared to the same circuit topology employing CCII. The realization of CCCII- can be achieved using two CCCII+. In the CCCII- configuration, the lower current conveyor which is denoted as CC2, works as a negative impedance conveyor and consequently the X-terminal impedance of the CCCII- is

$$Z_{x(composite)} = Z_{x1} + A_{i2}Z_{x2} \cong Z_{x1} - Z_{x2} \quad (2)$$

It is clearly seen from (2) that the current gain A_{i2} should be designed slightly lower than the first in order to prevent a negative X-terminal impedance for the composite conveyor. In addition, all even order nonlinearities in Z_{x1} and Z_{x2} are effectively summed together and hence X-terminal impedance nonlinearity is increased.



(a)



(b)

Fig. 2 Composite second-generation current conveyor implementation using CCIIs.
(a) Composite CCII- with lower Z_x.
(b) Composite CCII+ with enhanced Y_x.

Fortunately, in most cases the nonlinearity of the X-terminal impedance has little effect on the total amplifier distortion [25].

It is possible to implement the CCCII by using the current conveyor blocks as sub-circuit. This current conveyor based CCCII implementation method makes it possible to employ the circuit by using commercially available integrated circuits that can be used as current conveyor such as AD844.

3 Proposed Circuit Topology

The proposed CCCII based voltage-mode quadrature sinusoidal oscillator topology is shown in Fig. 3. The circuit analysis of the proposed quadrature sinusoidal oscillator yields the following characteristic equation

$$s^2C_1C_2 + G_1G_2 = 0 \quad (3)$$

The radian frequency of oscillation is

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (4)$$

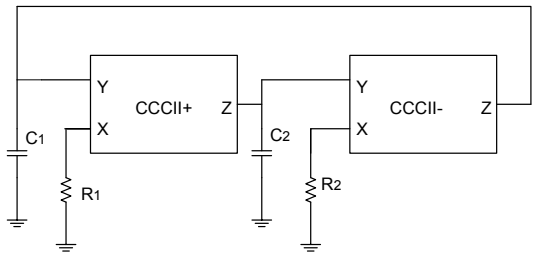


Fig. 3 Proposed circuit topology

The sensitivity of radian frequency to the passive components are all calculated as

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -1/2 \quad (5)$$

As it is shown in (5), the sensitivities of passive components are quite low.

4 MOS-C Realization of the Proposed Circuit

A linear resistor can be realized by using parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in Fig. 4 [26]. This method cancels out the non-linearity of the MOSFET significantly.

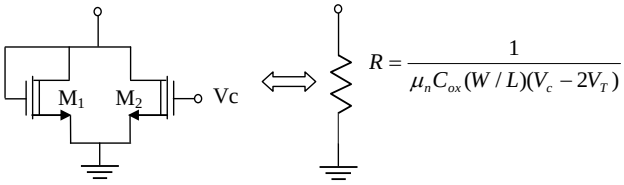


Fig. 4 Linear resistor realization using nonlinearity cancellation technique in parallel connection of two NMOS transistors

W and L are the channel width and length and V_T is the threshold voltage of the MOSFET, μ_n is the free electron mobility in the channel and C_{ox} is the gate oxide capacitance per unit area. The resistance values are tunable via V_C and since the even-order nonlinearities are cancelled out, it operates linearly over an extended voltage range. For achieving the fully MOS-C realization of the proposed oscillator circuit, the resistors must change with their MOS transistor conjugates. Fig. 5 shows MOS-C realization of the proposed circuit.

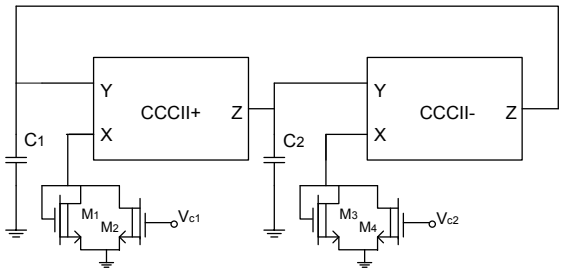


Fig. 5 MOS-C realization of the proposed circuit

It can be clearly seen from this figure that the oscillation frequency of the circuit can be controlled by gate voltages V_{C1} and V_{C2} of the MOS transistors.

5 Simulation Results

The proposed circuit's performance has been evaluated for two different implementation of CCCII by PSPICE simulation program using the MOSIS 0.35 µm CMOS process parameters and AD844 Macro-model parameters.

5.1 CMOS Based CCCII Simulation Results

The circuit schematic of dual output CMOS CCII used to implement the CCCII is shown in Fig. 6 [27]. The circuit is supplied with symmetrical voltages of ±1.25 V. W/L parameters of MOS transistors used in simulation are given in Table 1.

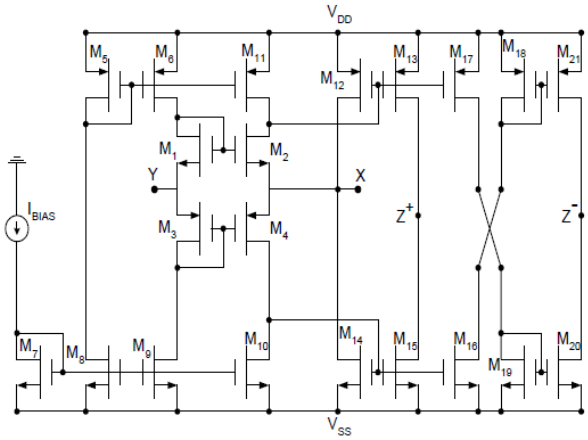


Fig. 6 Circuit schematic of dual output CMOS CCII used for CCCII implementation

Table 1 Dimensions of the transistors

Transistor	*W(µm)*	*L(µm)*
M1, M2	12	0.35
M3, M4	36	0.35
M5-M6, M11-M13, M17-M18, M21	18	0.35
M7-M10, M14-M16, M19-M20	6	0.35

The biasing currents are taken *as* $I_{B(CCII+)} = I_{B(CCII-)} = 5\ \mu A$. The passive component values taken in simulation are given in Table 2. In the simulation, the dimensions of MOS transistors used to realize the resistors in Fig. 5, are taken as W=8.3 µm and L=0.7µm for all M1, M2, M3 and M4. MOS gate voltages are taken as V_{C1}= V_{C2} =2.9 V and the resistor value is found as $R \cong 254\ \Omega$.

Table 2 Passive component values

R_1	R_2	C_1	C_2
250 Ω	250 Ω	500 pF	500 pF

The calculated value of the oscillation frequency (f_0) is 1.27 MHz. In order to do performance comparison, two simulations are performed for the circuits employing CCII and CCCII. The oscillation frequency and total harmonic distortion (THD) values obtained from the simulations are given in Table 3. *V(1)* and *V(2)* denote the voltages across the capacitors C_1 and C_2.

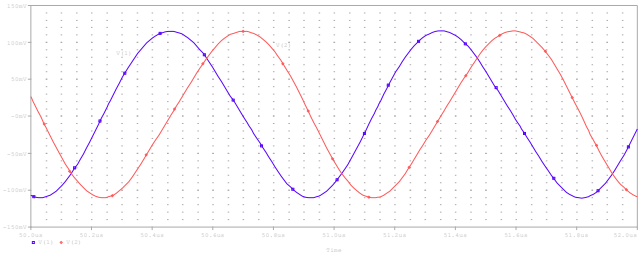
Table 3 Oscillation frequency and THD values for CMOS implementation

	Circuit employing CCII		**Circuit employing CCCII**	
Oscillation Frequency (MHz)	1.15		1.22	
THD %	*V(1)*	*V(2)*	*V(1)*	*V(2)*
	6.1	8.5	3.1	3.9

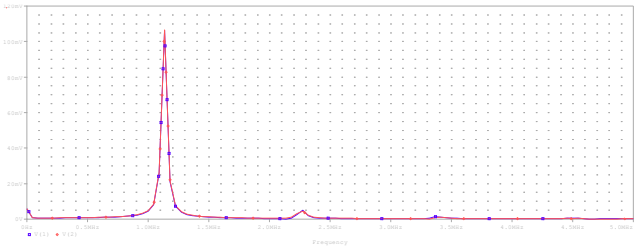
As it is seen from Table 3, simulation results agree well with the theoretical calculations and the proposed circuit achieves a good THD performance. Results also show that the oscillation frequency and THD values of the circuit employing CCCII are significantly better than the values of the circuit employing CCII.

The power dissipation of the circuit employing CCCII is 2.69 mW for the initial voltage of 0.2 mV given to C_1. The quadrature phase error is 1.98 % and the oscillation frequency deviation error is 3.93 % for the circuit employing CCCII.

The voltage waveforms of the proposed circuit employing CMOS based CCCII are shown in Fig.7.



(a)



(b)

Fig. 7 Simulation results of the quadrature sinusoidal oscillator circuit employing CMOS based CCCII. (a) Steady state waveform (b) Frequency spectrum

In order to evaluate the tunability of oscillation frequency, the gate voltages of M2 and M4, which are denoted as V_{C1} and V_{C2}, are varied in a range of 2-3 V. The frequency values obtained by the variations of V_{C1} and V_{C2} are given in Table 4.

Table 4 The oscillation frequency and THD values obtained by the variation of V_{C1} and V_{C2}

V_{C1}, V_{C2} (V)	**Oscillation Frequency (MHz)**	**THD %**	
		V(1)	*V(2)*
2.0	0.87	1.0	1.7
2.2	0.96	1.6	2.5
2.4	1.04	0.9	1.3
2.6	1.10	1.0	0.8
2.8	1.19	2.1	2.4
3.0	1.26	5.4	3.7

5.2 AD844 Based CCCII Simulation Results

Another simulation is performed by using the AD844 SPICE Macro-model parameters to check the workability of the presented circuit by using commercially available integrated circuit. The circuit is supplied with symmetrical ±10 V and the passive component values taken in simulation are given in Table 5.

Table 5 Passive component values

R_1	R_2	C_1	C_2
1 kΩ	1 kΩ	75 pF	75 pF

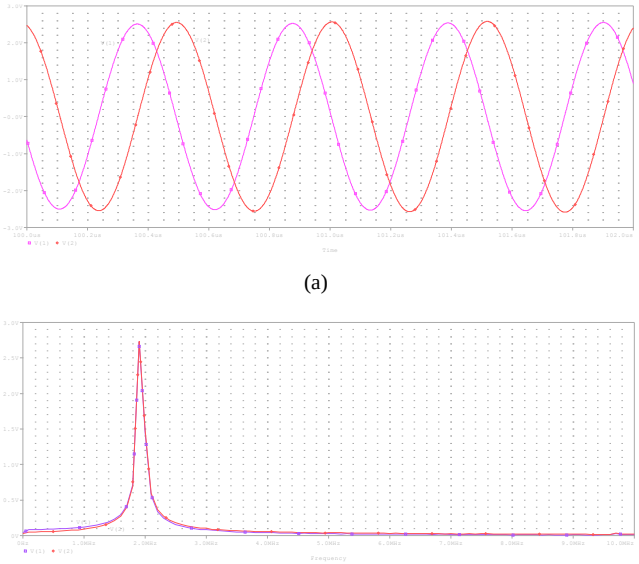
These component values yields an oscillation frequency (f_0) of 2.12 MHz. As it is done before, two simulations are performed for the circuits employing CCII and CCCII. The oscillation frequency and THD values obtained from the simulations are given in Table 6. The voltage waveforms of the proposed circuit employing AD844 based CCCII are shown in Fig.8.

Table 6 Oscillation frequency and THD values for AD844 implementation

	Circuit employing CCII		**Circuit employing CCCII**	
Oscillation Frequency (MHz)	1.91		1.97	
THD %	*V(1)*	*V(2)*	*V(1)*	*V(2)*
	2.4	3.3	0.8	1.1

Also in AD844 based CCCII implementation, the oscillation frequency and THD values of the circuit are better than the values of the circuit employing CCII as it is seen in Table 6. The power dissipation of the circuit employing CCCII is 521 mW for the initial voltage of 0.1 mV given to C_1. The quadrature phase

error is 1.55 % and the oscillation frequency deviation error is 7.07 % for the circuit employing CCCII.



(a)

(b)

Fig. 8 Simulation results of the quadrature sinusoidal oscillator circuit employing AD844 based CCCII.
(a) Steady state waveform (b) Frequency spectrum

6 Conclusion

A new voltage-mode tuneable MOS-C quadrature sinusoidal oscillator based on CCCII has been presented. The resistors used in the circuit are implemented by MOS transistors and the capacitors are all grounded. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. The simulation results agree well with the theoretical analysis. The proposed circuit achieves a good THD performance and the quadrature phase error is quite low. It is stated that the CCCII employing circuits improve the circuit performance significantly when compared to the same topology employing CCII. The workability of the presented circuit is also verified by using commercially available AD844. Taking these advantages into consideration, it is expected that the proposed circuit will be useful in various telecommunication and signal processing applications. As future work, this circuit topology can be improved by adding cascade connection of identical stages to achieve multiphase sinusoidal oscillator which provide more than two signals equally spaced in phase.

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