Analysis and Design of Wireless Power Transfer: A Capacitive Based Method for Low Power Applications

^{1,2,a}Kamarudin.Kh, ^{1,b}ShakirSaat, ^{1,c}Y.Yusmarnita, ^{1,d}Norezmi Jamal ¹Faculty of Electronic and Computer Engineering Universiti Teknikal Malaysia Melaka ²Faculty of Electrical Engineering Universiti Teknologi Mara ^akhairul@johor.uitm.edu.my, ^bshakir@utem.edu.my, ^cyusmarnita@utem.edu.my,^djamalnorezmi@gmail.com

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1 Introduction

Wireless Power Transfer (WPT) is a process of transferring power from a primary circuit to another pick up circuit without any physical contact between them. It is highly advantageous in where physical wires are a hassle. Several schemes for wireless power transfer exist such as Inductive, Capacitive, Laser, Microwave and others. Among these, Inductive Power Transfer (IPT) is a most popular one since the last two decade due to its inherently simple approach in manipulating magnetic flux. However, the disadvantages of IPT are; 1.Inability to penetrate metal and 2. High standing power losses which might causes eddy current loss [1].

Recently, the CPT approach has been proposed to overcome the IPT problems such as its failure to operate over metallic obstacle [2, 3]. To be specific, in the capacitive interface the field is confined between conductive plates, alleviating the need for magnetic flux guiding and shielding components that add bulk and cost to conductive solution [4]. In contrast to inductive based method, the simplicity and low cost of capacitive interfaces makes them very attractive for wireless charging stations and galvanically isolated power supplies. However, conventional CPT solutions are widely used in either larger capacitors or lower power applications, such as coupling of power and data between integrated circuits or transmitting power and data to bio signal instrumentation systems [4].Therefore, this paper uses series resonance approach that enables efficient high frequency and moderate voltage operation through soft-switching approach. Furthermore, the Class E converter is proposed to be used in this paper to improve the efficiency of the CPT system. This paper contributes to the implementation of a Class E Amplifier to be used in a CPT system which allows for a highly efficient CPT system.

This paper is organized as follows: The operational principles and analysis of a Class E MOSFET Converter is explained in Section 2. This section also presents the simulated and experimental results of the Class E Converter. In Section 3, the modeling and design of a CPT System is presented. This section also highlights the simulation of the system and its experimental results. The conclusion is then given in Section 4.

2 Class E MOSFET Converter

This section explains the analysis and design of Class E MOSFET converter. It will focus on the key

operation of a Class E converter. This work focuses on a simplified analytical model for the class-E switch-mode amplifier using an inductive choke in the bias circuit, as constructed in [5].

2.1 Class E Operation

Class E operation is based on the hypothesis that the active device is used as a switch, which is different from the usual current source mode. In the usual setup of a current source mode, the active device is not implemented as a total switch. The popularity of this Class E converter comes from the fact that it is simple in design, 100% theoretical efficiency and inherent robustness to parameter variations circuit [6].

In order to achieve a high efficiency, the peak of the current and voltage waveforms for the switch must be displaced in the time. When the switch is turned on, the current flows through it with no voltage drop across. On the opposite, there will be a voltage induced when the switch is off, blocking any flow.

The Basic class E Amplifier is as shown in Figure 1.



Figure 1: The basic class E Amplifier

Based on the Figure 1, the active device is represented by an ideal switch. While in practical, we would use the diverse class of power electronic switching devices such as a BJT, MOSFET, IGBT or etc. The shunt capacitance, C_1 is added to the switch, although at higher frequencies most or all of this may be provided by the device capacitance. The output series tuned circuit; L_2 - C_2 resonates below the operating frequency, so that there is excessive inductive reactance



Figure 2: The output voltage and current across switching [7]

As shown in Figure 2, when the switch is on, the drain current, I_D is at maximum level and drain voltage is zero. However, when the switch is off, the I_D is zero and V_D is at maximum point. From this argument, we know that the switching loss of Class E converter is zero. It is also known as Zero Voltage Switching (ZVS) where the inductor retrieves the loss charge on the C_1 capacitor and no sudden current impels are drawn to the switch [8] such in Figure 2. This gives a great advantage of applying Class E type in the high frequency application [6].

2.2 Design of Class E MOSFET Converter



Figure 3: Block Diagram design Class E MOSFETs Inverter

The process of designing a Class E MOSFET converter is shown in Figure 3. The analysis is simplified by first assuming that the switch is perfect in which it is instantaneous in its opening and closing action leading to it being loss-less. Secondly, the Radio Frequency (RF) choke on the DC supply is set to look like an ideal open circuit at the frequency of operation. Thirdly, the switch duty cycle is set at an optimal 50%. Next, the quality factor, Q of the load RLC circuit should be high enough

so that the passage of harmonic signal to the load is negligible. Finally, the Class E conditions is set to be fulfilled when the switch closes at $t = 2\pi n$. The voltage across the switch is given by V(ωt) and the current through the switch is denoted by I(ωt) at any instant in normalised time (ωt).

Since the choke inductor is assumed to be ideal (no resistance) the supply voltage V_{CC} must be equivalent to the average voltage appearing across the switch/shunt capacitor over a full on-off cycle. This produces the first important design relationship.

$$V_{cc} = \frac{1}{2\pi} \int_{\pi}^{2\pi} V(\omega t) d(\omega t) = \frac{I_0}{\pi \omega c}$$
(1)

Since the switch is defined to be lossless and the class-E conditions are satisfied, the DC power provided by the bias DC source should be equal to the power dissipated in the load resistor. Defining the resistance to be that before the L-match to be R, we have

$$I_0 V_{CC} = \frac{1}{2} I_{r0}^2 R \tag{2}$$

Hence, the power delivered to the load is

$$P_{load} = \frac{8V_{CC}^2}{(\pi^2 + 4)R} \tag{3}$$

Based on the calculations so far, we can specify the amplifier power output in terms of the V_{CC} and load resistance. We can also specify I_0 and hence shunt capacitance C. Note that the shunt capacitance C contains the parasitic collector (or drain) capacitance of the switch. Hence, this will affect the choice of switching transistor. The design process involves finding a good combination of Vcc, R, C that allows for a realisable amplifier. Generally R should not be too small otherwise the series inductor will be too small to be physically realisable.

The next step is to treat the series resonant part of the output circuit, L_{res} and C_l . The center frequency and load resistance R are already specified in the design. What remains is to specify the Q-factor of the resonant circuit. Any value above 5-7 should suffice. Lower Qs will require "some tweaking" of the excess inductance and shunt capacitor values as harmonic leakage becomes significant. Low-Q permits operation over wider bandwidths, but at the cost of more harmonic leakage (unless a higher-order output filter network is used). From a straightforward analysis of a series resonant LCR network we can find the values of resonant capacitance and inductance:

$$C_1 = \frac{1}{\omega QR} \tag{4}$$

$$L_{res} = \frac{QR}{\omega} \tag{5}$$

$$L_0 = C_m R R_1 \tag{6}$$

The final value for the series inductor corresponds to the sum of all the computed inductances:

$$L_{total} = L_{ext} + L_{res} + L_0 \tag{7}$$

For analytical expressions of the output power and the power conversion efficiency are derived by using the waveform equations given by addition of equivalent series resistances. In real circuits, the power losses occur in the parasitic resistances of each component. It is assumed that the parasitic resistances are small enough not to affect the waveforms.

The specifications that are needed in this work are given in Table 1.

Table 1: Amplifier specification

V _{cc}	12V
Pload	5W
ω	2π1MHz
Q	10
R ₁	50Ω

The value of the RF choke inductor is not specified, but in practical implementation, this value is not so critical because as long as its impedance is at least an order of magnitude higher than the load resistance and it is not self-resonant at the first three or four harmonics, then it should give a good result as mentioned in [9].

The current drawn from the DC supply is given as follows:

$$I_o = \frac{P_{load}}{V_{cc}} = \frac{5}{12} = 0.4167A$$
(8)

Hence, we need a shunt capacitance of

$$C = \frac{I_o}{\omega \pi V_{cc}} = \frac{0.4167}{(2\pi 1M)\pi (12)} = 1.7592nF$$
(9)

This means we need a transistor with a parasitic collector/drain capacitance less than this value. The required load resistance seen by the switch is computed as follows

$$R = \frac{8V_{cc}^2}{(\pi^2 + 4)P_{load}} = \frac{(8)(144)}{(13.869)(5)} = 16.6\Omega$$
(10)

The excess series inductance L_{ext} is then found from

$$L_{ext} = \frac{1.153R}{\omega} = \frac{1.153(16.6)}{2\pi 1M} = 3.046mH$$
(11)

At this frequency, this value of inductance is realizable and comes with multiple options already available in the market.

Next, we move on to computing the resonant circuit parameters. Based on the specified Q, we have

$$C_1 = \frac{1}{QR\omega} = \frac{1}{(10)(16.6)(2\pi 1M)} = 0.959nF$$
(12)

$$L_{res} = \frac{QR}{\omega} = \frac{(10)(16.6)}{2\pi 1M} = 26.42\,\mu H \tag{13}$$

Finally, we design the L-match using

$$C_{m} = \frac{1}{\omega R_{1}} \sqrt{\frac{R_{1}}{R} - 1} = \sqrt{\frac{\frac{50}{16.6} - 1}{(2\pi 1M)(50)}} = 4.515nF$$
(14)

$$L_0 = RR_1 C_m = 3.7475 \mu H \tag{15}$$

The value of the series inductor is the sum of all the computed inductances which is equal to 33.214mH. Based on the calculated values which are described in the previous paragraph, the simulation of Class E

MOSFET is carried out using SPICE as shown in Figure 4.



Figure 4: Circuit Simulation Class E Amplifier

The results of drain voltage, V_D and drain current, I_D is shown in Figure 5. Based on Figure 5, we can easily see that the switching loss of this Class E converter is zero.



Figure 5: Switching Results of Class E MOSFETs Converter

This confirmed that the calculated components are acceptable and in addition, implementable. This also validated the stated theory as mentioned in [10]. From the results of Figure 5 we can also see that the zero voltage switching is obtained perfectly in the simulation.



Figure 6: Simulation Result of Output Voltage and Output Current

The output current and the output voltage are shown in Figure 6. The efficiency of the proposed Class E MOSFET is around 90.7%.

The circuit is then analyzed through experimental works. The crystal oscillator is used to generate the sinusoidal wave. The TC4421/TC4422 is used as a driver. This driver is able to drive large MOSFETSs.



Figure 8: Oscillator Circuit

The Push pull circuit is to maintain a constant voltage difference between the bases of the two transistors. In addition MOSFETs must have high-current buffer/drivers that is capable of driving large MOSFETs by using IC TC4422 as shown in Figure 9 which consists of push pull circuit and high driver MOSFETs circuit.



Figure 9: Push-pull Circuit

The practical circuit for Class E amplifier is shown in Figure 10 with all the values that calculated earlier. Furthermore, the practical circuit for transmitter part is shown in Figure 11 which consists of an oscillator circuit, a push pull circuit and a class E converter.



Figure 10: Schematic Circuit for Class E Amplifier



Figure 11: Transmitter module for CPT



Figure 12: Result of Switching Class E MOSFET Converter

The Figure 13 shows the practical output of the Class E Converter which has been developed in this work. From Figure 13, the generated frequency is 1MHz with 50% duty cycle and the maximum peak voltage is 11.2V. This then validated the design from simulation.



Figure 13: Class E Practical Result of Output Voltage

In theory, the value of V_D must be bigger from V_{CC} by 2 to 3 fold. Based on the practical result, the value of V_D is 20 Volt, and the waveform shows a very minimal overlap. The result has some power loss during switching. Other cause of power loss is also the parasitic resistance in inductors and capacitors or also known Equivalent Series Resistance (ESR). In the section to follow, the focus will be more on construction of hardware of capacitive power transfer to transfer the 5W of power to the load.

3 Modeling And Practical Of CPT Design

In this section, the fundamental of CPT design, including modeling and practical, will be explained.

3.1 CPT operation



Figure 14: Block diagram of a typical CPT system [11]

Based on the Figure 14, a power supply voltage is converted to a high frequency AC voltage which is then supplied to two primary metal plates. When two pickup plates are placed close to them, alternating electric field is formed between the plates. Thus the displacement current can 'flow' through and the power can be transferred to a load without direct electrical contact [12]. To obtain sufficient amount of power as well as provide electrical insulation between the primary and secondary sides, a tuning inductor (either in series or in parallel connection) is usually used to compensate the equivalent coupling capacitance and dielectric materials are coated on the surfaces of the plates. An inverter is then used to produce AC voltage and feed current through the capacitive interface and into the load [13].

3.2 Design of Capacitive Power Transfer

The design steps of our CPT system are shown in Figure 15. By referring to Figure 15, the first step to analyze a CPT system is to understand the capacitive and therefore some basic analysis of capacitive couplings are required. Nevertheless, because the capacitive coupling is treated as a whole part when designing a CPT system, the analysis becomes very difficult particularly when the system order is high. Furthermore, since always being considered in the whole system, there is no convictive conclusion on evaluating the effectiveness of the coupling itself. However, the terms defined were mainly for signal filter design or investigating the effect of mutual capacitances, not for coupled capacitive power transfer [11].

In Modelling of CPT system, the focus is more on from AC source to a load through capacitors formed by parallel plates on transmitting and receiver end. The realizable amount of coupling capacitance is limited by the available area of the device, imposing a challenging design constraint on contactless power delivery. Furthermore, the fundamental issue of CPT is the incapability to be applied in high-power systems as it suffers from limited power delivery and/or low efficiency. This is the real challenge of using CPT based method for wireless power transfer and the reason why IPT received high volume of attention from researchers.



Figure 15: Flow chart design of Capacitive Power transfer

In the design, the values of capacitance between primary and secondary plate come from practical values measurement. The value of capacitance measurement is 23842pF for plate of size 12cm x 12 cm with the thickness of 0.1mm. The CPT circuit is shown in Figure 16. The load of 1 Ω is used in this work. A simulation result of secondary plates of CPT system is shown in Figure 17.



Figure 16: The Circuit of capacitive power transfer

Figure 17 shows the simulation results of maximum voltage and current output at secondary plate of CPT system which are V_{out} =329.705mV and I_{out} =321.908mA respectively.



Figure 17: Result Simulation of Capacitive Power Transfer



Figure 18: Plates primary and secondary of capacitance

Meanwhile for practical CPT system, the output voltage of Class E MOSFET converter is connected to the primary plate as shown in Figure 18. The output power of this developed CPT system is 2.00mW with the combined interface capacitance of 23842 pF, and at an operating frequency of 1 MHz. The voltage transferred to the secondary plate is varied with the distance of the plate; this behavior is shown in Figure 20.

From Figure 19, the output voltage percentage drops from primary plates is 49.06%, and this is shown in equation (16).

$$VoltagePercentageDrop = \frac{10.6 - 5.4}{10.6} \times 100\% = 49.06\%$$
(16)

The capacitive interface has to be measured first before applying to the practical circuit. The validity of the CPT concept has been verified by an experimental CPT system that is delivered 2.00mW power through a combined interface capacitance of 23842 pF, at an operating frequency of 1 MHz. Generally the capacitive structure that is used in this work is given as follows:-.

$$C = \frac{A\varepsilon_0 \varepsilon_r}{d} \tag{17}$$

Where A, d, ϵ_0 (8.85×10-12) and ϵ_r denote the effective coupling area, the coupling distance, the permittivity in vacuum, and the relative permittivity of the dielectric material between the coupling plates, respectively.



Figure 19: Result experiment on Secondary plate capacitance.

In the simulation part, the permittivity in smallgap vacuum is considered in order to calculate capacitance values. However, for practical circuit, air medium is used which is occupied by atmosphere gas. Figure 20 shows results of current and power delivery at the load and we can see that there are gradually dropped when the plates distanced is increased from 0.1 cm to 10 cm. This is because the electrical field will decrease with the increase of distance. The capacitive power transfer must use high frequency to be injected in primary capacitive plates. Before transferring the energy, the performance of source energy must be clarified to avoid power loss.



Figure 20: Analysis of Output Current and Power due to distance plate.

4 Conclusion and Recommendation

The wireless power transfer technology has been successful analyzed and designed by using a capacitive based method. The finding shows that small air gap capacitors enable high efficiency contactless power transfer. In Class E MOSFETs Inverter, the performance has been analyzed in its switching capabilities and efficiency of the system. For modeling and practical CPT design, the design challenges of a contactless power delivery has been dealt even though with it's very small delivery power at secondary plate it is successful for almost nearly 2.00 mW output power which is suitable for small application.

It is recommended that CPT is adapted for small size applications such as biomedical plant, medical applications or charging of space-confined system such as robots or mobile device and etc. CPT is based on pairing electric field between two capacitive plates and it does not require expensive ferrite core and protection due to the electric field between plates.

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