The DC Behavioural Electrothermal Model of Silicon Carbide Power MOSFETs under SPICE

A. LAKRIM (Member Student IEEE), D. TAHRI
Signals, Systems and Components Laboratory (SSCL),
EMC and Power Electronic Systems Team
Faculty of Sciences and Technologies
BP.2202 Fez, Morocco
Morocco
Abderrazak.lakrim@usmba.ac.ma

Abstract: - This paper presents a new behavioural electrothermal model of power Silicon Carbide (SiC) MOSFET under SPICE. This model is based on the MOS model level 1of SPICE, in which phenomena such as Drain Leakage Current IDSS, On-State Resistance R_{DSon}, gate Threshold voltage V_{GSth}, the transconductance (gfs), I-V Characteristics Body diode, temperature-dependent and self-heating are included and represented using behavioural blocks ABM (Analog Behavioural Models) of Spice library. This ultimately makes this model flexible and easily can be integrated into the various Spice -based simulation softwares.
The internal junction temperature of the component is calculated on the basis of the thermal model through the electric power dissipated inside and its thermal impedance in the form of the localized Foster canonical network. The model parameters are extracted from manufacturers' data (curves data sheets) using polynomial interpolation with the method of simulated annealing (SA) and weighted least squares (WLS). This model takes into account the various important phenomena within transistor. The effectiveness of the presented model has been verified by Spice simulation results and as well as by data measurement for SiC MOS transistor C2M0025120D CREE (1200V, 90A).

Key-Words: - SiC power MOSFET, DC Electro-thermal Model, ABM Spice library, SPICE Behavioural Modeling, C2M0025120D CREE

1 Introduction

The silicon carbide (SiC) MOSFET has become a strong competitor for the new wide Bandgap components. It is predicted to replace silicon (Si) in high voltage semiconductor devices and in high frequency applications due to its high breakdown voltage [1], its lower specific on-resistance (Ron) [2], as also its ability to operate in high temperature [3, 4].
The simulation at the circuit design is very important for the optimization of power electronic circuits within the EMC aspects [5], and leakage constraints supported by semiconductors [6, 7]. In order to get credible results based on simulations, we need to have accurate models, with acceptable complexity and the ability to be adapted to the used simulator [8].
To reduce the complexity of the model, only the most important physical phenomena affecting the characteristics and parameters of the component must be taken into account in the process of constituting the model. Among these phenomena, self-heating affecting properties of the power MOS transistor which yields up a significant increase in the internal junction temperature contribute into reducing its performance [6, 9].
SPICE simulator [10] (Simulation Program with Integrated Circuit Emphasis) is a well and widely used tool for analyzing electronic circuits. Unfortunately, the MOSFET models integrated in SPICE (different levels) [11, 12] are formulated for isothermal low power MOS, while self-heating is not included in these models. Besides, these models are characterized by excessive complexity and by a large number of physical parameters which we cannot wholly control and which virtually require obtaining a proper identification for each component [13]. Recently a large number of MOS transistor isothermal models have been introduced in both research [14, 15] and manufacturer’s works [16, 17]. Yet, despite the complexity of some models, many important physical phenomena are missing which usually results in faulty imprecision [18]. Currently, the SiC MOSFETs are still under improvement and marketed by a very limited number of companies such as Cree Inc., ROHM Semiconductor, General

Electric, and ST Microelectronics. This means that their models are still very restricted in use [6].
As an attempt to improve these models, we propose in this paper a flexible behavioural electrothermal model based on the Spice model MOS level 1 [19], and voltage controlled voltage source and current source (VCVS: Ei and VCCS: Gi) of the Spice ABM library [20]. For in addition to its flexibility it can be easily integrated in different simulation softwares adopting Spice. Many important physical phenomena relating to temperature are included in a behavioural form in this model. The internal junction temperature of the device is calculated on the basis of the thermal model through the electric power dissipated inside the component and its thermal impedance in the form of the canonical localized Foster network [21].
The coefficients and parameters of control equations for each voltage or current ABM source are extracted from manufacturers' data (curves data sheets) using polynomial interpolation with simulated annealing (SA) and weighted least squares (WLS) methods [22]. To further prove the performance of this model, which our main contribution, an example of these transistors in silicon carbide (CREE C2M0025120D (1200V, 90A)) [23] will also be given.

2 ABM Macromodeling Technique

The physical investigation of a power device gives a set of integral-differential equations that describe device's static and dynamic behaviour. The challenge in modelling ABM SPICE lies in how to present these equations and thus reduce problems of convergence. Figure (Fig.1) shows a diagram of the underlying principle of this modelling. The starting point is the static model resulting in many voltage and current controlled sources.

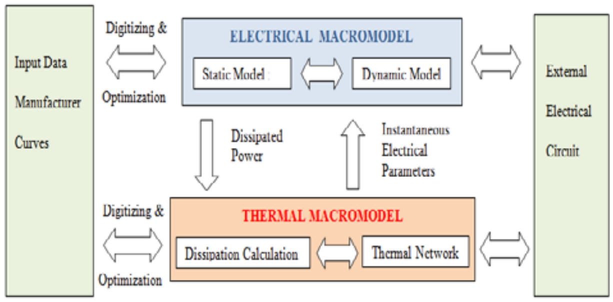

Figure 1 Diagram of an ABM model of Power SiC MOS

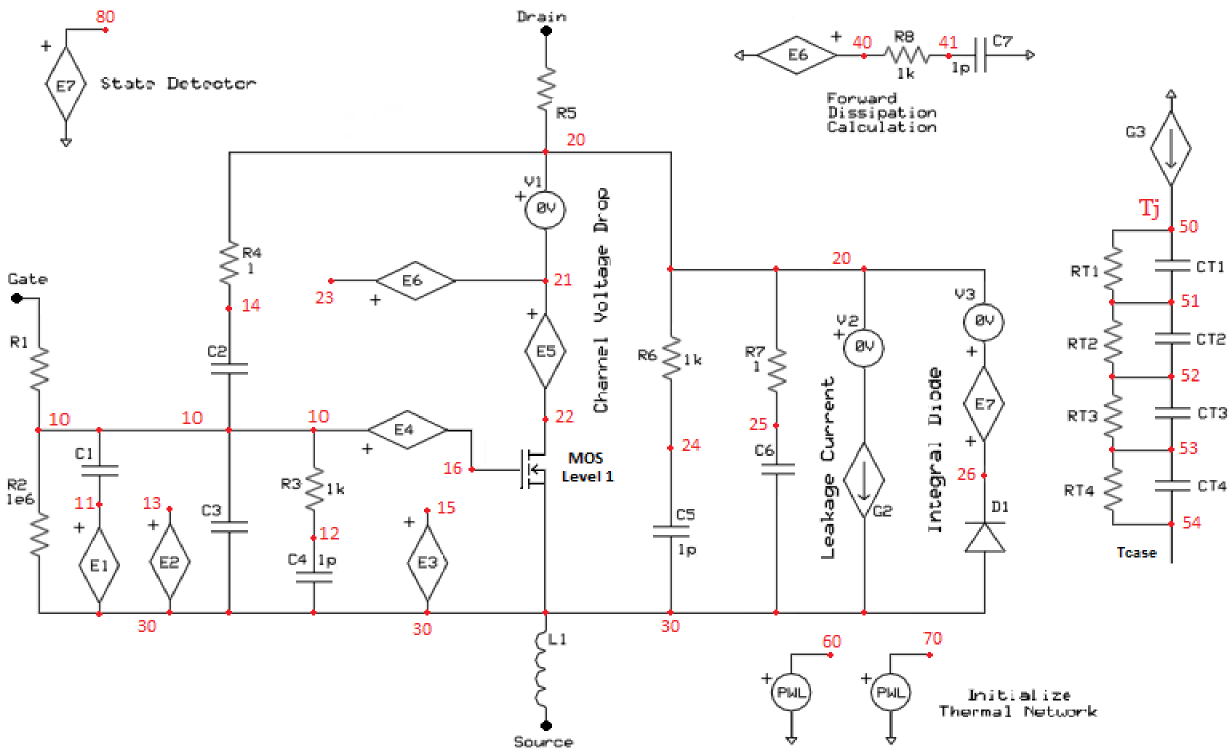

Figure 2. The Behavioural Electrothermal Model of SiC MOS transistor

3 Spice SiC Behavioral Electrothermal MOS Model

The behavioural electrothermal model of SiC MOS transistor is shown in Figure (Fig.2). The static characteristics modelized depending on the junction temperature of the SiC MOS are:

- Transfer Characteristics
- Output Characteristics
- On-State Resistance R_{DSOn}
- Gate Threshold Voltage V_{GSTh}
- Body Diode I-V Characteristics
- Drain Leakage Current I_{DSS}

3.1 Transfer Characteristics & On-State Resistance R_{DSon}

The level 1 model of the MOSFET (MOSLev1) is used to describe the gain of the transistor at ambient temperature (T =25°C) for a full range of current starting from the sub-threshold region. Vt0 and Kp MOSLev1 parameters are extracted from the interpolation of the datasheet transfer curve I_D (V_{GS}) (Fig.3) in the form equation 1:

$$I_D = Kp.\left(V_{GS} - V_{GS(th)} \right)^2 \qquad (1)$$

Vt0= zero-bias threshold voltage

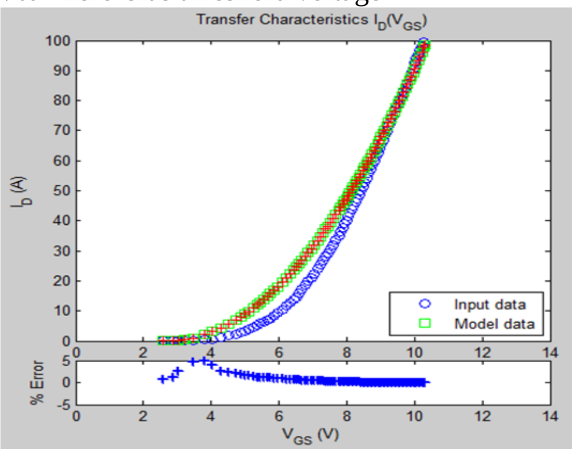

Figure 2. Input Data and Model Input of Admittance Characteristics $I_D(V_{GS})$, and the Percentage Absolute Error (Down)

An ABM source (VCVS) E3 is added to adjust the gain to temperature variations. It also contributes to the change in R_{DSon}. For simplicity, the transfer curve $I_D(V_{GS})$ is represented in a linear form dependent on the internal junction temperature instead of on a quadratic representation. Equation E3 is:

$$E_3 = \left(Ga_0 + Ga_1.V(T_j) + Ga_2.V(T_j)^2 \right) + \left(Gb_0 + Gb_1.V(T_j) + Gb_2.V(T_j)^2 \right) \times V_{C4} \qquad (2)$$

Ga_0, Ga_1, Ga_2, Gb_0, Gb_1 and Gb_2 are the coefficients of the polynomial interpolation of the manufacturer data curves (Fig.4).

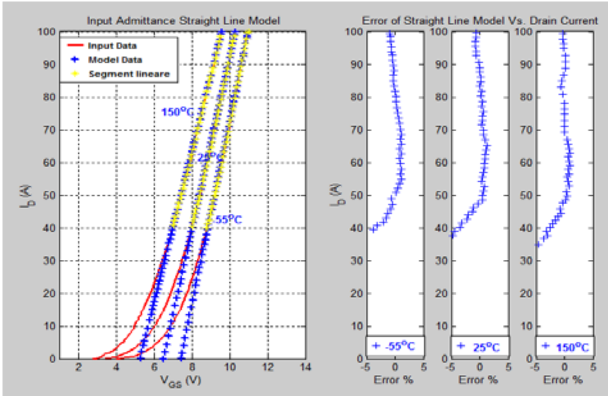

Figure 3. Input Data and Straight Line Model of Input Admittance (left), and Percentage Absolute Error (Right)

The modelization of the output characteristics requires the use of more voltages VGS. However; in order to reduce its complexity we used only three high voltages; i.e (V_{GS} = 16V, 18V and 20V) which are characterized by a broad common linear part representing the R_{DSon} resistance (Fig.5) refer to3.

$$R_{DSon} = \frac{\Delta V_{DS}}{\Delta I_D} \qquad (3)$$

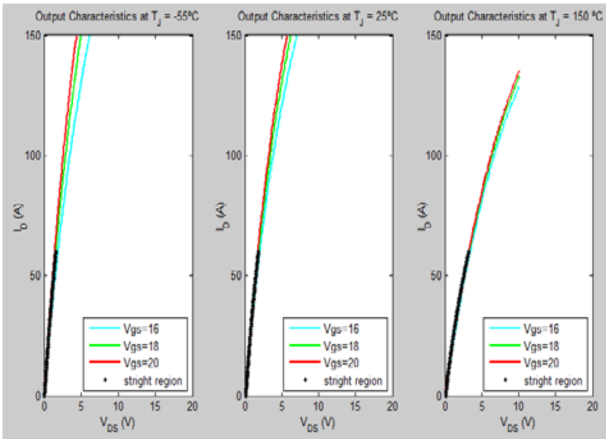

Figure 4. Output characteristics data and straight line model vs. drain source voltage for T=-55°C, T =25°C and T =150°C

The source E6 represents the ohmic region and adjusts the model in its linear region, it depends on the internal temperature of the junction and takes the form of equation 4.

$$E_6 = \left(Ra_0 + Ra_1.V(T_j) \right) + \left(Rb_0 + Rb_1.V(T_j) \right) \times I(V_1) + \left(Rc_0 + Rc_1.V(T_j) \right) \times I(V_1)^2 \qquad (4)$$

Ra_0, Ra_1, Rb_0, Rb_1, Rc_0 and Rc_1 are the coefficients of the polynomial interpolation using the intersection line of the three curves of VGS = 16V, 18V, 20V (Fig.5). The output of E4 is a ramp limited by the maximum value of the ohmic region (20V, 100A).

The source E5 is the error amplifier used to fit the model in its active region, causing the drain-source voltage drop and limiting I_D to a value determined by the input admittance (E3) as shown by the equation 5 follows:

$$E_5 = Gain\left(I_D - I_{adm}\right) \qquad (5)$$

The output of E5 is limited by the ramp maximum value of the voltage V_{DS} of active region (1400V).

3.2 Gate Threshold Voltage V_{GSTh}

As the manufacturer datasheet's shows (Fig.6), the threshold voltage Vth varies according to temperature in a linear form (Refer to 6). This threshold voltage is represented by the source E4.

$$V_{th} = a.\ V(T_j)\ +\ b \qquad (6)$$

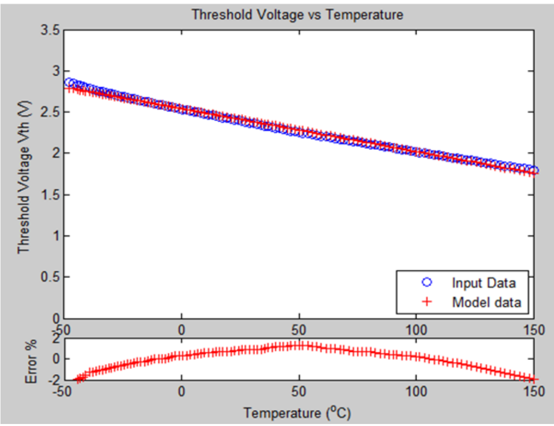

Figure 5. Input Data and straight line model of Threshold Voltage vs. Temperature, And Percent Absolute Error (Down).

3.3 Body Diode I-V Characteristics

The curve's data of the body diode characteristics (Fig.7) is provided by I_{SD} (V_{SD}) for each temperature (T = -55 T = 25 and T = 150 °C) and for the negative V_{GS} (V_{GS} = -5, - 2 and 0V). The model of the body diode comprises a reference diode in series with a controlled voltage source [24]. For each temperature the I_{SD} (V_{SD}) curves of V_{GS} values have a similar form, and are almost the same. And so, for simplicity purposes, we selected the curve of V_{GS} = -2V. The control equation is:

$$E_7 = \log\left(\frac{I_D}{10^{-14}}+1\right)\times\left(Da_0 + Da_1.V_{Tj} + Da_2.V_{Tj}^2\right)\times 0.0257$$
$$+\ \left(Db_0 + Db_1.V_{Tj} + Db_2.V_{Tj}^2\right)\times I_D \qquad (7)$$

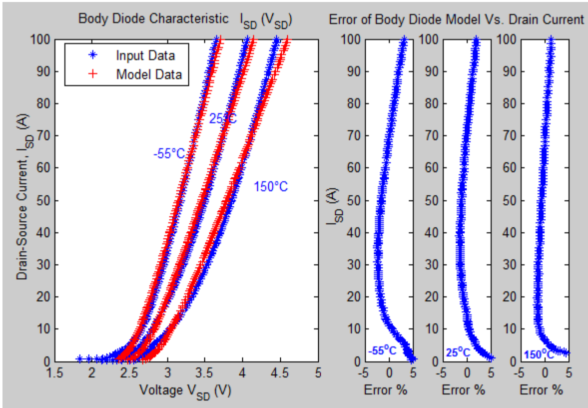

Figure 6. left: Input Data and Model Data of 3rd Quadrant Characteristic I_{SD}(V_{SD}). Right I_{SD} Percentage Absolute Error

In this figure (Fig.7) we notice an almost perfect correspondence between the curves of manufacturer's (input) data and the model data, and the absolute error does not exceed 5%. Da_0, Da_1, Da_2, Db_0, Db_1 and Db_2 are the coefficients of the interpolating polynomial depending on the junction temperature.

3.4 Drain Leakage Current I_{DSS}

The off-state current or the leakage current IDSS of the MOSFETs is evaluated according to the variation of the drain-source voltage V_{DS} and shorting its gate-source terminals (V_{GS} = 0) for temperatures under study. The measurements show that I_{DSS} increase slightly and proportionately with the increase in temperature [6].

The manufacturer datasheet provides maximum value for I_{DSS} under a certain condition (for this example V_{DS} = 1200V, V_{GS} = 0V). To simplify the model, we represent I_{DSS} by a constant current source. In the case where the manufacturer provides the evolution curve of I_{DSS} (V_{DS}, T°) we represent I_{DSS} by a voltage controlled current derived from this curve equation [24-25].

3.5 Thermal Model

The thermal model is designed independently of the electrical network model in the form of (R-C) Foster which is made up of 4 cells. The values of Ci and Ri are used to adapt the simulated thermal impedance curve (Fig.8) to the measured data. All heat losses of MOSFET are modelized by the current source G3 which represents the instantaneous power dissipation in the thermal model.

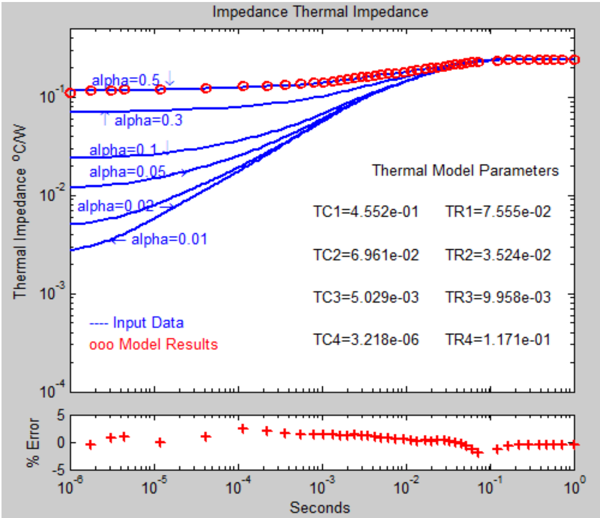

Figure 7. Measured (Input data) and simulated thermal impedance characteristics. And Percentage Absolute Error (Down)

The curve clearly shows that the absolute error between the model and the manufacturer's data does not exceed 3%.

4. Validation Of The Model By Spice Simulation

To prove the validity and significance of the model presented, we have compared the measurements results of the data-book and SPICE simulations of SiC power MOS transistor static characteristics. We applied this behavioural electrothermal model to SiC MOS C2M0025120D CREE (1200V, 90A) [23].

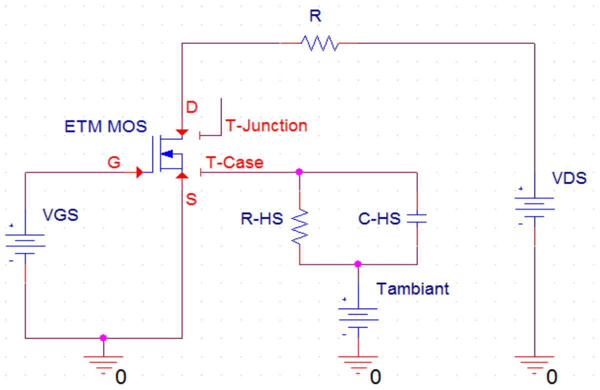

Figure 8. Spice simulation circuit

4.1 Simulation Results

The Spice simulation of this model has yielded up very satisfactory results. Indeed, the curves of transfer (Fig.9) and output (Fig.10) characteristics confirm our conclusion. The solid lines represent the results obtained with Spice simulation of the model, while the dotted-lines correspond to the measurements supplied by the manufacturer.

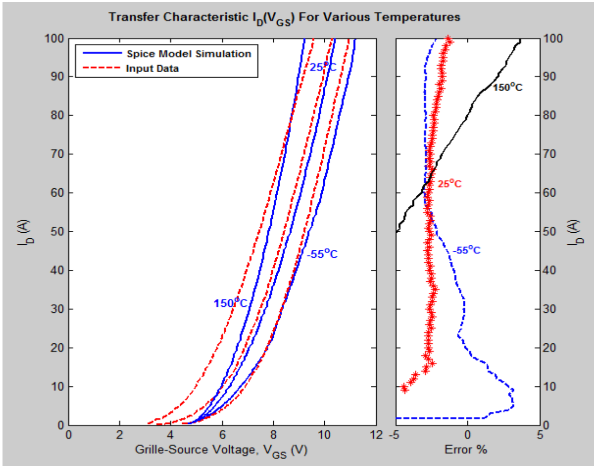

Figure 9. Left: Input Data and Spice Model Simulation of ID(VGS), right Percentage Absolute Error

4.2 Transfer Characteristics

We note that:

- The threshold voltage Vt0 model is constant for the three temperatures (blue line) because it was taken at a constant value in model of MOS Level 1.
- The curve of temperature 150°C showed unsatisfactory results due to the voltage Vt0 MOS Lev1 which was taken at a constant value and linear model of transfer characteristics I_D (V_{GS}).
- Despite these differences the relative error does not exceed 5% of the features.

4.3 Output Characteristics

The output characteristics are related to the non-saturation area (linear) for three voltages V_{GS} (16V, 18V, and 20V), at three temperatures -55 °C (Fig.11-a), 25 °C (Fig.11-b), and 150 °C (Fig.11-c).

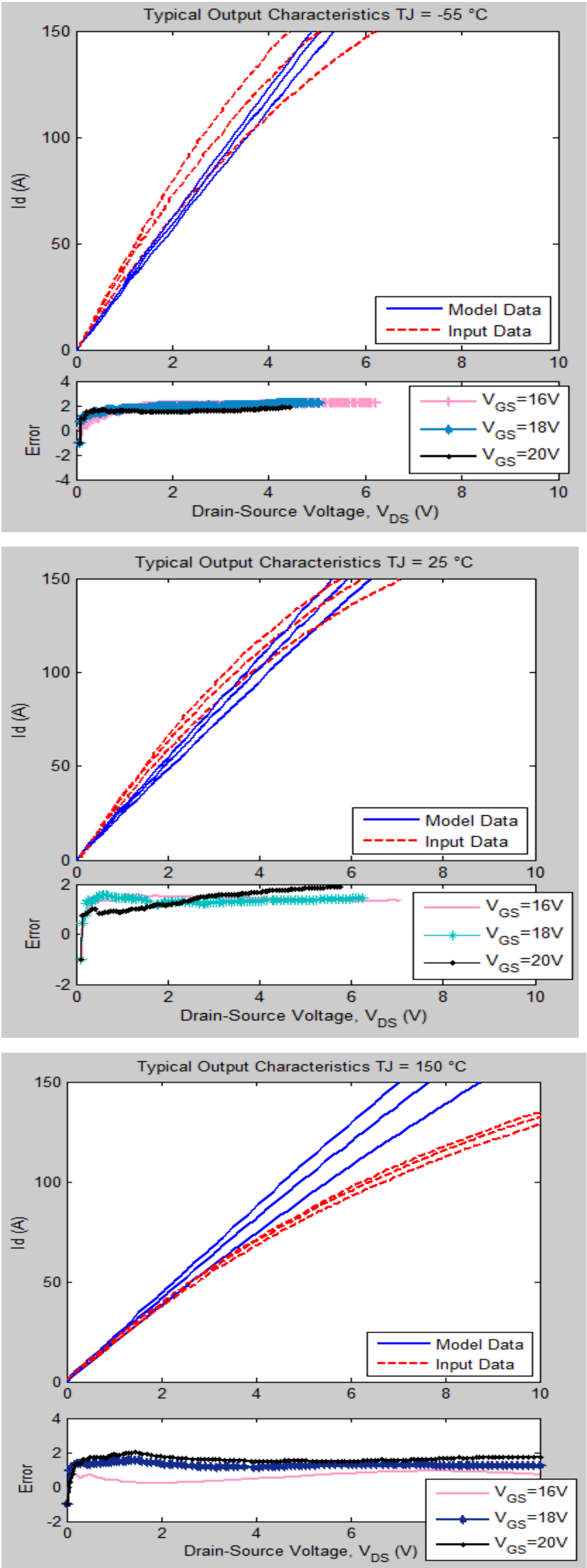

Figure 10. Top: data output characteristics and Spice Simulation model vs. drain source voltage for T=-55°C, T=25°C and T=150°C. Down Percentage Absolute Error

The analysis of these curves (Fig.11) shows that:

- The remarkable differences between the curves of measurements and simulations are due to the nonlinearity of the resistance model R_{DSon}
- The model shows good agreement for the average temperatures and remains viable despite our simplification (linearization of the curve).

5 Conclusion

In this article we dealt with the problem of modelling the MOSFET power. We proposed a behavioural model based on the electrothermal MOS model Level 1 of the SiC MOS transistor, and implemented it using a well known simulator (SPICE).

The effectiveness of the model was verified by a comparison between the measured static characteristics (manufacturer data) and those simulated with OrCAD Spice SiC MOS power transistor for C2M0025120D CREE (1200V, 90A). A good agreement between the simulation results and experimental results provided by datasheets is observed. An exception is noticed at temperature of 150 °C. The model has many advantages including simplicity and flexibility in its implementation for various modern simulators adopting Spice.

Finally this model is still being improved in terms of modelling quasi-saturation effects and R_{DSon} resistance for high temperatures.

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Authors

Abderrazak LAKRIM (M'2013) was born in Taza, Morocco, on December 28, 1985. He received the Bachelor and Master degrees in Industrial Engineering from Faculty of Sciences and Technologies – University Mohamed Ben Abdellah, Fez, Morocco in 2008 and 2010, respectively.

He is currently working toward the Ph.D. degree in Engineer Sciences and techniques at the Faculty of Sciences and Technologies of Fez (FST-USMBA).

Since 2011 he is Electricity Trainer Engineer at OFPPT Morocco

His research interests include: Spice Modeling, Power SiC Devices, Electromagnetic Compatibility, Switching cells, power circuits simulation,

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