A New Trans-admittance Mode Biquad Filter using MO-VDTA

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Abstract: - In this paper, a new trans-admittance-mode biquad filter configuration based on two multi output voltage differencing transconductance amplifiers (MO-VDTAs) as newly active elements is proposed which also consists of two grounded MOS resistors and two capacitors with one of the capacitor is being permanently grounded. The proposed configuration is competent of realizing trans-admittance-mode low pass (LP), band pass (BP), high pass (HP), band reject (BR) and all pass (AP) filtering responses. Moreover, the proposed circuit offers several excellent features such as electronic tunability of pole frequency and quality factor, low active and passive sensitivity and low power consumption. To justify the theoretical analysis, the proposed circuit is simulated using PSPICE in 0.35μm CMOS technology from TSMC.

Key-Words: - VDTA, TAM, Biquad, Filter, Analog signal processing, Tunable.

1 Introduction

In the last few decades, numerous number of current-mode active elements have been introduced and gained significant attention to implement analog biquad filters used for analog signal processing applications due to having their high performance attributes such as wider signal bandwidth, low power consumption, larger dynamic range, better linearity, simple circuitry and requirement of lesser on chip area [1-26] with respect to voltage-mode counterpart. Biquad filters with voltage input(s) and current output(s) are termed as trans-admittance-mode (TAM) filters and suitable for the applications where conversion of voltage signal into current signal is required. Such applications find usages in receiver baseband block of modern radio system, D/A converters and optical receivers etc [15-16]. Literature survey has shown that comparatively limited work has been proposed in the domain of TAM filter. In the available literature most of the circuits uses single input multi output (SIMO) configuration to realize TAM filter [15-22] while remaining circuit uses multi input single output (MISO)[23] configuration. Details comparative study among them is discussed in Table 1 which reveals that the various proposed TAM filter circuits uses (CII) [16], four terminal floating nuller (FTFN) [17], operational transconductance amplifier (OTAs) [19-20], voltage differencing trans-conductance amplifier (VDTA) [22] current differencing trans-conductance amplifier (CDTA) [23] etc., as current-mode active elements in the implementation and perform nicely with respect to various TAM filtering functions realization but unfortunately, they still suffer from one or more following drawbacks.

(i) Use of more number of active and /or passive elements [15-21].

(ii) Use of excessive number of floating passive components [16-18, 23]

(iii) Voltage input signal (s) is not applied at high impedance terminal [15-17, 23].

(iv) Incompetent of realizing all five standard filtering functions [16-20, 22].

(v) Lack of electronic tunability of filter parameters [16-18, 21].

(vi) Use of more than minimum number of capacitors (two) required to realize various filtering functions [15].

Moreover, it is also noted from Table 1 that only three input single output TAM circuit based on two CDTAs as active element can realize all the five standard filtering function [23]. However, it uses four passive elements (two resistors and two capacitors) among them three are being floating (not grounded), for realizing all five filtering functions. In addition, none of the voltage input signal is

Table 1. Comparison of different TAM filters with proposed TAM filter circuit

References → **Features ↓**	**[15]**	**[16]**	**[17]**	**[18]**	**[19]**	**[20]**	**[21]**	**[22]**	**[23]**	**Proposed**
No. & type of active element	2 CCCCTA	3 CCII	3 PFTFN	5 DCC-DVCC	4 OTA	4 OTA	3 CCCII	2 VDTA	2 CDTA	2 VDTA
No. & type of passive element	3 C	3R, 2C	3R, 2C	2C , 1R	2C	2C	2C	2C	2R, 2C	2R, 2C
No. of Floating passive element	NIL	4 (2R+2C)	4 (2R+2C)	3(2R+1C)	NIL	NIL	NIL	NIL	3(2R+1C)	1 (1C)
SIMO/MISO	SIMO	SIMO	SIMO	SIMO	SIMO	SIMO	SIMO	SIMO	MISO	MISO
Voltage I/P applied at high impedance terminal (s)	NO	NO	NO	YES	YES	YES	YES	YES	NO	YES
Realization type	LP,BP,HP, AP, BR	LP,BP,HP	LP,BP,HP	LP,BP,HP	LP,BP,HP	LP,BP,HP	LP,BP,HP, AP, BR	LP,BP,HP	LP,BP,HP, AP,BR	LP,BP,HP, AP,BR
Electronic tunability	YES	NO	NO	NO	YES	YES	NO	YES	YES	YES

applied at high impedance terminals. Keeping above discussion in the mind, we have proposed a new three input single output trans-admittance mode filter which uses two MO-VDTAs, two grounded MOS resistors , two capacitors and can realize all five filtering response (LP, HP, BP,BR,AP) in trans-admittance-mode. The circuit enjoys an electronic adjustment property of pole frequency (ω_o) as well as bandwidth independent of Q_0 and possesses low active and passive sensitivity performance. The performance of proposed circuit is verified by PSPICE simulations.

2 VDTA Description

VDTA is one of the new active element which is first introduced by A. Yesil, F. Kacar and H. Kuntman in 2011[24] and offers the advantage of its electronic tuning ability through two transconductance parameters. Moreover, this device can be operated in both current as well as voltage-modes, providing flexibility to the circuit designers [24-26]. MO-VDTA is modified version of conventional VDTA which can be obtained from VDTA by inserting additional transconductance outputs. It's symbolic diagram is shown in Fig.1 where P, N are two input terminals and Z, X+, X- are the output terminals. Each input and output terminals in VDTA have high impedance. Voltage difference between P and N ($V_P - V_N$) is transferred to a current at terminals Z (I_Z) by transconductance parameters (g_{mF}) of VDTA. Further voltage across Z terminal is also transferred to a current at terminals X^+ and X^- (I_X^+ and I_X^-) by other transconductance parameters (g_{mS}) of VDTA. The voltage current relationship between various input and output terminals of MO-VDTA can be described in the following matrix equation.

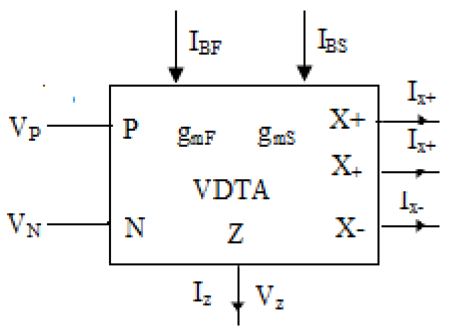


Fig.1: Block diagram of MO-VDTA

$$\begin{bmatrix} I_z \\ I_{X\pm} \end{bmatrix} = \begin{bmatrix} g_{mF} & -g_{mF} & 0 \\ 0 & 0 & \pm g_{mS} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \tag{1}$$

Both transconductance parameters g_{mF} and g_{mS} of VDTA are controlled by biasing current I_{BF} and I_{BS} of VDTA, respectively. The VDTA shown in fig.1 is realized using CMOS implementation and shown in Fig.2. For CMOS implementation of VDTA realized as shown in Fig.2, g_{mF} and g_{mS} can be mathematically related by following equations.

$$g_{mF} = \sqrt{I_{BF}\mu_n C_{ox}(\frac{W}{L})_{M1,M2}} \tag{2}$$

$$g_{mS} = \sqrt{I_{BS}\mu_n C_{ox}(\frac{W}{L})_{M5,M6}} \tag{3}$$

Where μ_n is the effective carrier mobility of NMOS transistor and C_{ox} is the gate-oxide capacitance per unit area. $(W/L)_{M1,\,M2}$ and $(W/L)_{M5,\,M6}$ are the aspect ratio of M1, M2 and M5, M6 NMOS transistor pairs, respectively.

3 Proposed TAM Filter and Its Analysis

The proposed TAM filter configuration is shown in Fig.3 which employs two MO-VDTAs , two grounded resistors (R_1 and R_2) and two capacitances (C_1 and C_2) with one of the capacitor (C_1) is being permanently grounded. In the proposed configuration as shown in Fig.3, each grounded resistor (R_i, where i=1, 2) has been realized by using parallel connection of two NMOS transistors (MR_1 and MR_2). Thus, the equivalent resistance can be calculated by

$$R_i = \frac{1}{2\mu_n C_{ox}\frac{W_{MRi}}{L_{MRi}}(V_{ci} - V_T)} \tag{4}$$

Where V_T is the threshold voltage of the NMOS transistor. V_{ci} is the biased voltage and $\frac{W_{MRi}}{L_{MRi}}$ stands for aspect ratio of NMOS transistor used in the resistance realization. Routine analysis of the proposed circuit of Fig.3, yields the expression of current output (I_{out}) on applying voltage inputs (V_{in1}, V_{in2}, V_{in3}) can be derived as

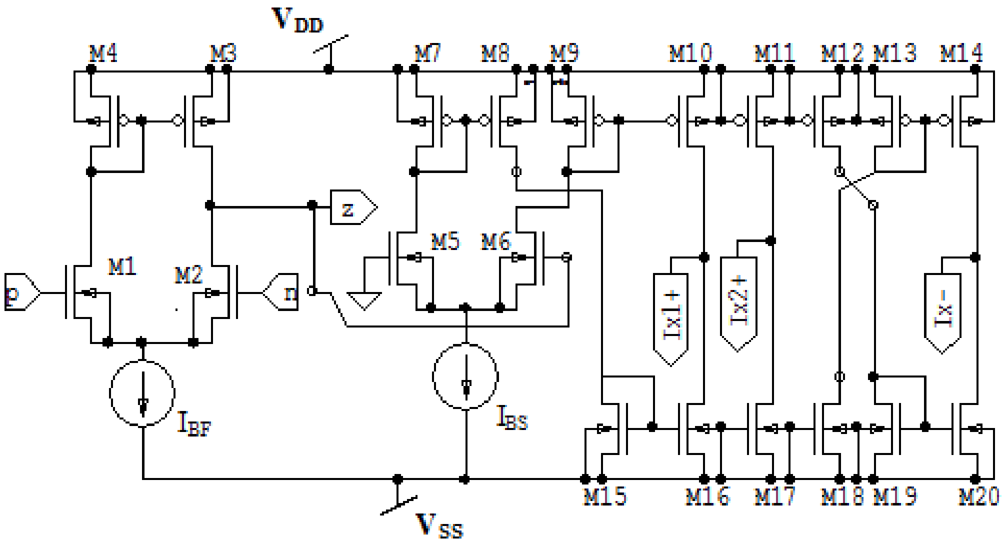


Fig.2: Implementation of MO-VDTA using CMOS transistors

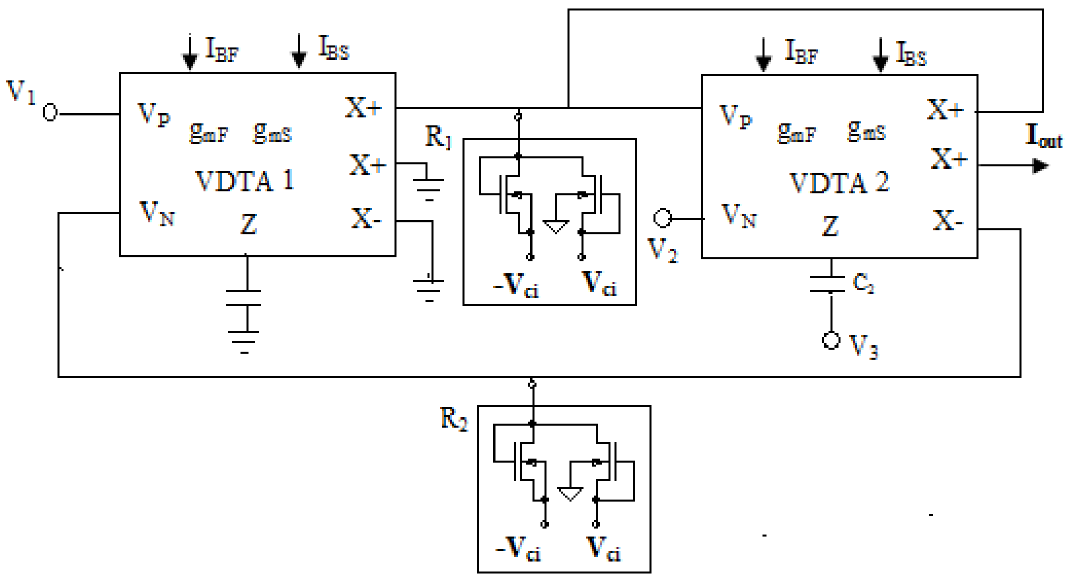


Fig.3: Proposed three input single output TAM Biquad filter

$$I_{out} = g_{mS2} \frac{\frac{g_{mF1} g_{mF2} g_{mS1} R_1}{C_1 C_2} V_1 - \frac{s g_{mF2}}{C_2} V_2 + s^2 V_3}{s^2 + s \frac{g_{mF2} g_{mS2} R_1}{C_2} + \frac{g_{mF1} g_{mS1} g_{mF2} g_{mS2} R_1 R_2}{C_1 C_2}} \tag{5}$$

Where g_{mFi} and g_{mSi} (i=1,2) denotes the first and second transconductance gains of i^{th} VDTA, respectively. It is seen from the above equation that the proposed filter circuit used as three input single output (TISO) configuration and realizes all five standard filter functions in TAM at current output (I_{out}) with following appropriate selection of input voltage signal.

(i) If V_1=V_2=0 and V_3=V_{in} , a biquadratic TAM HP filter can be realized.

(ii) If V_1=V_3=0 and V_2=V_{in}, a biquadratic TAM BP filter can be realized.

(iii) If $V_2=V_3=0$ and $V_1=V_{in}$, a biquadratic TAM LP filter can be realized.

(iv) If $V_2=0$, $V_1=V_3=V_{in}$, and $g_{mS2}R_2=1$, a biquadratic TAM BR filter can be realized.

(v) If $V_1=V_2=V_3=V_{in}$, $g_{mS2}R_1=1$ and $g_{mS2}R_2=1$, a biquadratic TAM AP filter can be realized.

The pole frequency (ω_0), the quality factor (Q_0) and bandwidth (BW) ω_0/Q_0 of each filtering response can be expressed as:

$$\omega_0=\sqrt{\frac{g_{mF1}g_{mF2}g_{mS1}g_{mS2}R_1R_2}{C_1C_2}} \quad (6)$$

$$Q_0=\sqrt{\frac{g_{mF1}g_{mS1}R_2C_2}{g_{mF2}g_{mS2}R_1C_1}} \quad (7)$$

$$BW=\frac{g_{mF2}g_{mS2}R_1}{C_2} \quad (8)$$

If we select $g_{mF1} = g_{mF2} = g_{mF}$ and $g_{mS1} = g_{mS2} = g_{mS}$ in the design procedure, then equations (6)-(8) can be further simplified as

$$\omega_0=g_{mF}g_{mS}\sqrt{\frac{R_1R_2}{C_1C_2}} \quad (9)$$

$$Q_0=\sqrt{\frac{R_2C_2}{R_1C_1}} \quad (10)$$

$$BW=\frac{g_{mF}g_{mS}R_1}{C_2} \quad (11)$$

It is clear from equations (9)-(11) that both filter parameters ω_0 and BW can be electronically tuned independent of Q_0 by varying either g_{mF} (I_{BF}) or g_{mS} (I_{BS}) or both. Furthermore, Q_0 can also be electronically tuned independent of ω_0 by maintaining the product of R_1 and R_2 as constant that can be done by adjusting the bias voltage of MOS transistors used in resistors at appropriate levels.

4 Non Ideal Effects and Sensitivity Analysis:

Taking the effects of non-ideal characteristics of the MO-VDTA into consideration, the current and voltage relations between various ports of VDTA can be rewritten as:

$$\begin{bmatrix} I_z \\ I_{X\pm} \end{bmatrix}=\begin{bmatrix} \beta_F g_{mF} & -\beta_F g_{mF} & 0 \\ 0 & 0 & \pm\beta_S g_{mS} \end{bmatrix}\begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad (12)$$

Where β_{Fi} and β_{Si} are the tracking error for the first and second stages of the i^{th} MO-VDTA (i=1,2). With consideration of above non ideal errors we further reanalyze the proposed circuit of Fig.3. The following non-ideal filter transfer function and its filter parameters can be obtained as.

$$I_{out}=\beta_{S2}g_{mS2}\frac{\frac{\beta_{F1}\beta_{F2}\beta_{S1}g_{mF1}g_{mF2}g_{mS1}R_1}{C_1C_2}V_1-\frac{s\beta_{F2}g_{mF2}}{C_2}V_2+s^2V_3}{s^2+s\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}R_1}{C_2}+\frac{\beta_{F1}\beta_{S1}\beta_{F2}\beta_{S2}g_{mF1}g_{mS1}g_{mF2}g_{mS2}R_1R_2}{C_1C_2}} \quad (13)$$

$$\omega_0=\sqrt{\frac{\beta_{F1}\beta_{S1}\beta_{F2}\beta_{S2}g_{mF1}g_{mS1}g_{mF2}g_{mS2}R_1R_2}{C_1C_2}} \quad (14)$$

$$Q_0=\sqrt{\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}R_2C_2}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}R_1C_1}} \quad (15)$$

$$BW=\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}R_1}{C_2} \quad (16)$$

It is evident from equation (13)-(16) that the filter parameters such as pass band gain, ω_0, Q_0 and BW of various TAM filtering responses of the proposed circuit may be slightly changed due to effect of tracking errors of VDTAs but these deviation can be minimized by adjusting the electronic controllable trans-conductance parameters.

The active and passive sensitivities of ω_0 and Q_0 for the proposed filter in Fig.3 are derived and given in equations (17)-(20).

$$S^{\omega_0}_{\beta_{F1},\beta_{S1},\beta_{F2},\beta_{S2}}=\frac{1}{2}, S^{\omega_0}_{R_1,R_2}=\frac{1}{2}, \quad S^{\omega_0}_{g_{mF1},g_{mS1},g_{mF2},g_{mS2}}=\frac{1}{2} \quad (17)$$

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2} \quad (18)$$

$$S_{\beta_{F1},\beta_{S1},g_{mF1},g_{mS1}}^{Q_0} = \frac{1}{2}, S_{R_2,C_2}^{Q_0} = \frac{1}{2} \quad (19)$$

$$S_{\beta_{F1},\beta_{S2},g_{mF1},g_{mS2}}^{Q_0} = -\frac{1}{2}, S_{R_1,C_1}^{Q_0} = -\frac{1}{2} \quad (20)$$

Consequently, all of the component sensitivities of ω_0 and Q_0 are within 0.5 in magnitude which is low.

5 Simulation Results

In order to verify the performance of the proposed filter as per discussion in the section 3, the circuit of Fig.3 has been simulated using CMOS implementation of VDTA (shown in Fig. 2), by using standard CMOS model parameters of 0.35μm technology from TSMC as given in Table 2. The supply voltages were selected as $V_{DD} = -V_{SS} = 1.0V$ and $+V_{ci} = -V_{ci} = 1.07V$. The passive and active components values were taken as $R_1 = R_2 = 2.79K\Omega$, $C_1 = C_2 = 25pF$ and $g_{mF1} = g_{mF2} = g_{mS1} = g_{mS2} \approx 376.67\mu A/V$ ($I_{BF1} = I_{BF2} = I_{BS1} = I_{BS2} = 40\ \mu A$), which results in total power consumption of about .992mW of the proposed circuit. The transistors aspect ratio of the VDTA as described in Table 3 was used in this simulation. Fig. 4 shows the simulated trans-admittance-mode gain and phase responses of LP, HP, BP, BR and AP for the proposed trans-admittance -mode biquad filter as shown in Fig.3. From the simulation results, the pole frequency was obtained as 2.51 MHz which is nearly same as the calculated value of 2.52 MHz. In Fig. 5, various BP and LP filtering responses for proving the feature of electronic tunability of pole frequency independent of Q_0 are shown which were obtained by simultaneous variation of all transconductance parameters of VDTAs as $g_{mF1} = g_{mF2} = g_{mS1} = g_{mS2} =$ 266.33uA/V, 376.67uA/V, 532.67uA/V ($I_{BF1} = I_{BF2} = I_{BS1} = I_{BS2} =$ 20μA, 40μA, 80μA) for a constant Q_0=1. Three pole frequencies variation were obtained as 1.25MHz, 2.51MHz and 5.02 MHz, respectively.

Next, the transient behaviour of LP and BP outputs for the proposed filter was also investigated by applying an appropriate sinusoidal input voltage signal having peak to peak amplitude of 80mV at frequency of 200 KHz in case of LP and 100 mV at frequency of 2.51 MHz in case of BP. The simulation results showing the large signal transient responses of LP and BP outputs are shown in Fig.6 where a load of 2.79KΩ resistor was used to obtain the output across LP and BP responses. Furthermore, the total harmonic distortion results for LP and BP responses are shown in Fig.7 which clearly shows that the THD values of the proposed filter for LP output was found in the range of .68 to 1.94% for sinusoidal input voltage signal of constant amplitude of 40mV and variable frequency between 500KHz to 5MHz whereas the THD values for the BP output remain in the range of 2.62 to 4.33 for the sinusoidal input voltage of constant frequency of 2.51MHz and variable amplitude between 10mV to 150mV.

Lastly, Monte-Carlo analysis is also performed to observe the tolerance variation of capacitive components on the performance of frequency response and pole frequency of the proposed circuit. The TAM BP output with 10% tolerance variation in $C_1 = C_2 = 25$ pF has been simulated for the presentation. The simulation was done simultaneously for five runs. The corresponding results are shown in Fig.8. These results demonstrate that capacitive tolerances (deviation) do not severely affect the circuit performance in term of frequency response and pole frequency.

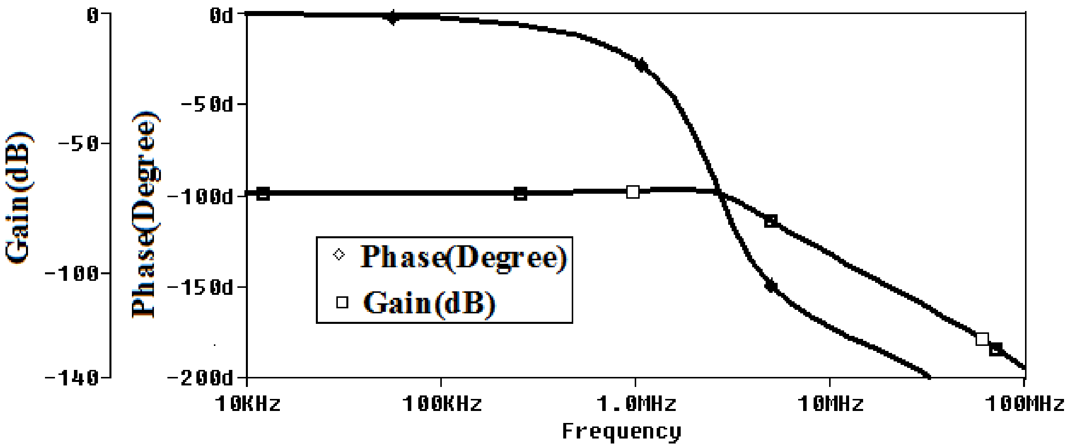
6 Conclusion

A new single input three output TAM biquad universal filter has been described in this paper which consits of only two MO-VDTAs, two grounded MOS resistors, two capacitors with one of which is permanentaly grounded and can realizes LP, BP, HP, BR and AP filtering responses. In addition, the proposed circuit offers the following advantages.

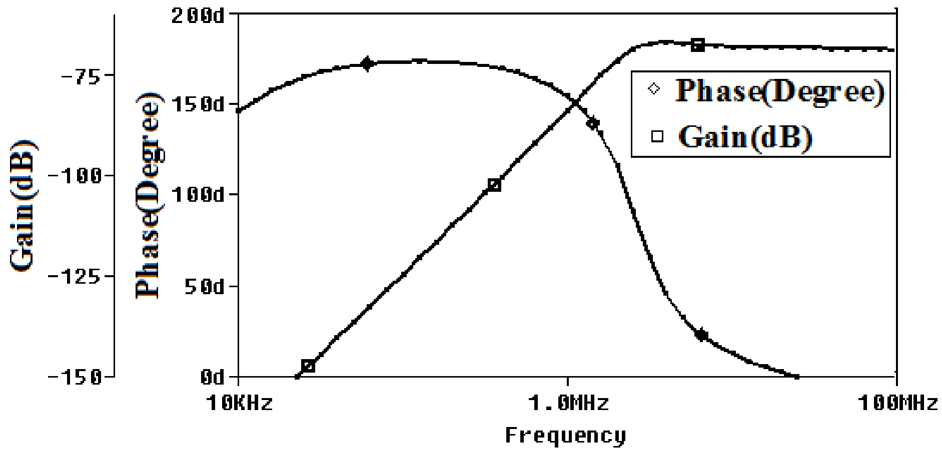
(i) Realization of all the five standard filtering responses in trans-admittance-mode with out requiring any inverted type and/or scaled type voltage input signal(s).
(ii) Use of grounded resistors which is easily realized using only two MOS transistors.
(iii) Availability of each trans-admittance filtering output explicitly at high impedance output.
(iv) Two of the voltage inputs are applied on high impedance input ports.
(v) All active and passive sensitivities are low and with in 0.5 in magnitude.
(vi) Low power consumption of 0.992mW.

(vii) Provide the feature of electronic tunability of filter parameters.
(viii) Provide the canonical structure.

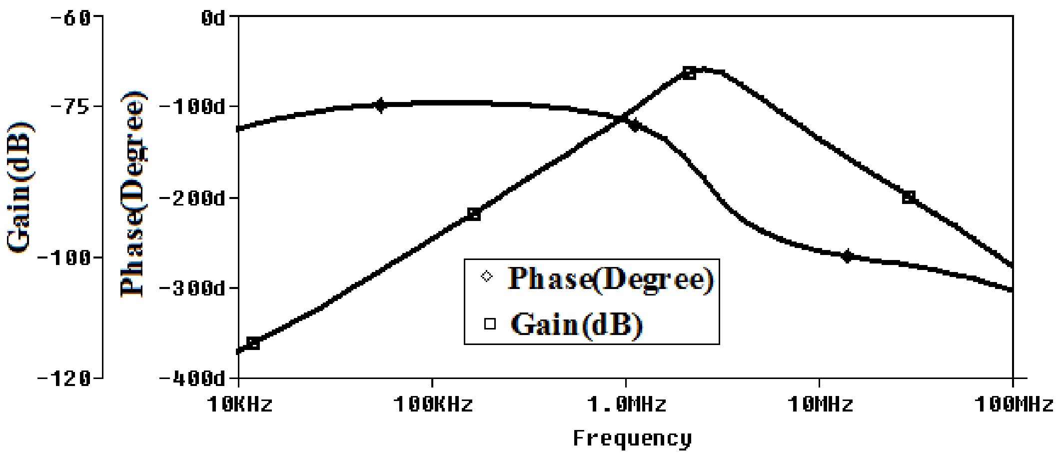
With above mentioned features it is very suitable to realize the proposed circuit in monolithic chip to use in battery powered, portable electronic equipments such as wireless communication system devices.



(a)



(b)



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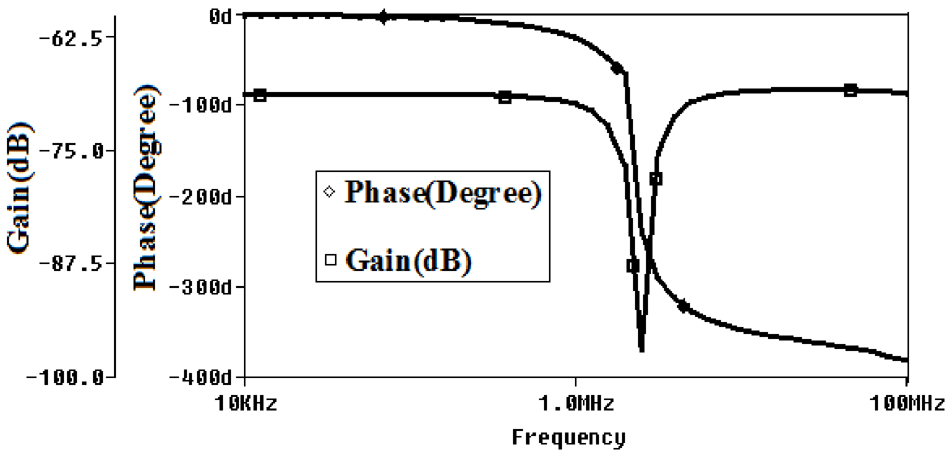

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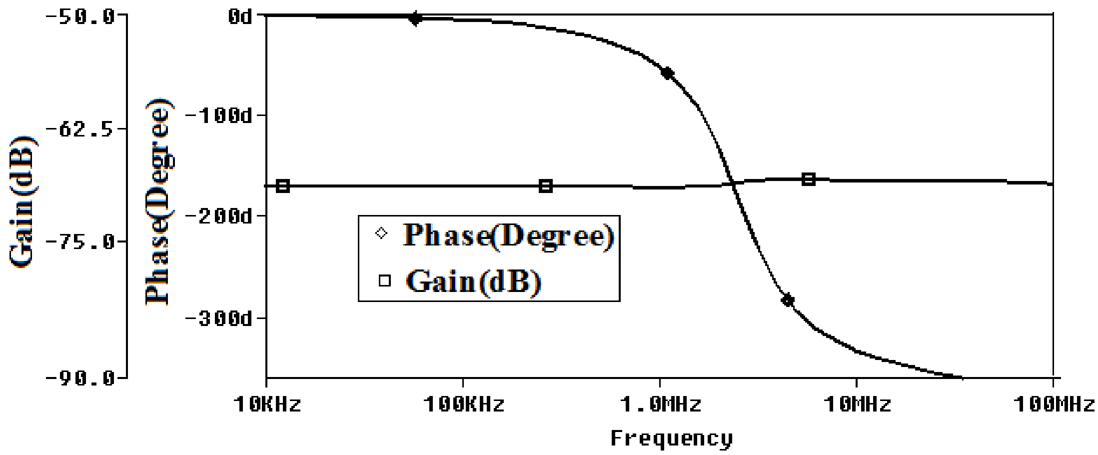
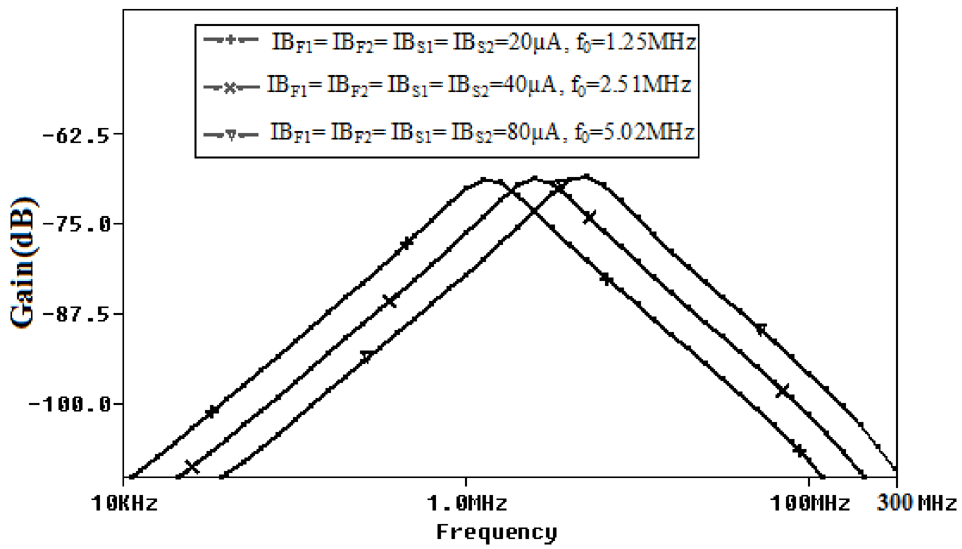
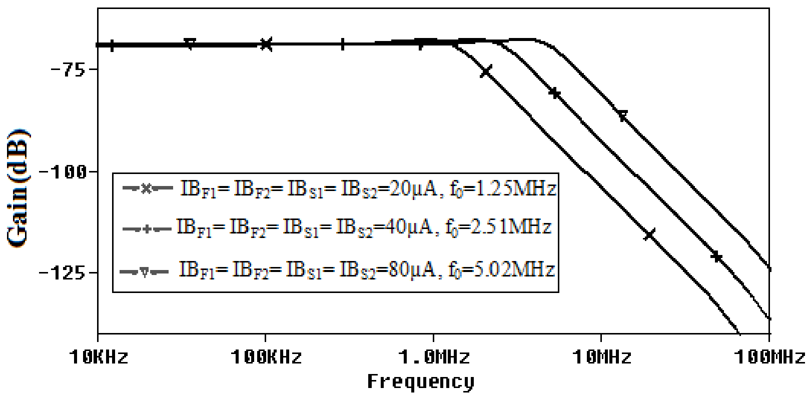


(e)

Fig.4: Gain and phase response of the (a) LP (b) HP (c) BP (d) BR (e) AP for proposed TAM filter of Fig.3

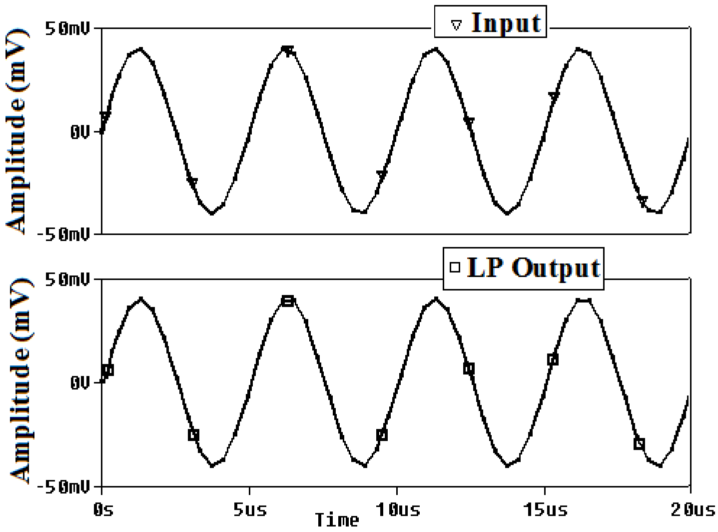


(a)

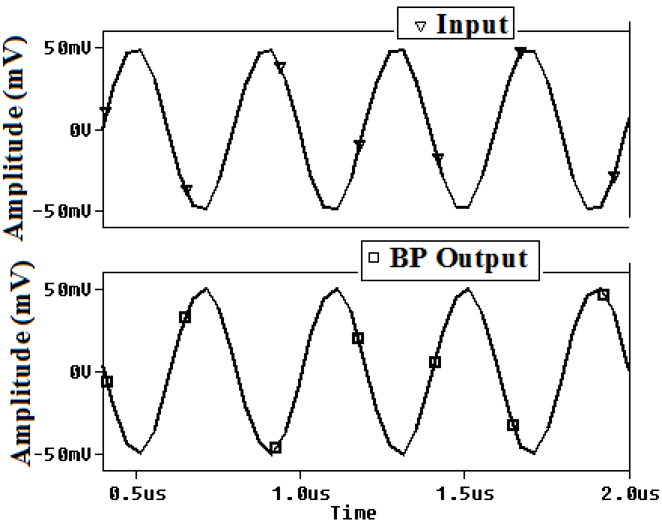


(b)

Fig.5 Electronic controllability of ω_0 of **(a)** BP response at Q_0=1 **(b)** LP response at Q_0=1

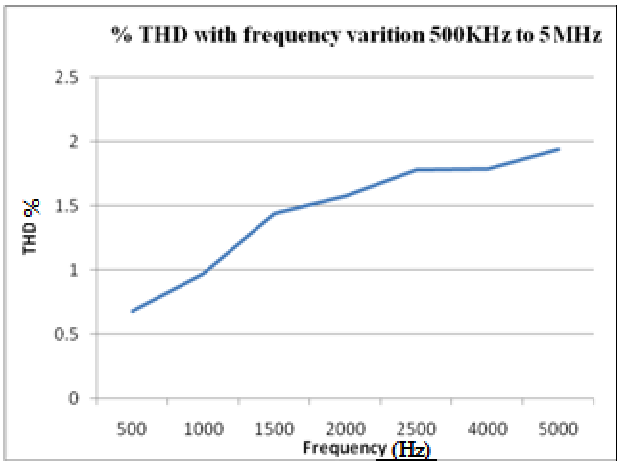


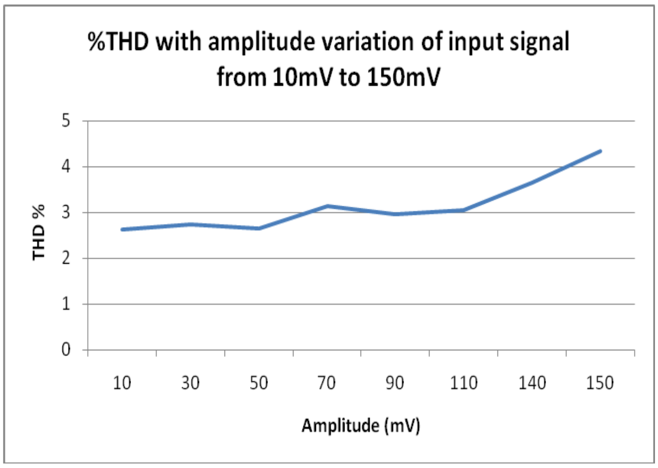
(a)



(b)

Fig.6 (a) Transient behavior of LP output for a sinusoidal input of 500KHz frequency **(b)** Transient behavior of BP output for a sinusoidal input of 2.51MHz frequency of proposed circuit in Fig.3





(a) (b)

Fig.7 %THD of (a) LP Filter (b) BP filter

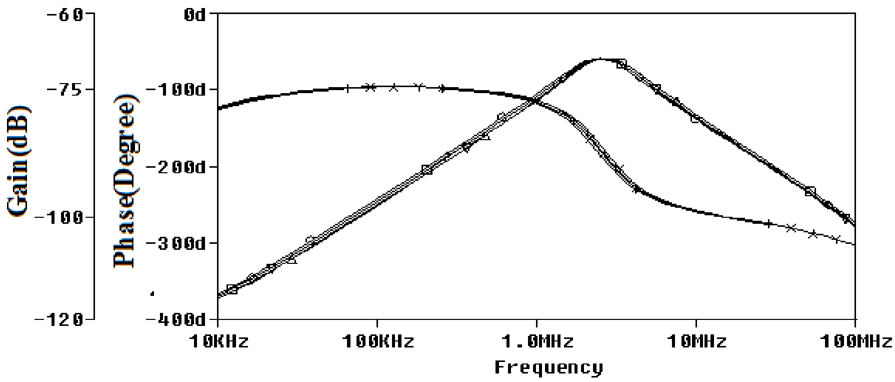


Fig.8 Montecarlo analysis of BP filter with 10% tolerance variation in capacitance

Table 2. Transistor Model parameters of 0.35 um TSMC file

.MODEL NMOS NMOS(LEVEL=3 TOX=7.9E-9 +NSUB=1E17 GAMMA=0.5827871 PHI=0.7 +VTO=0.5445549 DELTA=0 UO=436.256147 +ETA=0 THETA=0.1749684 +KP=2.055786E-4 +VMAX=8.309444E4 KAPPA=0.2574081 +RSH=0.0559398 NFS=1E12 TPG=1 XJ=3E-7 +LD=3.162278E-11 WD=7.04672E-8 +CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 +CJ=1E-3cvfr54 PB=0.9758533 MJ=0.3448504 +CJSW=3.777852E-10 MJSW=0.3508721)
.MODEL PMOS PMOS (LEVEL =3 TOX = 7.9E-9 +NSUB=1E17 GAMMA=0.4083894 PHI=0.7 +VTO=-0.7140674 DELTA=0 UO=212.2319801 +ETA=9.999762E-4 THETA=0.2020774 + KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5 + RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 +LD=5.000001E-13 WD=1.249872E-7 +CGDO=3.09E-10 CGSO=3.09E-10 + CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 +MJ=0.5 CJSW=4.813504E-10 MJSW=0.5)

Table 3. Transistors aspect ratios of CMOS implementation of MO-VDTA of Fig.2

MOS Transistors	Aspect Ratio
M1,M2,M5,M6	16.1/.7
M3,M4	28/.7
M7-M14	8.5/.7
M15-M20	7/.7
MR_i (i=1,2) for MOS resistance realization	3/1

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