Role of the threshold voltage and transconductance parameters of NMOS transistors in NMOS inverter performance for static and switching conditions of operation

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Abstract: The aim of this paper is to show the influence of the threshold voltage and transconductance parameters that characterize the NMOS transistors on the behavior of NMOS inverters in static and switching conditions of operation, as well as set directive that should be followed during the design phase of NMOS inverters that enable designers to design NMOS inverters with the best possible performance, depending on operation conditions. Designing the NMOS inverters with controlled parameters that characterize NMOS transistors in NMOS inverters also enables designers to design the logic circuits based in NMOS inverters (NMOS logic) with the best possible performance, according to the operation conditions and designers' requirements.

Key words: NMOS inverter, NMOS transistor, VTC characteristics, threshold voltage, critical voltages, noise margins, NMOS transconductance parameter, propagation delay times.

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1 Introduction

NMOS logic circuits represent the family of logic circuits which are realized with the highest packing density [1, 2, 3]. NMOS logic circuits contain only NMOS transistors, which enable to design circuits with smaller possible dimensions compared with other types of MOSFET transistors [3, 4]. The basic circuit in NMOS logic is NMOS inverter. Electrical and physical parameters that characterize the NMOS transistors determine the behavior of NMOS inverter, as for static conditions of operation, as well as dynamic conditions (or switching conditions) of operation [14]. The NMOS logic inverter is designed by interconnecting the two NMOS transistors; so that one of NMOS transistors plays the role of driver transistor and the other NMOS transistor play the role of nonlinear active load. NMOS inverters can be configured (designed) in several ways, but the configuration with depletion type of nonlinear active load achieves better performances compared with other type of configurations, so in particular will be discussed in the following [2]. The structure of NMOS logic inverter with depletion type of nonlinear active load is shown in Fig. 1.

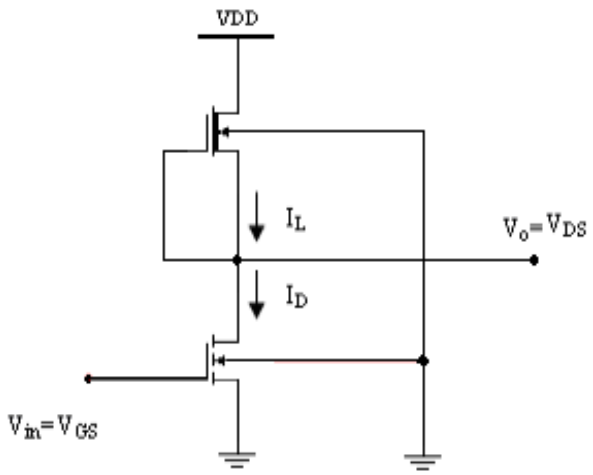

Fig. 1 NMOS inverter configuration with depletion type NMOS- load.

2 The impact of threshold voltage and transconductane parameters of NMOS transistors in VTC characteristic properties of NMOS- inverters

Behavior of NMOS inverter with depletion-type NMOS load for static conditions of operation is described by the voltage transfer characteristic (VTC) [5]. The characteristic properties that characterize the VTC characteristic are some critical voltage values at the input and output, as: V_{OH}, V_{OL}, V_{IL}, V_{IH} and V_{th} [2].

V_{OH} : maximum output voltage when the output voltage level is high or logic "1"

V_{OL} : minimum output voltage when the output voltage level is low or logic "0"

V_{IL} : maximum input voltage which can be interpreted as low voltage level or as logic "0"

V_{IH} : minimum input voltage which can be interpreted as high voltage level or as logic "1"

V_{th} : threshold voltage of NMOS inverter.

Critical voltage values are determined using combinations of operation regions (operation modes) of NMOS-driver transistor and NMOS-load transistor, depending on the level of the output voltage values relative to the voltage values at the input of NMOS driver transistor (enhancement type NMOS). In Tab. 1 are shown the operating regions and the voltage levels of NMOS transistors in NMOS inverter for critical voltage values at the input of driver transistor.

Tab. 1 The operating regions and the voltage levels of the driver and load transistors at critical voltage values in NMOS inverter.

V_{in}	V_o	*Operation region of driver transistor*	*Operation region of load transistor*
V_{OL}	V_{OH}	cut-off	linear
V_{IL}	$\approx V_{OH}$	saturation	linear
V_{IH}	small	linear	saturation
V_{OH}	V_{OL}	linear	saturation

NMOS transistors are constructed on the same substrate, therefore in NMOS transistor which acts as the load, the body effect must be taken in consideration [6, 7, 8, 9, 10, 11, 13].

$$V_{t,l} = V_{t0,l} + \gamma\left(\sqrt{\left|2\phi_F\right| + V_o} - \sqrt{\left|2\phi_F\right|}\right) \quad (1)$$

$V_{t,l}$ – threshold voltage of NMOS transistor as load,

$V_{t0,d}$ – threshold voltage of NMOS transistor as driver,

V_o – output voltage of NMOS inverter,

V_{in} – input voltage of NMOS inverter,

ϕ_F – Fermi potential,

λ – body coefficient.

Using drain currents of NMOS transistors in NMOS inverter depending on the input voltage levels, respectively output voltage levels, and the necessary conditions to determine the critical values can be derived expressions for the critical voltage values at the input and output of NMOS inverter, as:

$$V_{OH} = V_{DD} \quad (2)$$

$$V_{OL} = V_{OH} - V_{t0,d} + \sqrt{\left(V_{OH} - V_{t0,d}\right)^2 - \frac{k_l}{k_d}\left|V_{t,l}(V_{OL})\right|^2} \quad (3)$$

$$V_{IL} = V_{t0,d} + \frac{k_l}{\sqrt{k_l k_d + k_d^2}}\left|V_{t,l}(V_o)\right| \quad (4)$$

$$V_{IH} = V_{t0,d} + 2\left|V_{t,l}(V_o)\right|\sqrt{\frac{k_l}{3k_d}} \quad (5)$$

k_l – transconductance parameter of NMOS transistor as load (NMOS-load),

k_d – transconductance parameter of NMOS transistor as driver(NMOS-driver.

The values of output critical voltage V_{OL} are found using the numerical interaction between expressions (1) and (3), while the input critical voltage values V_{IL} and V_{IH} are found using the numerical interaction between expressions of the output voltage and the expressions for the critical values of voltage at the input. Interaction methods enable convergence of voltage critical values to the correct values. Also, static power dissipation which appears to output in low state (V_{OL}) depends on parameters of NMOS transistor as load [12].

$$P_{DC} = \frac{k_l V_{DD} V_{t,l}^2}{4} \quad (6)$$

Parameters that influence on the behavior of NMOS inverters for static conditions of operation are: the value of the threshold voltage of driver transistor, the value of the threshold voltage of load transistor, the ratio of the transconductance parameters of NMOS transistors and values of voltage source.

3 The impact of threshold voltage and transconductane parameters of NMOS transistors in switching characteristics of NMOS inverter

The performance of NMOS inverter during switching conditions evaluate by propagation delays of output voltage related by input voltage. Propagation delay times are dependent on the physical and electrical parameters of the NMOS transistors which construct the NMOS inverter. To calculate propagation delay times will be used the NMOS inverter with an equivalent lumped linear capacitance, connected between the output node and ground (C_l capacitance) shown in Fig. 2. The equivalent lumped capacitance will be called the load capacitance, which is the sum of parasitic capacitance components that appear in NMOS inverter.

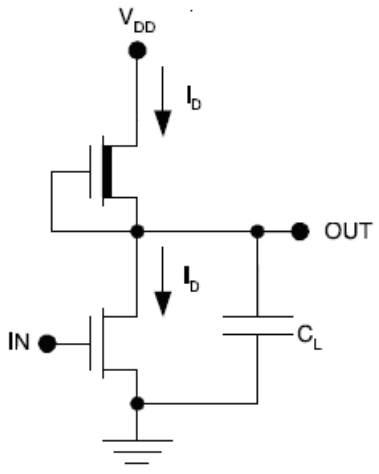

Fig. 2 The NMOS-inverter with equivalent lumped capacitive load.

The lumped parasitic capacitance components expression is:

$$C_l = C_{gd,driver} + C_{gd,load} + C_{db,load} + C_{db,driver} + C_{sb,load} + C_{\text{int}} + C_g \quad (7)$$

$C_{gd,driver}$ - gate-to-drain parasitic capacitance of NMOS-driver,

$C_{gd,load}$ - gate-to-drain parsitic capacitance of NMOS-load,

$C_{db,load}$ - drain-to-body parasitic capacitance of NMOS-load,

$C_{db,driver}$ - drain-to-body parasitic capacitance of NMOS- driver,

$C_{sb,load}$ - source-to-body parasitic capacitance of NMOS-load,

C_{int} - lumped interconnect parasitic capacitance,

C_g - gate parasitic capacitance of an another NMOS-inverter connected at output of NMOS-inverter.

Some of the parasitic capacitance components aren't included in lumped capacitance expression, because those not have effect on the transient behavior of the NMOS-inverter.

Propagation delay times during transition output voltage from low-to-high level t_{PLH}, when input voltage have transition from high-to-low level (when the fall time is negligible), calculate according to the case when the driver transistor driver goes into cut-off and load transistor goes into saturation mode of operation. After application of derivation procedure for calculation propagation delay t_{PLH}, using load drain current and capacitive current during charge up, the propagation delay time for low-to-high output transition can be expressed as,

$$I_{D,l} = \frac{k_l V_{t,l}^2}{2} \quad (8)$$

$$C_l \frac{dV_o}{dt} = \frac{k_l V_{t,l}^2}{2} \quad (9)$$

$$t_{PLH} = \frac{V_{DD} C_L}{k_l V_{t,l}^2} \quad (10)$$

The propagation delay time of the output voltage during the transition from high-to-low level t_{PHL}, when the input voltage switches from low-to-high level (with negligible rise time), calculate based in

case that the NMOS-driver transistor is in saturation mode, while the NMOS-load transistor operates in the linear region of operation. Applying the same logic as for the calculation of the propagation delay t_{PLH}, and using only current driver transistor and capacitive current during charge down, while ignoring the current of load transistor, the approximate expression for propagation delay time t_{PLH} can be expressed as,

$$t_{PHL} \approx \frac{V_{DD} C_l}{k_d (V_{DD} - V_{t0,d})^2} \qquad (11)$$

From expressions (10) and (11) shows that propagation delay times are dependent from parameters that characterize the NMOS transistors in NMOS inverter. The propagation delay t_{PLH} depends on the parameters of NMOS transistor which plays the role of load (NMOS-load transistor), and the propagation delay t_{PHL} depends on the parameters of NMOS driver-transistor.
Propagation delay times are parameters which determine the maximal work frequency of NMOS-inverters.
Switching power dissipation of NMOS- inverter evaluated by expression,

$$P_{AC} = f C_l V_{DD} \qquad (12)$$

f- switching frequency

The overall power dissipation of NMOS- inverter is,

$$P_D = P_{DC} + P_{AC} \qquad (13)$$

or

$$P_D = \frac{k_l V_{DD} V_{t,l}^2}{4} + f C_l V_{DD}^2 \qquad (14)$$

The static power dissipation is dominate on switching power dissipation (or dynamic power dissipation) especially at low switching frequency of driver voltage at input of NMOS-inverter, and when fan-out parameter is low.

4 Results and Discussion

The impact of threshold voltage of NMOS-driver transistor and threshold voltage of NMOS-load transistor on the critical value of the output voltage V_{OL} when the ratio of NMOS transistors transconductance parameters has the value $k_d / k_l = 1$, $\gamma = 0.126 V^{1/2}$, t_{ox} = 7.5 nm (the thickness of the oxide layer) and V_{DD} = 2.5 V are shown in Fig. 3 and Fig. 4.

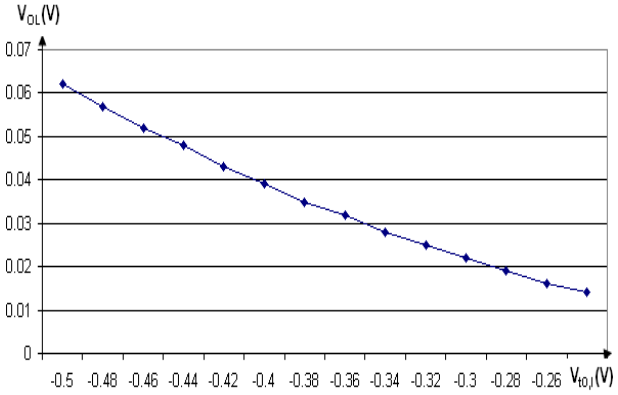

Fig. 3 The dependence of the output voltage critical value (V_{OL}), as a function of the NMOS-load threshold voltage ($V_{t0,l}$), when $V_{t0,d}$ = 0.5 V.

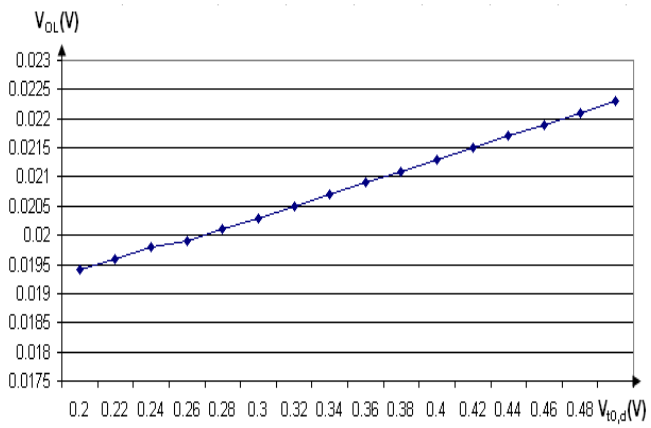

Fig. 4 The dependence of the output voltage critical value (V_{OL}), as a function of the NMOS-driver threshold voltage ($V_{t0,d}$), when $V_{t0,l}$ = - 0.3 V.

Presented results in Fig. 3 and Fig. 4 show that for the smaller absolute values of the load threshold voltage, as well as the smaller values of the driver threshold voltage, the output critical value V_{OL} is reduced to smaller values.
Impact of transconductance parameters ratio of NMOS transistors (by the driver-to-load ratio) in the output critical value V_{OL}, when $\gamma = 0.126 V^{1/2}$, t_{ox} = 7.5 nm, $V_{t0,l}$ = – 0.3 V, $V_{t0,d}$ = 0.5 V and V_{DD} = 2.5 V is shown in Fig. 5.

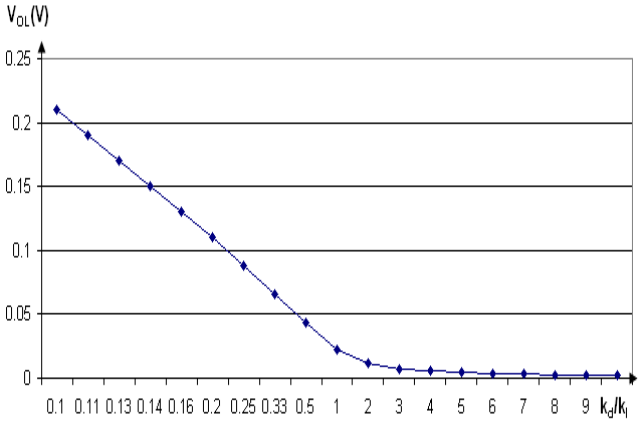

Fig. 5 The dependence of the output critical value V_{OL}, as a function of the NMOS transconductance parameters ratio (k_d / k_l).

From Fig. 5 it can be seen that for the higher value of the NMOS transconductance parameters ratio, the output critical voltage value V_{OL} is reduced to lower values with more significant impact on the band of small values.

The impact of the NMOS threshold voltage values and NMOS transconductance parameters ratio in input critical voltage values (V_{IL} and V_{IH}), where $\gamma = 0.126V^{1/2}$, t_{ox} = 7.5 nm and V_{DD} = 2.5 V are presented in Fig. 6, Fig. 7, Fig. 8, Fig. 9, Fig. 10 and Fig. 11.

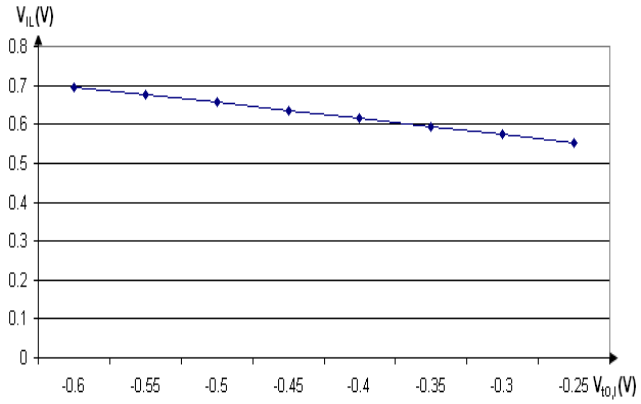

Fig. 6 The dependence of the input critical voltage V_{IL}, as a function of the NMOS-load transistor threshold voltage ($V_{t0,l}$), when the ratio of transconductance parameters k_d / k_l = 2 and $V_{t0,d}$ = 0.5 V.

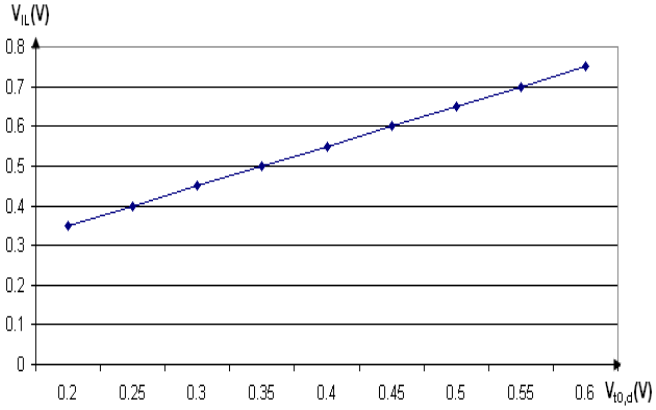

Fig. 7 The dependence of the input critical voltage V_{IL}, as a function of the NMOS-driver transistor threshold voltage ($V_{t0,d}$), when the ratio of transconductance parameters k_d/k_l = 2 and $V_{t0,l}$ = – 0.5 V.

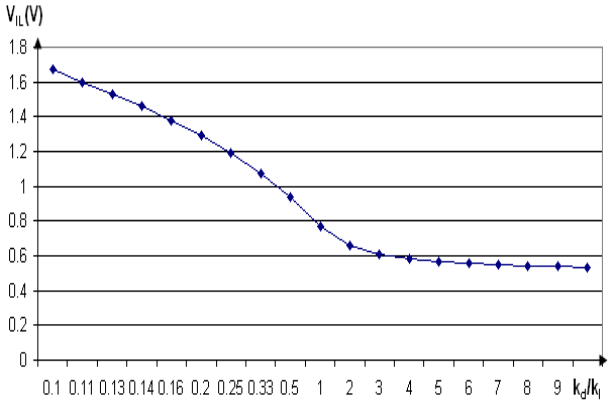

Fig. 8 The dependence of the input critical voltage V_{IL} from NMOS transconductance parameters ratio (k_d/k_l), when $V_{t0,l}$ = – 0.5 V dhe $V_{t0,d}$ = 0.5 V.

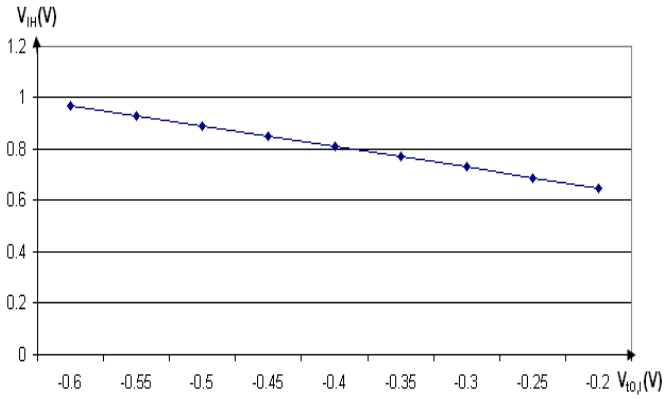

Fig. 9 The dependence of the input critical voltage V_{IH}, as a function of the NMOS-load transistor threshold voltage ($V_{t0,l}$), when the ratio of transconductance parameters k_d/k_l = 2 and $V_{t0,d}$ = 0.5 V.

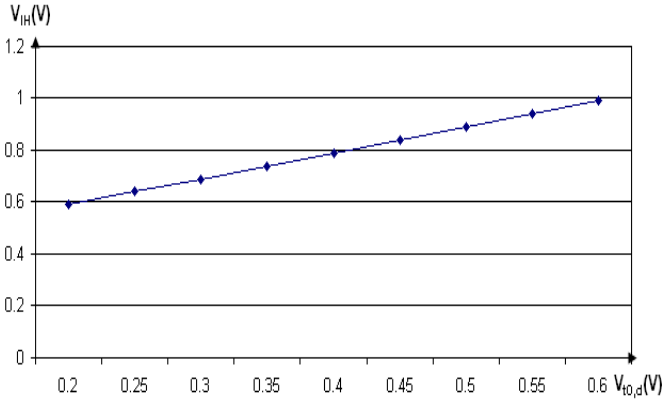

Fig. 10 The dependence of the input critical voltage V_{IH} from NMOS-driver transistor threshold voltage ($V_{t0,d}$), when the ratio of transconductance parameters $k_d/k_l = 2$ and $V_{t0,l} = -0.5$ V.

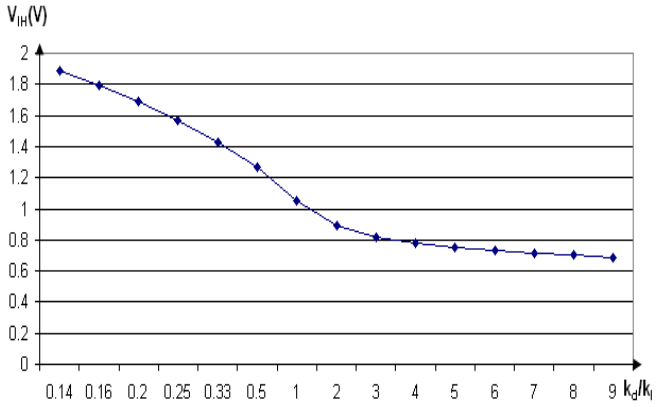

Fig. 11 The dependence of the input critical voltage V_{IH} from NMOS transconductance parameters ratio (k_d/k_l), when $V_{t0,l} = -0.5$ V dhe $V_{t0,d} = 0.5$ V.

The presented results from Fig. 6 to Fig. 11 show that for higher absolute values of the NMOS-load transistor threshold voltage, as well as the higher value of the NMOS-driver transistor threshold voltage, the input critical voltage values (V_{IL} and V_{IH}) will have higher values, while for higher values of the NMOS transistors transconductance parameters ratio, the input critical voltage values will be lower, with more sensitivity in the low values band of the NMOS transconductance parameters ratio.

NMOS-inverter noise margins for both logic voltage levels depend by input and output critical voltage values. The impact of the threshold voltage values and the ratio of NMOS transconductance parameters in noise margins are shown in Fig. 12, Fig. 13 and Fig. 14.

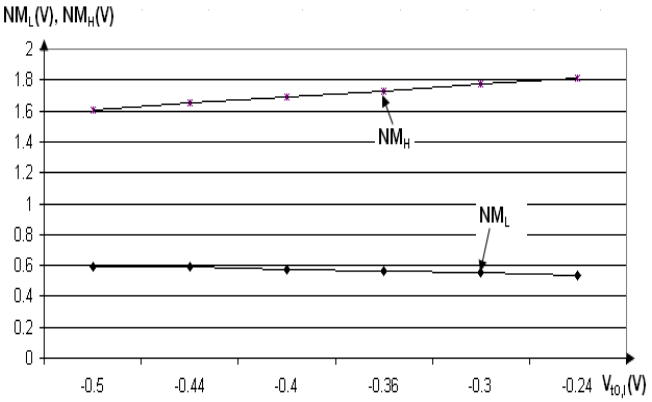

Fig. 12 The dependence of the noise margins for both logic levels (NM_L, NM_H), as a function of the NMOS-load transistor threshold voltage ($V_{t0,l}$), when $V_{t0,d} = 0.5$ V and $k_d/k_l = 2$.

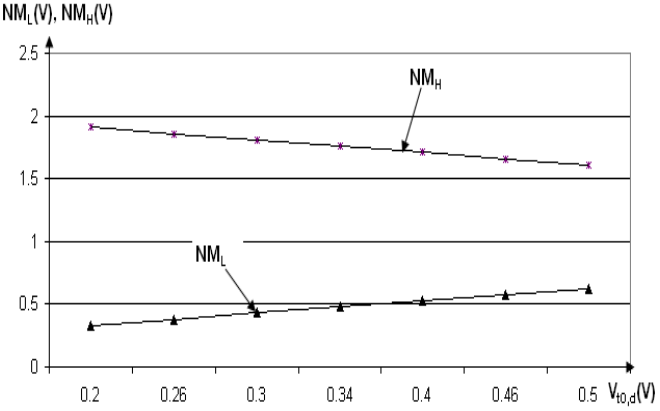

Fig. 13 The dependence of the noise margins for both logic levels (NM_L, NM_H), as e function of the NMOS-driver transistor threshold voltage ($V_{t0,d}$) when $V_{t0,l} = -0.5$ V and $k_d/k_l = 2$.

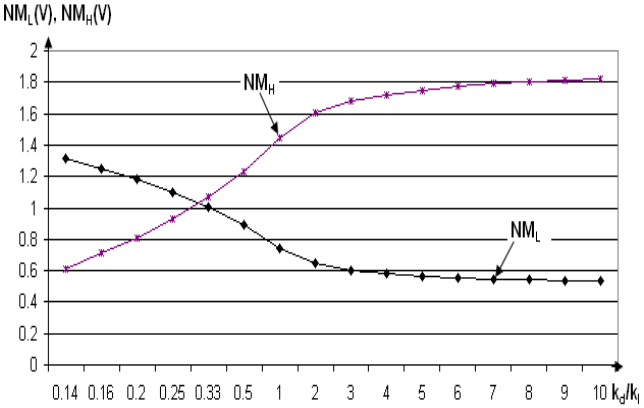

Fig. 14 The dependence of the noise margins for both logic levels (NM_L, NM_H) from the NMOS transistors transconductance parameters ratio (k_d/k_l), when $V_{t0,l} = -0.5$ V and $V_{t0,d} = 0.5$ V.

The presented results in Fig. 12, Fig. 13 and Fig. 14 show that for the lower absolute values of NMOS-load threshold voltage values, noise margins for high level (NM_H) will increase, while noise margin for low levels (NM_L) will decrease. For the lower values of NMOS-driver threshold voltage, noise margins for high level (NM_H) will increase, whereas it will decrease for the low level (NM_L). When value of NMOS transconductance parameters ratio increases, noise margins for the high level increase, whereas for the low level decrease.

In Fig. 15, Fig. 16 and Fig. 17 is shown the influence of the NMOS transistor threshold voltage values and the NMOS transistors transconductance parameters ratio in VTC characteristic shape. From presented characteristics show that for lower absolute values of NMOS-load transistor threshold voltage, and for lower values of NMOS-driver transistor threshold voltage, the VTC characteristic shift to the left, compared to the higher values and the slope of the VTC characteristic remains almost the same. While the value of NMOS transistors transconductance parameter ratio increases, the slope of the VTC characteristic rise and shows better switching performances.

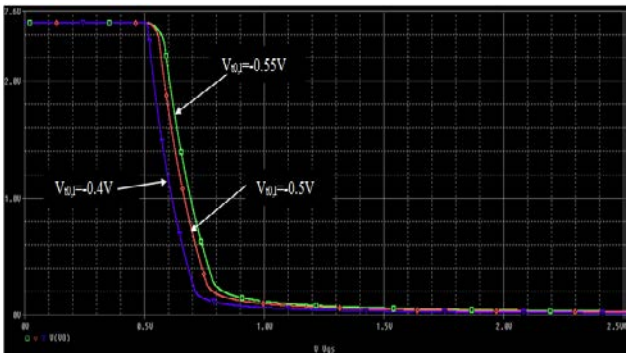

Fig. 15 The VTC characteristic forms of NMOS inverter for some parametric values of the NMOS-load transistor threshold voltage, when: $V_{t0,\ d}$ = 0.5 V, k_r = 4, L = 0.18 μm, W = 1 μm and V_{DD} = 2.5 V.

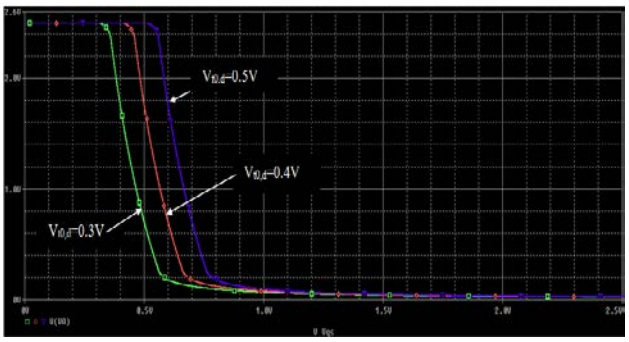

Fig. 16 The VTC characteristic forms of NMOS inverter for some parametric values of the NMOS-driver transistor threshold voltage, when: $V_{t0,l}$ = – 0.5 V, k_r = 4, L = 0.18 μm, W = 1 μm and V_{DD} = 2.5V.

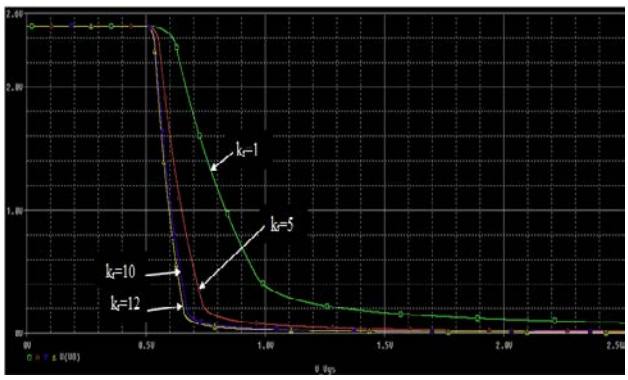

Fig. 17 The VTC characteristic forms of NMOS inverter for some parametric values of NMOS transistors transconductance parameters ratio (k_r = k_d/k_l) when: $V_{t0,d}$ = 0.5 V, $V_{t0,l}$ = – 0.5 V, L = 0.18 μm, W = 1 μm and V_{DD} = 2.5V.

Based on VTC characteristic of NMOS- inverter presented in Fig. 15, Fig. 16 and Fig. 17 show that the threshold voltage of two NMOS transistors and transconductance parameter ratio of NMOS transistors will have significant impact in value of NMOS- inverter threshold voltage as: for higher values of NMOS-driver transistor threshold voltage the threshold voltage of NMOS-inverter will be higher, and for lower values of NMOS-load transistor as well for higher values of NMOS transistors transconductance parameters ratio the value of NMOS- inverter threshold voltage will be lower. The NMOS transistors transconductance parameters ratio (most specifically for lover values of NMOS transistors transconductance parameter ratio) and the NMOS – driver transistor have more significant impact compared with NMOS-load transistor threshold voltage in values of NMOS-inverter threshold voltage (V_{th}).

The dependence of propagation delay times from the threshold voltage values of the driver-transistor and load-transistor for several different values of the transistor tranconductance parameters are shown in Fig. 18 and Fig. 19

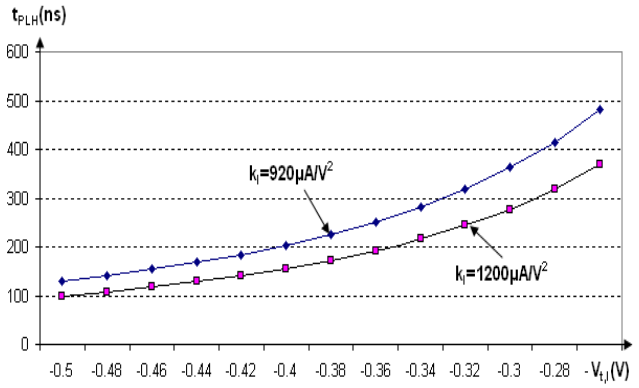

Fig. 18 The dependence of the propagation delay times t_{PLH} on level of the NMOS-load threshold voltage (V_{tl}) when transconductance parameter (k_l) of NMOS-load have two parameters values, and V_{DD} = 2.5 V, C_l = 12 pF.

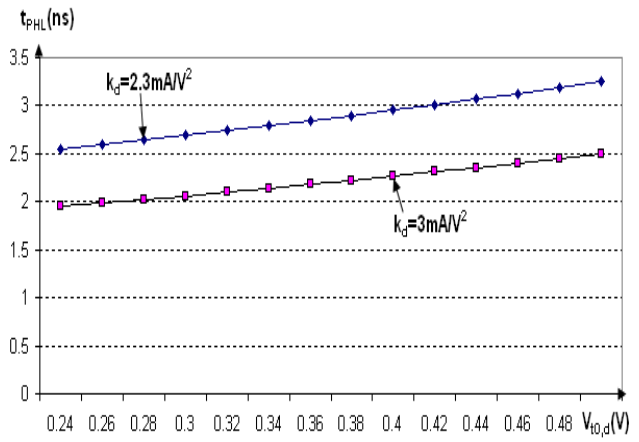

Fig. 19 The dependence of the propagation delay times t_{PHL} on level of the NMOS-driver threshold voltage ($V_{t0,d}$) when transconductance parameter (k_d) of NMOS-driver have two parameters values, and V_{DD} = 2.5 V, C_l = 12 pF.

The results presented in Fig. 18 and Fig. 19 show that the propagation time delays will reduced when the values of the NMOS-load transistor threshold voltage is more negative, and the values of the NMOS-driver transistor threshold voltage are more smaller, as well when the NMOS-load and NMOS-driver transistors transkonductance parameters will have higher values.

The behavior of NMOS-inverter when the input voltage at NMOS-driver transistor has rectangular shape with negligible rise and fall time for some different value of NMOS-load transistors transkonductance parameters for two different values of NMOS-load threshold voltage (NMOS-depletion type) when output load is an equivalent lumped capacitive load, are shown in Fig. 20 and Fig. 21.

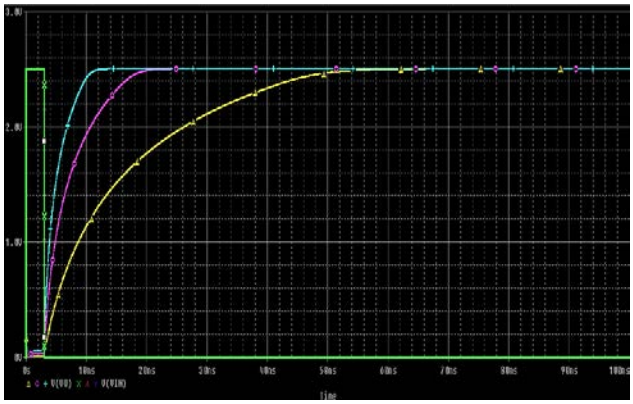

Fig. 20 Time response of output voltage in NMOS inverter on input driver voltage for some different values of NMOS-load transistor transconductance parameters ($k_{l1} < k_{l2} < k_{l3}$, or $k_{l3} = 2k_{l2} = 6k_{l1}$), when $V_{t0,l}$ = - 0.5 V, V_{DD} = 2.5 V and C_l = 12 pF.

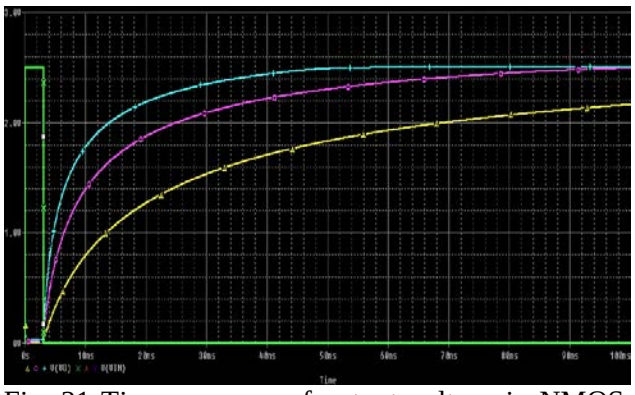

Fig. 21 Time response of output voltage in NMOS inverter on input driver voltage for some different values of NMOS-load transistor transconductance parameters ($k_{l1} < k_{l2} < k_{l3}$, or $k_{l3} = 2k_{l2} = 6k_{l1}$), when $V_{t0,l}$ = - 0.4 V, V_{DD} = 2.5 V and C_l = 12 pF.

The behavior of NMOS-inverter when the input voltage at NMOS-driver transistor has rectangular shape with negligible rise and fall time for some different value of NMOS-driver transistors transkonductance parameters (NMOS- enhancement type) when output load is an equivalent lumped capacitive load, is shown in Fig. 22.

The results presented from show that the higher value of the transkonductance parameter and the higher value of the threshold voltage by absolute value of the NMOS load-transistor, propagation delay time t_{PLH} of the NMOS-inverter will be smaller and the shape of the response time will have greater slope. Also, higher values of the transconductance parameter of driver NMOS transistor time delay t_{PHL} will result in smaller values and larger slope of the response time.

Impact of V_{t0} voltage of NMOS-driver transistor is significantly smaller in delay time t_{PHL}, compared with the impact the threshold voltage $V_{t,l}$ of NMOS-load transistor in time delay t_{PLH}. Impact on the propagation delay time values will have also and source voltage values V_{DD} and equivalent capacitive load C_l connected to the output of inverter (fan-out parameter).

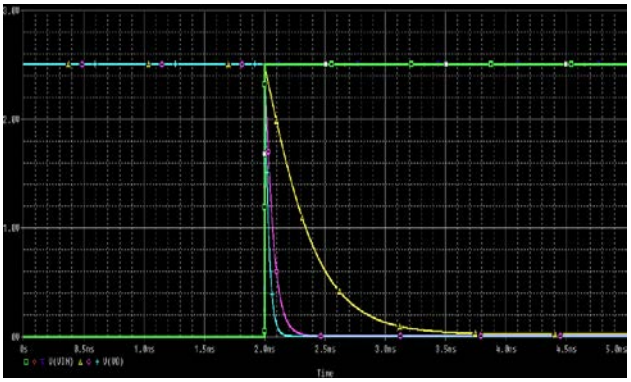

Fig. 22 Time response of output voltage in NMOS inverter on input driver voltage for some different values of NMOS-driver transistor transconductance parameters ($k_{d1} < k_{d2} < k_{d3}$, or $k_{d3} = 2k_{d2} = 10k_{d1}$), when $V_{t0,l} = -0.5$ V, $V_{DD} = 2.5$ V and $C_l = 12$ pF.

Propagation delays t_{PHL} are significantly smaller than the propagation delays t_{PLH}, so during the design phase of NMOS-inverters always must taken into consideration the propagation delay t_{PLH}, as well as the other parameters. Propagation delays are deterministic factor for maximum frequency of NMOS-inverter speed.

Conclusion

If during the design phase of NMOS inverter, the threshold voltage values of NMOS transistors and ratio of NMOS transistors transconductance parameters are controlled, or fit, NMOS inverter can be designed with high performance as for static conditions of operation, as well as for dynamic conditions of operations, depending on the designer requirements and operating conditions.

As for the output critical voltage value V_{OL}, the transconductance parameter ratio of the NMOS transistors has a significant impact, compared to their threshold voltage values.

As for the input critical voltage value V_{IL}, the transconductance parameter ratio of the NMOS transistors and the value of the NMOS-driver transistor threshold voltage have a significant impact.

As for the input critical voltage value V_{IH}, the transconductance parameter ratio of the NMOS transistors and their threshold voltage values have a significant impact.

As for the threshold voltage of NMOS inverter V_{th}, the transconductance parameter ratio and threshold voltage of NMOS-driver transistor have more impact than threshold voltage of NMOS-load transitor.

As for the noise margin and the VTC characteristic slope, the ratio of NMOS transistors transconductance parameters has a dominant impact. When NMOS transistors transconductance parameters are matching, NMOS inverters can be designed with equal noise margin for two logic levels. Also for lower absolute value of NMOS-load transistor threshold voltage the static power dissipation results in lower value when NMOS inverter is in low output state (V_{OL}).

The propagation delay times are significant factor which determine the maximal operation frequency of NMOS- inverters, and in design phase of NMOS-inverters must taken in consideration. The parameters which characterize NMOS transistors are determine factor in time response of NMOS-inverter.

As for the propagation delay times, the threshold voltage of NMOS-load transistor and transconductance parameters of both NMOS-transistors have more impact than threshold voltage of NMOS-driver transistor. Propagation delay times during transition output voltage from low-to-high level t_{PLH} is dominant compared with propagation delay times during transition output voltage from high-to-low level t_{PHL}, then during design phase of NMOS-inverter the parameters of NMOS-load transistor must selected to appropriate values.

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