

Proposal of an ASIC CMOS for Sliding Mode Control of Switched Reluctance Aerogenerators

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Abstract: This paper proposes an ASIC CMOS for sliding mode control (direct power one) applied to switched reluctance aerogenerators. The topology of the circuit is designed in order to carry out, in the most optimal way, the mathematical function which processing directly the power error and supply the turn-off angle to the power system converter. The specifications and simulation performance are in close agreement, which validate the proposed compact design. The ASIC final layout is also presented.

Key-Words: ASIC; CMOS; SRG; sliding mode control; wind energy.

1 Introduction

The growing demand for energy sources as an alternative to fossil fuels becomes renewable energy a great area of research, which has been explored by many countries around the world. Among these alternatives, the wind energy is one of most important and most environmentally-friendly [1].

For this purpose, the Switched Reluctance Machine (SRM) is a type of device that can be used in wind generation for micro-grids or isolated systems with relatively low loads, due to it can operate at variable speed with high efficiency and low cost [2, 3, 4]. In the Figure 1 is presented a visual diagram of a possible wind generation system connected to the grid system using a Switched Reluctance Generator (SRG).

There are several academic papers that discuss techniques to control the SRG [5, 6, 3]. In [7], the author proposes a control strategy for the SRG connected to the power grid based on sliding mode control. This strategy proposes the control acts directly on the generated power.

In the other way, the steady growth of the CMOS (Complementary Metal-Oxide-Semiconductor) technology to implement integrated circuit has been shown as a trend in the design of new devices to cater the increasing demand for analog and digital

ASIC (Application Specific Integrated Circuit) systems. These ICs (Integrated Circuits) are customized for a particular use, rather than ICs for general purpose utilization [8].

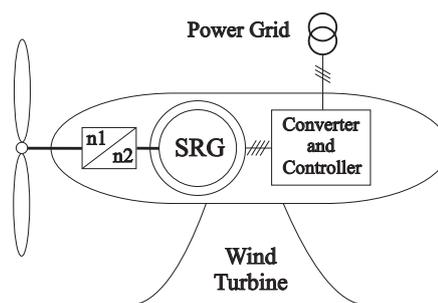


Figure 1: Wind generation system connected to the power grid using an SRG.

In this context, this paper presents the design of an analog integrated circuit for sliding mode control. It is implemented by dedicated CMOS Operational Amplifiers, which perform the direct power control of SRG. This topology is a full ASIC circuit to be used as an alternative to traditional control implementations by programmable processors [9]. The ASIC design uses the $0.35\mu\text{m}$ CMOS process models from AMS (Austriamicrosystems) foundry [10].

2 SRG and the Direct Power Control

SRG operation is based on the reluctance variation of its rotor magnetic circuit [11]. The inductance in an SRM is related to the reluctance, and it presents a linear variation in accordance with the poles' alignment position of rotor and stator, having a maximum inductance when the poles are fully aligned and a minimum inductance when the poles are completely misaligned. To operate as a generator, the SRM must have their phase excited during degrowth of its inductance [11, 4].

There are several power converters for activating SRG, however the configuration commonly used is the HBC (Half-Bridge Converter), which is presented in Figure 2 [12]. Its operation is in two steps: 1) Excitation step, which both SRG switches of each phase are activated, making the bus voltage V_{dc} to energize the stage, causing an increase in current flow through the coil and transferring energy to its magnetic field and; 2) Generation step, which both switches are turned off (open switches) and the current starts to flow by the diodes to load [13].

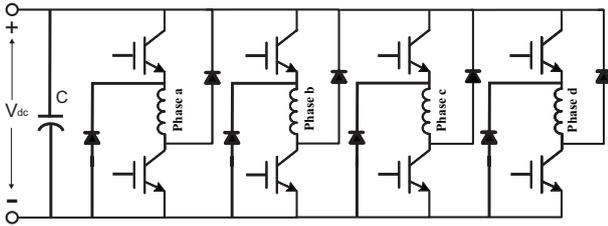


Figure 2: Power HBC.

As strategy control, in this paper has adopted the SM-DPC (Sliding Mode - Direct Power Control) technique, previously reported in [7]. In this one, the wind generation system is based on the control of two separate converters, in which the HBC connected to the SRG regulates the extraction of the maximum electrical power generated by the wind system, and a second converter connected directly to the power grid is responsible for regulating the continuous voltage V_{dc} , allowing that the energy generated by SRG has been sent to the power grid [14]. The switching surface of the HBC is defined by the processing of the error between a reference power value, P_{ref} , and the instantaneous power value generated by the system, P , where this value is calculated from the measured values of voltage and current of the SRG. An expression that represents this error is given by:

$$ep = P_{ref} - P \quad (1)$$

The set S of the switching surface is given by: [14]:

$$S = s_1 = ep + kd \frac{dep}{dt} \quad (2)$$

where: kd is a constant that represents the derivative gain defined in accordance to desired system response.

The sliding mode system controls the power of the SRG by the actuation at the turn-off angle θ_{off} of the HBC. The turn-on angle θ_{on} is kept at a fixed value. The control law that reproduces this behavior is given by [14]:

$$\theta_{off} = \left(kp + \frac{ki}{s} \right) eval(s_1) \quad (3)$$

where: ki and kp are the PI controller gains, and the $eval$ function is responsible for determining the reaction of the control system, acting linearly with saturation limits, as can be seen in (4).

$$eval(s_1) = \begin{cases} s_1 ke & \text{if } l_{min} < x < l_{max}, \\ l_{max} & \text{if } x > l_{max}, \\ l_{min} & \text{if } x < l_{min}. \end{cases} \quad (4)$$

where: ke is a constant that represents the $eval$ function gain and l_{min} and l_{max} represent the minimum and maximum limits, respectively.

The Figure 3 shows the block diagram of the DPC-SM for the SRG, where can be observed that the error processing is carried out by comparing of the P_{ref} signal with the P signal and the switching surface S is calculated from equation (2). Thus, the turn-off angle θ_{off} , presented by equation (3), is found through the action of the PI controller applied to the switching surface S , and processed by the $eval$ function.

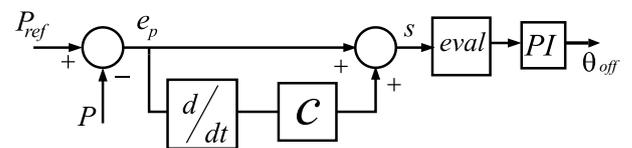


Figure 3: Block diagram of the SM - DPC adopted.

3 ASIC - Basic Block - Operational Amplifier

3.1 CMOS Operational Amplifier Architecture

The CMOS technology is widely used in the design of operational amplifiers (opamps) [15, 16] and, as a rule, a designer must accomplish the most of the required functions using only MOS transistors and small

capacitors [8, 17]. The Figure 4 presents the complete schematic of the opamp adopted as the core of the proposed ASIC. The opamp is composed by a rail-to-rail input stage with two complementary folded-cascode circuits and a rail-to-rail output stage biased in Class-AB. For easily visualization of the schematic, the bias circuit was omitted in the schematic. This one is formed by MOS voltage dividers, which provide the biasing voltages V_{b1} - V_{b4} .

The rail-to-rail input stage is implemented with two complementary circuits (PMOS differential pair), MP3 and MP5, connected in parallel with an NMOS differential pair, MN4 and MN6 [18, 19]. The first circuit is composed by PMOS transistors, MP1, MP3 and MP5, and by NMOS transistors, MN8, MN10, MN12 and MN14. The second circuit is composed by NMOS transistors, MN2, MN4, MN6, and by PMOS transistors, MP7, MP9, MP11 and MP13. The differential pairs are biasing by MP1 and MN2 transistors, which operate as current sources, providing a biasing current to the circuit [20].

The MP7-MN10 transistors are current mirrors and, together with the MP11-MN14 transistors, represent a summing circuit that adds the signals from the input stage and aid to improve the voltage gain achieved by the input differential pairs. They are biasing by a floating current source formed by MP15 and MN16 transistors [21, 22].

Each of the differential pairs leads the input signal by a different path and generates an independent A_{VP} (Voltage Gain). The ones of PMOS and NMOS differential pairs can be found by (5) and (6), respectively, and the input stage gain is given by (7) [23].

$$A_{VP} \approx -\frac{gm_5}{(gd_5 + gd_{10})} \cdot \frac{(gm_{14} + gmb_{14} + gd_{14})}{gd_{14}} \quad (5)$$

$$A_{VN} \approx -\frac{gm_6}{(gd_6 + gd_9)} \cdot \frac{(gm_{13} + gd_{13})}{gd_{13}} \quad (6)$$

$$A_{V1} = A_{VP} \cdot A_{VN} \quad (7)$$

$$gm = KP \cdot \frac{W}{L} \cdot (|V_{GS}| - |V_{th}|) \quad (8)$$

$$gd = \frac{I_d}{\left(\frac{1}{\lambda} + V_{DS}\right)} \quad (9)$$

$$gmb = gm \cdot \left(\frac{\gamma}{2\sqrt{|2\phi_f| + V_{SB}}} \right) \quad (10)$$

where: KP is the transistor transconductance, W is the transistor channel width, L is the transistor channel length, V_{th} is the threshold voltage, I_d is the transistor drain current, λ is the transistor channel-length modulation, γ is the transistor body factor and ϕ_f is the fermi potential.

The Class-AB rail-to-rail output stage is implemented by complementary transistors pairs, MP19 and MN20, by transistors, MP17 and MN18 (floating voltage source) which biasing the output transistors, and also function as a DC level shifter. It couples the input signals to the MP19 and MN20 gate terminals.

The MP21-MN24 transistors form two translinear loops with the output transistors pairs, MP19 and MN20, and the transistors pairs of the DC level shifter. The MP17 and MN18 directly control the quiescent biasing current of the output stage, according to (11) and (12). The output stage gain can be given by (13), and the circuit total gain is given by (14), where, RL is a resistive load [20, 24].

$$V_{GS19} + V_{GS17} = V_{GS23} + V_{GS21} \quad (11)$$

$$V_{GS20} + V_{GS18} = V_{GS22} + V_{GS24} \quad (12)$$

$$A_{V2} = \frac{gm_{19} + gm_{20}}{gd_{19} + gd_{20} + \frac{1}{RL}} \quad (13)$$

$$A_{VT} = A_{V1} \cdot A_{V2} \quad (14)$$

3.2 Design and Optimization

The opamp design has used a voltage supply of $\pm 1.65V$. The adopted biasing currents were the following: $20\mu A$ for the current mirror and differential input stage, resulting in a current of $10\mu A$ for each arm; $10\mu A$ to the summing circuit, MP11-MN14; $5\mu A$ for the floating current source, MP15-MN16, and DC level shifter, MP17-MN18; and $I_{dq} = 60\mu A$ to the quiescent current of the output stage transistors. The MOS transistors must be biased in the saturation region to operate as amplifiers and (15) gives the (W/L) ratio required to bias correctly the transistors in this region [25, 26].

$$(W/L) = \frac{2 \cdot I_d}{KP \cdot (V_{GS} - V_{th})^2 \cdot (1 - \lambda V_{DS})} \quad (15)$$

The V_{GS} and V_{DS} voltages of each transistor were set to operate in the saturation region, obtaining the best possible response to the opamp and the (W/L) ratios of all transistors were calculated by (15).

For the output stage, it is fixed a maximum output voltage excursion $V_{out} = \pm 1.55V$. The maximum

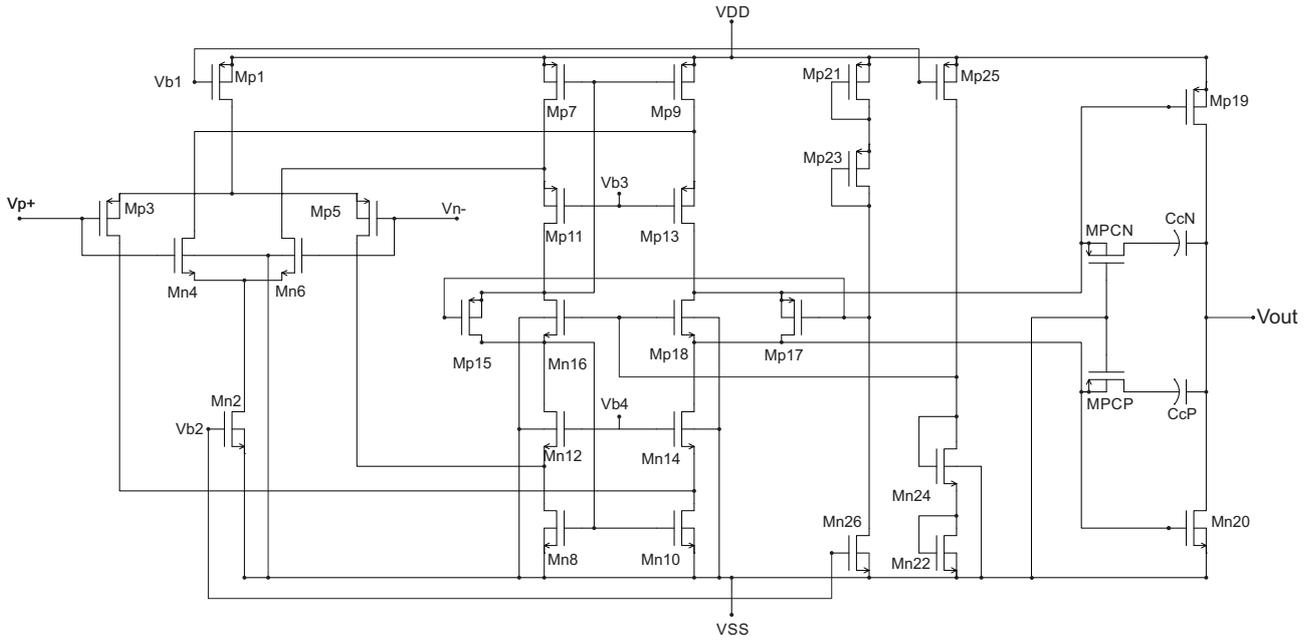


Figure 4: Full opamp schematic.

output current was calculated considering a resistive load of 500Ω connected to the circuit output, reaching a value of $I_{dmax} = (+1.65V/500\Omega) = 3.3mA$. Considering the moment of peak output voltage, the PMOS transistor MPS1 will be driving and operating in the linear region, while the MNS2 transistor will be cut. Thus, the MPS1 transistor must be biased in accordance with the equation (16).

$$I_{max} = \frac{1}{2}(W/L) (2(V_{GS} - V_{thp}) - V_{DS}) V_{DS} \tag{16}$$

Adopting a $V_{GS} = -3.3V$ and $V_{DS} = -0.1V$, the (W/L) ratio of the MP19 transistor can be found from (16). Similarly, adopting a $V_{GS} = +3.3V$ and $V_{DS} = +0.1V$, the (W/L) ratio of the MN20 transistor can also be found from (16).

The (W/L) ratios, optimized by simulations, and the main values of transistors biasing are summarized in the Table 1.

To maintain the circuit stability in the closed loop feedback, it is important an appropriate frequency compensation design. In this topology, the Miller frequency compensation is performed by two loops. The first one is formed by MPCN transistor in series with the CcN capacitor, and the second one is formed by MPCP transistor in series with the CcP capacitor. Each of the folded-cascode circuits present two main poles that can affect your open-loop gain.

In small signal analysis, the DC level shifter can be replaced by a short, and for this condition, both

frequency compensation loops operate as if they were connected in parallel. Considering that the resistors and capacitors have the same values, the two loops are equivalent to a single loop compensation provided by the capacitor Cc and resistor Rc, and the following relationships can be expressed by:

$$R_c = \frac{R_p}{2} = \frac{R_n}{2} \tag{17}$$

$$C_c = 2C_{cP} = 2C_{cN} \tag{18}$$

where: R_p and R_n represents the resistance value of the MPCP and MPCN transistors, respectively.

The positions of the two poles of the PMOS input differential pair are shown by (19) and (20). The positions of the two poles of the NMOS differential pair can be found in the analogous way.

$$W_{p1P} \approx \frac{1}{C_2 \left(\frac{1}{g_{d5} + g_{d10}} \right) \left(\frac{g_{m14} + g_{mb14} + g_{d14}}{g_{d14}} \right)} \tag{19}$$

$$W_{p2P} \approx \frac{1}{C_{1P} \left(\frac{1}{g_{m14} + g_{mb14} + g_{d14} + g_{d5} + g_{d10}} \right)} \tag{20}$$

where: C_{1P} represents the gate-source capacitance of MN14 transistor and C_2 is the output impedance of the differential pairs, multiplied by the gains of MP13 and MN14 transistors.

Table 1: Summary of opamp values.

Opamp Transistors	I_D (μA)	V_{GS} (V)	V_{DS} (V)	L (μm)	W (μm)
MP1	20	-1.00	-0.61	2	19.95
MN2	10	1.00	0.60	2	2.75
MP3	10	-1.04	-2.09	4	14.25
MN4	10	1.05	2.10	4	5.10
MP5	10	-1.04	-2.09	4	14.25
MN6	10	1.05	2.10	4	5.10
MP7	20	-1.15	-0.60	2	8.55
MN8	20	1.00	0.60	2	2.95
MP9	20	-1.15	-0.60	2	8.55
MN10	20	1.00	0.60	2	2.95
MP11	10	-0.84	-0.55	2	32.10
MN12	10	0.90	0.40	2	13.60
MP13	10	-0.84	-0.55	2	32.10
MN14	10	0.90	0.40	2	13.60
MN15	5	-0.85	-1.15	2	18.90
MN16	5	1.00	1.15	2	2.00
MP17	5	-0.85	-1.15	2	18.90
MN18	5	1.00	1.15	2	2.00
MP19	10	-1.15	-1.65	2	438
MN20	10	1.00	1.65	2	155
MP21	5	1.22	1.22	2	165
MN22	5	1.00	1.00	2	2.00
MP23	5	-0.85	-1.15	2	18.90
MN24	5	1.00	1.15	2	2.00
MP25	20	-1.00	-1.30	2	19.95
MN26	20	1.00	1.30	2	2.75
MPCN	-	-2.15	-	2	5.50
MPCP	-	-1	-	2	23.65

The insertion of the capacitor changes the poles positions and also adds a zero on the right side of the complex plane. This zero increases the gain and decreases the phase, so it can lead to instability [27]. The zero value is given by:

$$W_Z \approx \frac{1}{C_c \left(\frac{1}{gm_{19} + gm_{20}} - \frac{1}{gc} \right)} \quad (21)$$

An option to eliminate this zero is to adopt $RC = 1/(gm_{19} + gm_{20})$, in this way, moving the zero to infinity, according to (22). The circuit has adopted a compensation capacitor $C_{cN} = C_{cP} = 1pF$ ($C_c = 2pF$).

$$Rc = \frac{1}{gc} = \frac{1}{gm_{19} + gm_{20}} \quad (22)$$

The (W/L) ratios of the two compensation transistors can be calculated by (23), finding the value of $(W/L)_{MPCN} = (5.5/2)$ and $(W/L)_{MPCP} = (23.65/2)$

$$(W/L) = \frac{(1/2Rc)}{K(V_{GS} - V_{thp})} \quad (23)$$

The main parameters analyzed are the Open-Loop frequency response; Closed-Loop Bandwidth (CLB); Common Mode Rejection Ratio (CMRR); Output swing ($V_{out\pm}$) and the Input (R_{in}) and Output (R_{out}) resistances. The Figure 5 shows the opamp Open-Loop frequency response. The main results of the simulations are presented in Table 2.

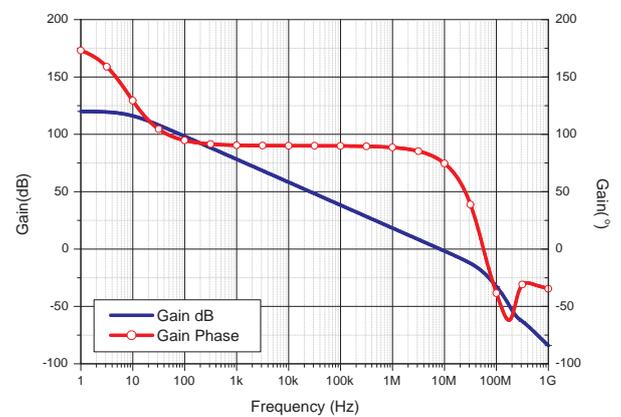


Figure 5: Opamp open-loop frequency response.

Table 2: Opamp - Simulation results

Parameters	Values
A_{vo}	119.90dB
GBW	8.10MHz
PM	77.10°
CLB(-3dB)	4.70MHz
CLB(PM)	124.60°
CMRR	131dB
$V_{out\pm}$	$\pm 1.64V$
R_{in}	1.16T Ω
R_{out}	185 Ω

In this simulation, the opamp output is connected to a resistive load in parallel with a capacitor (10k Ω and 10pF, respectively). The DC gain, A_{vo} , has presented 119.90dB. The gain bandwidth, GBW, is

8.4MHz, and the phase margin is 77.10° . These results show that the circuit has the necessary stability for a satisfactory operation.

The values of CMRR, CLB and output swing have shown satisfactory results. The impedances values are also satisfactory, with R_{in} much higher than R_{out} . In this way, the opamp has shown excellent performance, validating the circuit topology to be used in the proposed analog controller.

4 ASIC - Analog Dedicated Circuit Control

Figure 6 presents the fully integrated ASIC schematic, which is implemented by an optimized arrangement of opamps (only the capacitors are not integrated, due to the large sizes and necessity of external control compensations). For this reason, the first design approach was of the CMOS opamp. After the optimization of the opamp, the complete ASIC design can be accomplished.

In Figure 6 can be highlight seven main blocks:

- 1) Isolator input block, in which the P_{ref} and P signals are applied;
- 2) Power error calculation block;
- 3) Power error derived calculation block, where the derivative gain kd is found through its output equation (24);
- 4) Switching surface calculation (S) block;
- 5) Anti-windup circuit block;
- 6) PI controller block, where the proportional (kd) and integrator (ki) gains are found through their output equations (25) and (26), respectively;
- 7) Gain adjustment block, which provides a final gain for optimized response of the circuit.

Finally, the output circuit will provide the turn-off angle θ_{off} acting in the power control of the wind generation system.

$$V_o(t) = -kd \cdot \frac{dV_E(t)}{dt} \quad (24)$$

where: $V_o(t)$ corresponds to the output signal, kd is the derivative gain given by $(R_{der} \cdot C_{der})$, and V_E corresponds to the error signal.

$$V_o = -kp \cdot V_E \quad (25)$$

where: kp is the proportional gain given by (R_{prop1}/R_{prop2}) .

$$V_o(t) = -ki \cdot \int_0^t (V_E(t) dt) \quad (26)$$

where: ki is the integrator gain given by $(1/R_{int} \cdot C_{int})$.

5 Simulation Results

To perform the simulations and to verify the ASIC operation was used as reference model an input signal corresponding to P_{ref} , a feedback power signal, P and their output signal resultant, corresponding to the turn-off angle of the HBC switches, θ_{off} . All signals were obtained through of a mathematical model simulation, performed by Matlab/Simulink with the SimPowerSystems tool [7]. In this model, a signal P_{ref} was inserted, and the P and θ_{off} values were analyzed.

The power reference P_{ref} , which can be seen from Figure 7, has a step waveform with variations of the active power and the power factor according to the following pattern: The active power starts at 2.5 kW. In the time instant of 0.4s, the one is changed to 5 kW. Again, in the time instant of 1s, the one is changed to 2.5 kW. In the time instant of 1.5s, the one is changed to 3.75 kW. Finally, in the time instant of 2.0s, the one returns to their initial values.

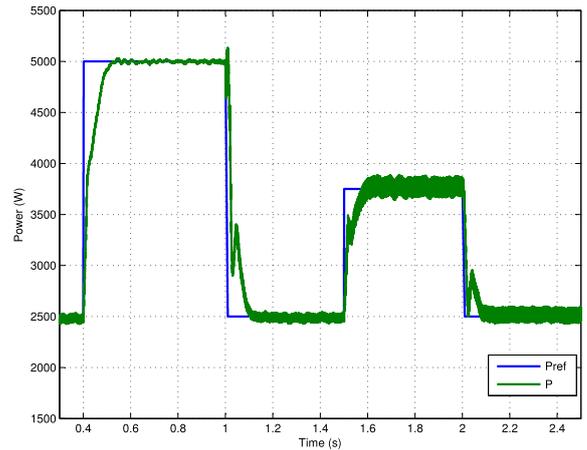


Figure 7: Reference model of the P_{ref} and P signals.

The ASIC simulation was carried out by inserting the same input signals P_{ref} and P of Figure 7 (reference model). The Figure 9 shows a comparison between the turn-off angle of the ASIC and the reference model of Figure 8. The y-axis scale of Figure 9 corresponds to 10% of the same axis of Figure 8. The analysis begins at 0.3s due to the time necessary to SRG complete its magnetization, as can be seen in Figure 7. It is possible to observe that the analog sliding mode controller implemented by Opamp developed in this work (the proposal ASIC) converged to the same θ_{off} output angle obtained in the mathematical model. In this way, the integrated circuit is totally operational and the analysis of results shows a satisfactory performance of the proposed ASIC, validating the topology. In addition, this one can be used in an SRG real plant as an alternative to programmable processors.

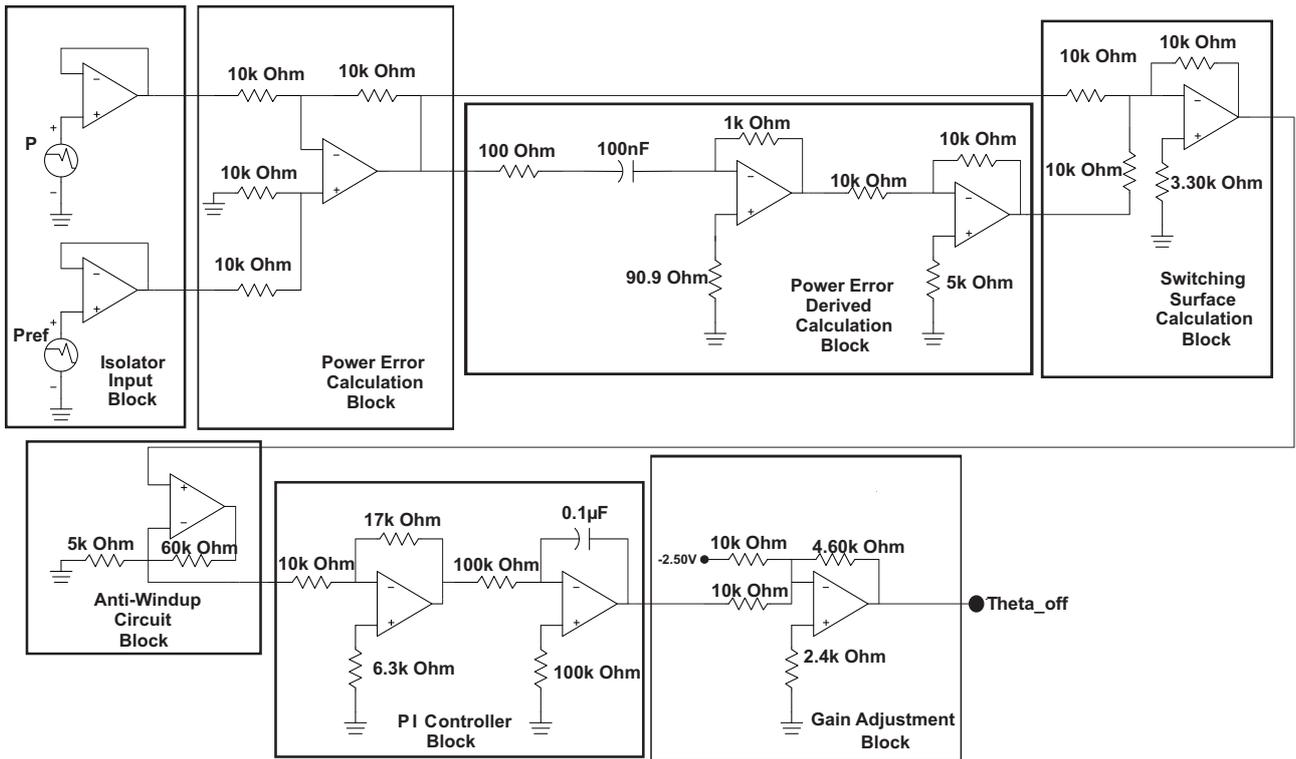


Figure 6: ASIC - Analog Slide Mode Controller.

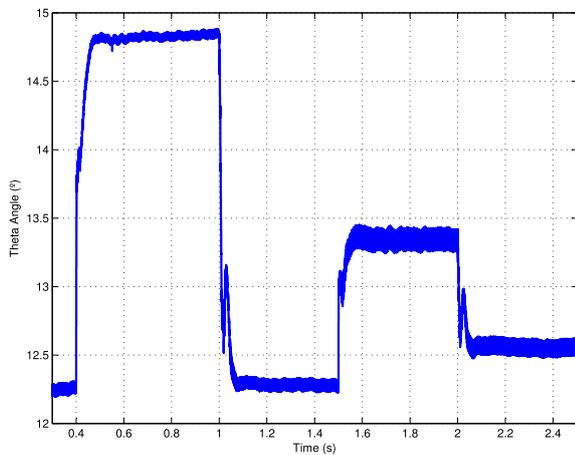


Figure 8: Reference model of the turn-off angle θ_{off} .

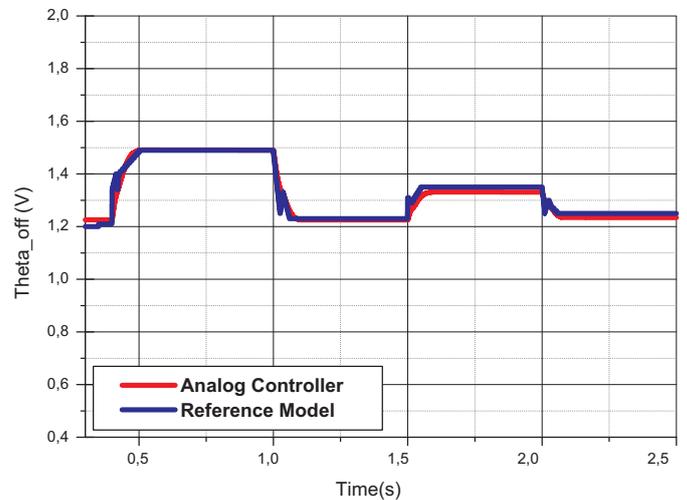


Figure 9: Comparison of the turn-off angle θ_{off} between the ASIC and the reference model.

To complete the design, Figure 10 presents the layout of the opamp (isolated) and Figure 11 presents the complete ASIC layout. To avoid offset problems in the design of the amplifier components, the match between them must be carefully done. The transistors are placed as close as possible to decrease the gradient, and then applied the common centroid configuration, which ensure that the gradient affect all transistors in the same way [8].

6 Conclusions

This paper presented a proposal of an ASIC CMOS design for sliding mode direct power control applied to SRG. Firstly, it was accomplish the design of a dedicated CMOS opamp and several simulations were performed, demonstrating excellent results. The ana-

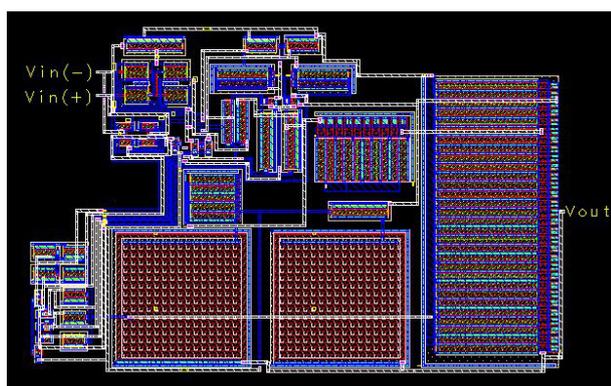


Figure 10: Opamp layout ($0.15 \times 0.11 = 0.017 \text{ mm}^2$).

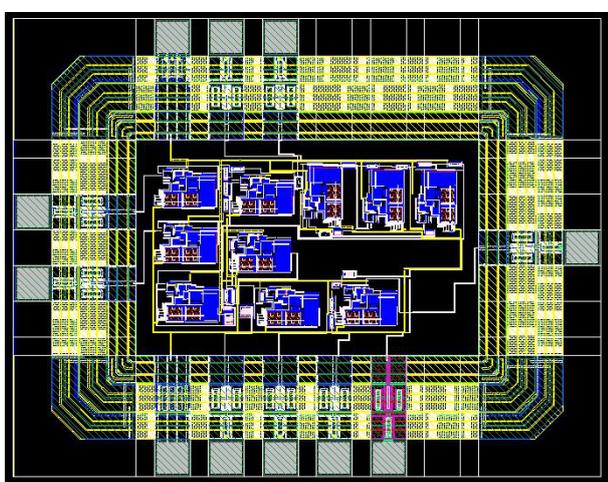


Figure 11: ASIC - Analog controller circuit layout ($1.63 \times 1.28 = 2.09 \text{ mm}^2$).

log sliding mode controller was implemented by a optimized arrangement of these CMOS operational amplifiers. Its simulation results demonstrated that the circuit ones converged at the same turn-off angle θ_{off} of the mathematical model used as the reference, confirming its effectiveness. The obtained results of the the analog sliding mode controller were extremely satisfactory, showing the feasibility of such device in $0.35\mu\text{m}$ technology. Finally, the complete layout was also proposed.

Appendix

Gains values for the analog controller circuit:
 $kd = 0.0001$ ($R_{der} = 1k\Omega$ and $C_{der} = 100nF$);
 $kp = 1.7$ ($R_{prop1} = 17k\Omega$ and $R_{prop2} = 10k\Omega$);
 $ki = 100$ ($R_{int} = 100k\Omega$ and $C_{int} = 0.1\mu F$).

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