Transient Analysis of VLSI Tree Interconnects based on Matrix Pade Type Approximation

M.KAVICHARAN, N.S.MURTHY, N.BHEEMA RAO
Department of ECE
National Institute of Technology Warangal
Andhra Pradesh-506004, India
kavicharan@nitw.ac.in, nsm@nitw.ac.in, nbr.rao@gmail.com

Abstract: - This paper presents a novel, simple and accurate delay estimation model for single interconnect and tree interconnects, which is based on new matrix Pade-type approximant (MPTA). The proposed model provides a simpler rational function approximation for estimating delay and overshoot in lossy VLSI interconnects. Computational complexity is reduced by considering rational function denominator as scalar polynomial and avoiding matrix inversion. With the reduced order lossy interconnect transfer function, finite ramp responses are obtained and line delay and signal overshoot are estimated. The estimated delay and overshoot values are compared with the existing Pade model and HSPICE W-element model. Single interconnect 50% delay results are in good agreement with those of HSPICE within 0.5% error while the overshoot error is within 1% for a 1 mm long interconnects. For global lines of length more than 1 mm in SOC (system on chip) applications, the proposed model is found to be nearly two times more accurate than existing Pade model. Tree interconnects 50% delay values are also well agreeing with HSPICE and better than existing U-transform model. Furthermore the proposed model is computationally more efficient than HSPICE, Pade model and U-transform model.

Key-Words: - Delay, matrix rational model, ramp input, RLC interconnects, transient analysis, transfer function, Distributed tree interconnect, new MPTA approximant, U-transform.

1 Introduction

Accurate estimation of delay and overshoot is crucial for the design of high speed systems in VLSI technology. As the physical dimensions scale down, interconnect delay dominates the gate delay in determining circuit performance [1]. Hence, for the design of complex circuits, simple, fast and more accurate analytic models are useful for IC designers to predict the interconnect effects.

Originally VLSI interconnects were modeled as RC lines and single pole Elmore-based models [2], [3] because of long channel device delay dominance over negligible interconnect delay. However the Elmore model fails at high frequencies since it does not consider the inductance effects [4]. It is necessary to use a second-order model, which includes the effect of inductance. Kahng et al. considered equivalent Elmore delay model based on the Resistance Inductance and Capacitance (RLC) of the interconnects [4] and [5]. Ismail et al. [6] proposed a two pole model to capture far end time domain solution for single line interconnect.

A simplified voltage transfer function obtained using Taylor series approximation for transient analysis [7], [8] has less accuracy in delay calculation. Nakhla et al. [9] use modified nodal analysis (MNA) for obtaining far end and near end responses of interconnects. Roy [10] extended [9] for obtaining more accurate far end responses of coupled RLC interconnects using delay algebraic equations.

A matrix rational-approximation model for SPICE analysis of high-speed interconnects is presented by Dounavis et al. [11], [12]. However, the approximations made to derive these models contributed to more inaccuracy. This has been improved using Pade approximation model [13] to estimate the delay of interconnects. All the above models still suffer from accuracy and computational inefficiency and need better models to efficiently estimate delay and overshoot of interconnects. Further, none of these models considered the analysis of tree structures.

In general, interconnects are in the form of tree rather than a single line. Thus, the time-domain response and delay estimation for interconnect trees are of primary importance. Initially, the Elmore delay model was developed for lumped resistor-capacitor (RC) trees [14]. Later this model was extended to include distributed models of RC trees

[15] [16] and lumped Resistor Inductor-Capacitor (RLC) trees [17]-[19]. These models provide analytical delay formulas by simplifying the sub-tree interconnect with capacitance model, which results in limited accuracy. To include transmission line effects, a numerical method based on ABCD matrix and moment matching technique was developed for distributed RLC trees [20]. All the above models need improvements for accurate delay estimations as they suffer from various inaccuracies.

A clock signal is generally derived from a common global clock source and distributed through tree interconnect networks and hence experiences delay. Unfortunately, the delay at any point on a VLSI chip cannot be estimated exactly, resulting in delay uncertainty [24]. Hence, various delay estimation models are proposed for estimation of delay of global interconnect tree structures.

The performance of a synchronous circuit is heavily dependent on the design of a clock distribution network. RLC interconnect trees are common structures in clock networks. An accurate model of an RLC interconnect tree is therefore critical in modern digital circuit design. In this paper, a more accurate analytic delay model is proposed. The concepts developed by Dounavis et al [11]-[13] for on-chip RLC interconnects are extended in the proposed model. For a given number of terms used in the transform, the MPTA requires less algebraic manipulations than the Pade and U-transform models and thus computationally less expensive. The Matrix Pade Type Approximation (MPTA) model is used to solve the Telegrapher's equations of tree interconnects for the first time. The proposed model is based on MPTA, [22] and [23] which is simple in structure and easier to implement.

The proposed algorithm is tested for both single interconnect and tree structure networks. The single interconnect estimated delay and overshoot values are compared with those of Pade model [13] and HSPICE and found to be more promising for global interconnects of length 1-5 mm. Similarly tree interconnect results are compared with those of existing model [21] and found to be more accurate than existing U-transform based model. This is due to the fact that the Pade model with rational matrix approximation has numerator and denominator matrices requiring inverse matrix operations leading to severe computational complexity. The proposed MPTA model reduces the computational complexity by considering rational function denominator as scalar polynomial and avoiding matrix inversion.

The remainder of the paper is organized as follows. Section 2 briefly describes the mathematical analysis to determine the linear transfer function of RLC interconnects and to find the time domain response. Section 3 deals with the distributed tree interconnect modeling, while section 4 presents the proposed new MPTA model. Section 5 deals with the validation of the proposed model. In this section simulation results are compared with standard HSPICE and existing models. Conclusions appear at the section 6.

2 Analysis of RLC Interconnect

The analysis of on-chip RLC interconnects begins with Telegrapher's equations in frequency domain. All the closed-form RLC interconnects models assume quasi-TEM (transverse electromagnetic) mode of signal propagation. The Telegrapher's equations are a pair of linear partial differential equations, which illustrate the voltage and current on a transmission line with distance and time as transmission line variables.

The solution of interconnects are described by telegrapher's equations as

$$\frac{\partial}{\partial x}V(d,s) = -(R+sL)I(d,s) \tag{1}$$

$$\frac{\partial}{\partial x}I(d,s) = -sCV(d,s) \tag{2}$$

where '*s*' is a Laplace-transform variable, '*d*' is a variable which represents position; *V*(*d*,*s*) and *I*(*d*,*s*) stand for the voltage and current vectors of the transmission line, respectively, in the frequency domain; and *R*, *L* and *C* are the per unit length (p.u.l.) resistance, inductance, and capacitance matrices, respectively.

The solution of (1) and (2) can be written as an exponential matrix function as

$$\begin{bmatrix} V(d,s) \\ -I(d,s) \end{bmatrix} = e^{\varphi d}\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix}$$

(3a)

Where

$$\varphi = \begin{bmatrix} 0 & -Z \\ -Y & 0 \end{bmatrix}$$

where '*d*' is the length of the transmission line, with $Z=R+sL$ and $Y=sC$. The exponential matrix of (3a) can be written in terms of cosh and sinh functions as

$$e^{\varphi d} = \begin{bmatrix} \cosh\left(d\sqrt{ZY}\right) & -Y_0^{-1}\sinh\left(d\sqrt{YZ}\right) \\ -Y_0\sinh\left(d\sqrt{YZ}\right) & \cosh\left(d\sqrt{YZ}\right) \end{bmatrix} \tag{3b}$$

where

$$Y_0 = Y(\sqrt{YZ})^{-1}$$

Equation (3a) does not have a direct representation in the time domain, so it is difficult to analytically predict the delay and overshoot of transmission lines. Hence, there is a need for approximate models. The basic idea of the matrix rational-approximation model is to use predetermined coefficients to analytically obtain rational functions for (3a). To obtain a passive model, the exponential function is approximated and the resultant model is used for obtaining time response.

A single RLC line is shown in Fig. 1. The line is driven by a 1-V finite ramp with rise times of 0.1 ns and 0.05 ns. This represents a point-to-point interconnection driven by a transistor (modeled as a resistance R_s) and connected to the next gate (modeled as a capacitance C_l).

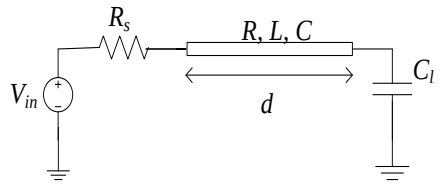

Fig.1. Circuit model of the single-line distributed RLC interconnect.

$$V_f(s) = \frac{V_{in}(s)}{(1+sR_sC_l)\cosh(\Gamma d) + \left(R_sY_0 + sC_lY_0^{-1}\right)\sinh(\Gamma d)} \quad (4)$$

where

$$\Gamma = \sqrt{YZ}$$

In (4), R_s is the source resistance at the near end, C_l is the load capacitance at the far end, and V_{in} is the input voltage. It is extremely difficult to find the time domain response of this complex transfer function, hence an approximate transfer function has been derived using new MPTA model. The time domain response of this function is used for estimation of delay and overshoot in single RLC interconnect.

3 Analysis of Tree interconnect

In this section, the proposed MPTA model is extended to analysis of tree structures. More accurate results can be obtained by increasing the order of model. The computational complexity is linear with the size of the tree and increases with the order of model.

Based on the analysis of single interconnect, the transfer functions for distributed trees can be derived from the above iterative method. The exact transfer functions are hyperbolic, exact, but very complicated. To simplify the transfer functions for distributed trees, the new MPTA method is used.

Fig. 2 shows an example of a distributed RLC tree, which is often used to analyze clock distribution networks. The driver is modelled as a resistance R_s and connected to the Node N_0. The leaf nodes (N_4 to N_6) are called leaves and connected with load buffers which can be used to drive the RLC trees in the next level. The load buffers are modelled by capacitors C_0 to C_3. All of the branches in the tree are represented by distributed RLC lines. The load capacitances of all leaf nodes are assumed to be same (100 fF).

The transfer function from N_0 to N_1 is similar to that of single interconnect as presented in last section. The transfer function of any single branch can be obtained by (4), in which replace source resistance R_s by 0 and sC_l by Z_L.

$$V_{f,1} = \frac{V_{in}}{\cosh(\Gamma d) + \left(Y_0^{-1} \big/ Z_L\right)\sinh(\Gamma d)} \quad (5)$$

The total transfer function from N_0 to N_k is the product of all of the transfer functions along the path. The transfer function between input and any node N_i of tree can be written as

$$V_{f,i}(s) = \frac{Z_{L,0}}{R_s + Z_{L,0}} \prod_i \left\{ \frac{V_{in}(s)}{\cosh(\Gamma_i d_i) + \left(Y_{0,i}^{-1} \big/ Z_{L,i}\right)\sinh(\Gamma_i d_i)} \right\} \quad (6)$$

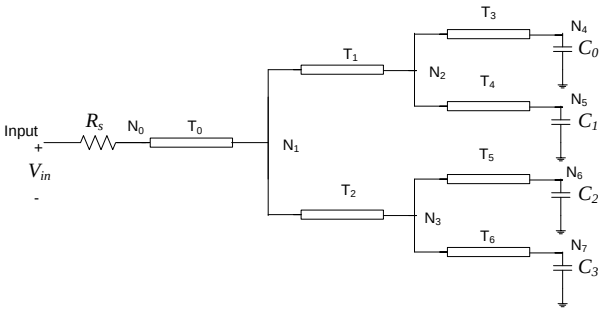

Fig. 2 General interconnect tree.

4 Proposed new MPTA model

The proposed model is based on new MPTA approximation [27], [28]. The new MPTA approximation is used for approximation of exponential matrixes. The exponential matrix can be written as power series. For the power series expansion of a function *f(x)*, where '*x*' is a complex variable

$$f(x)=C_0+C_1x+C_2x^2+\ldots+C_nx^n+\ldots, C_i=(C_i^{(uv)})\in C^{sxt}; x\in C \quad (7)$$

The exponential matrix (4) can be written as above series and the closed form rational function approximation for an exponential matrix in (4) is written as

$$R_{mn}(x)=P_{mn}(x)/\tilde{v}(x) \quad (8)$$

is called as new MPTA approximant and is denoted by order (m/n)
where

$$P_{mn}(x)=\tilde{v}(x)\sum_{i=0}^{m-n} c_i x^i + x^{m-n+1}\tilde{W}_l(x), \quad (9)$$

$$\tilde{v}(x)=x^n v(x^{-1}),$$

Let 'v' be a scalar polynomial of degree n

$$v(x)=b_0+b_1x+\ldots\ldots+b_nx^n \quad (10)$$

These coefficients b_0 to b_n can be calculated using [28].
Furthermore

$$\tilde{W}_l(x)=x^{n-1}W_l(x^{-1}),\ l=m-n+1 \quad (11)$$

$$\tilde{W}_l(x)=\sum_{l=0}^{n-1}\left(\sum_{i=0}^{l} b_{n-l+i}c_{i+m-n+1}\right)x^l \quad (12)$$

For the 2/2 approximation order, the rational approximation is

$$R_{22}(x)=P_{22}(x)/\tilde{v}(x) \quad (13)$$

where

$$P_{22}(x)=\tilde{v}(x)c_0+z\tilde{W}_l(x)$$

and

$$v(x)=b_0+b_1x+b_2x^2$$

Thus, R_{22} represents a table of rational functions, each element of which is an approximant of original series (7) and obtained from the series of below steps.

Calculation procedure for estimating delay and overshoot using new MPTA approximants are as follows.

(i) Telegrapher's equations are solved and the solution is written as exponential matrix and the derived transfer function (4) is approximated using the new MPTA model.
(ii) The coefficients W_1 of the resultant exponential function are calculated using (13).
(iii) $P_{mn}(x)$ can be calculated for any order of m/n from the relation (9). However, for validation with Pade model (2/2), the proposed model (13) is calculated with $m=n=2$
(iv) Total sums of the numerator $P_{22}(x)$ and the denominator are calculated and the approximated transfer function is obtained.
(v) Ramp response of the transfer function is obtained to estimate the delays of single interconnect and tree interconnect.

5 Simulation results

Single RLC interconnect and Tree interconnect results are presented in this section to demonstrate the validity and efficacy of the proposed model. The results obtained using MATLAB R2010a operating on HP 64-bit Intel i5 processor with clock speed of 2.53 GHz, are compared with HSPICE W-element model.

The typical interconnect parameters considered for simulation of interconnects are given in Table 1. The Pade approximation [13], U-transform based model [26] and proposed new MPTA model are implemented in MATLAB for the same set of input parameters.

Table 1: The values of Interconnects parameters [13]

V_{dd}	1 V
Length	0.1 mm to 0.5 cm
Resistance	88.29 Ω/cm
Capacitance	1.8p F/cm
Inductance	15.38 nH/cm
Input ramp rise/fall time	0.1 ns
Source resistance	50 Ω to 100 Ω
Load capacitance	50 fF to 100 fF

The far-end response to a finite ramp input of single interconnect is plotted in Fig. 3. The plots compare the responses of proposed and Pade model [13]. It is evident from Fig. 3 that, the proposed new MPTA model and Pade model [13] match very closely for the same order of 2/2. However, computational complexity of the proposed model is less than that of the Pade model, because for the same accuracy the former needs less number of poles than the latter.

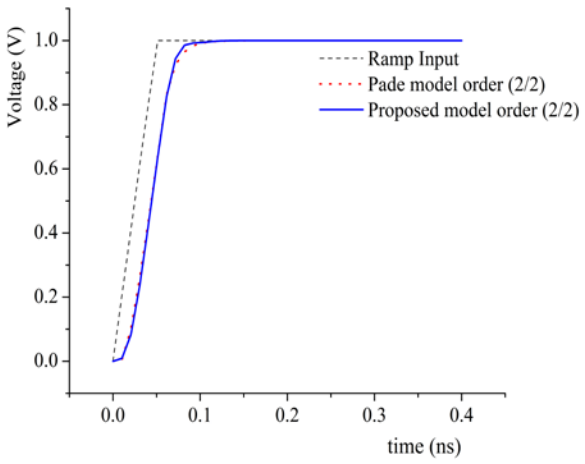

Fig. 3. Transient response of single interconnect line, with length = 0.5 mm, R_s=50 Ω, C_l=50 fF and rise time=0.05 ns.

Fig. 4 shows the results of finite ramp response for the input rise time of 0.1 ns, line length of

0.5mm, source resistance of 100 Ω and load capacitance of 100 fF. The single interconnect overshoot values using proposed model well matches with existing Pade model [13] for the same approximation order of 2/2.

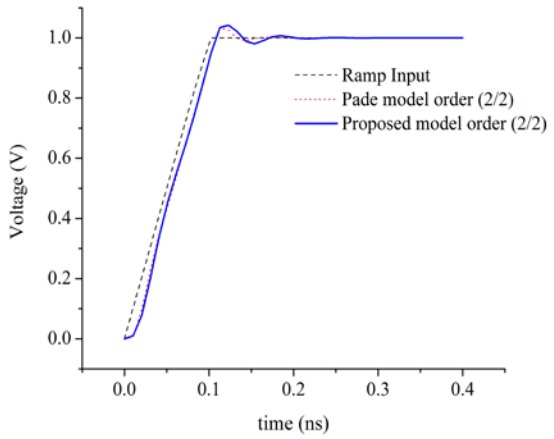

Fig. 4. Ramp response of single line when length =0.5 mm, R_s=50 Ω and C_l=50 fF and rise time=0.1 ns.

Tables 2 and 3 give the comparisons of 50% delay and overshoot values obtained using HSPICE W element model, Pade model [13] and proposed model for various lengths, source Resistances, load Capacitances and rise times. These tables include the average and maximum error percentages values of Pade model and proposed model with respect to HSPICE. From Table 2, the Pade model of order 2/2 has average and maximum error of 0.73% and 3.9%, whereas proposed model has 0.41% and 1.53% respectively.

For global interconnects (1-5 mm) the proposed model works much better than Pade model for delay and overshoot estimation. Even though, both Pade and proposed models perform similarly for smaller length (<1 mm) interconnects, but for longer lengths of 5mm, proposed model has better error percentage than existing Pade model.

From Table 3, it is observed that the Pade model [13] has maximum overshoot error of 1.05%, while the proposed model has an error of 0.96%. Overall, the average error percentages of delay and overshoot estimations are within 1% for the proposed model.

Table 2: Comparisons of single interconnect 50% delay values of HSPICE W Element, Pade model and proposed model for various lengths, source Resistances, load capacitances and input Ramp rise times.

L (mm)	R_S (Ω)	C_l (fF)	t_r (ns)	HSPICE	Pade model [13] order 2/2	Proposed Model order (2/2)
				50% delay (ps)	*50% delay (ps)*	*50% delay (ps)*
0.1	50	50	0.1	53.45	53.5	53.5
	100	100	0.05	36.45	36.5	36.5
0.5	50	50	0.1	57.33	57.5	57.6
	100	100	0.05	43.79	43.9	43.95
1	50	50	0.1	61.92	61.95	61.94
	100	100	0.05	52.94	53.1	53.05
5	50	50	0.1	135.6	136.7	136.5
	100	100	0.05	125.11	120.2	123.2
Average error % w.r.t. HSPICE					0.73	0.41
Maximum error % w.r.t. HSPICE					3.9	1.53

Table 3: Comparisons of single interconnect overshoot values of HSPICE W Element, Pade model and proposed model for various lengths, source Resistances, load capacitances and input Ramp rise times.

L (mm)	R_S (Ω)	C_l (fF)	t_r (ns)	HSPICE	Pade model [13] order 2/2	Proposed Model order (2/2)
				Overshoot (V)	*Overshoot (V)*	*Overshoot (V)*
0.1	50	50	0.1	1.004	1.005	1.005
	100	100	0.05	1	1	1
0.5	50	50	0.1	1.035	1.045	1.045
	100	100	0.05	1	1	1
1	50	50	0.1	1.071	1.081	1.075
	100	100	0.05	1	1	1
5	50	50	0.1	1.143	1.155	1.147
	100	100	0.05	1	1	1
Average error % w.r.t. HSPICE					0.378	0.209
Maximum error % w.r.t. HSPICE					1.05	0.96

The tree branches are also assumed to have same interconnect parameters [13]. The far-end responses to a finite ramp input of tree structure at nodes N_2 and N_4 are plotted in Fig. 5 and Fig. 6. The plots compare the responses of proposed, existing U-transform model and HSPICE W-element models. It is observed that, as compared to the existing U-transform model the proposed model results well match with HSPICE.

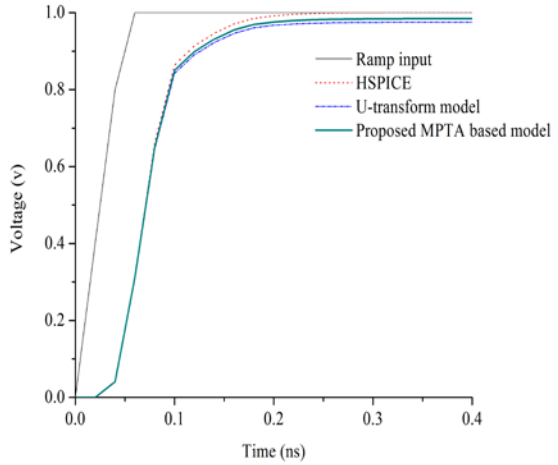

Fig. 5. Ramp response at the node N_2 of the given Tree structure with branch lengths 0.1 mm, R_s=50 Ω and C_l=50 fF.

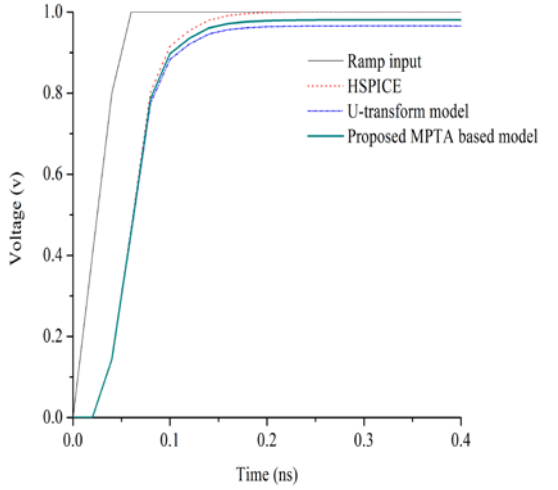

Fig. 6 Ramp response at the node N_4 of the given Tree structure with branch lengths 0.1 mm, R_s=50 Ω and C_l=50 fF.

Table 4 and 5 compares the 50% delay values obtained using existing U-transform model of order 2/2, proposed model of order (2/2) and HSPICE for various lengths, input rise times, source Resistances and load Capacitances. These values are calculated at nodes N_2 and N_4. These tables also include the percentage error values with respect to HSPICE. It is apparent that, the proposed model results are much better than existing model. The existing U transform model worst case error is 6.85%, whereas the proposed model has 4.61%. In addition, the proposed model is computationally more efficient than existing model.

Table 4. Comparisons of tree interconnect 50% delay values of HSPICE W Element, U-transform model and proposed model for various line lengths, source Resistances, load Capacitances and input rise times at node N_2.

L (mm)	R_S (Ω)	C_l (fF)	t_r (ns)	HSPICE	U-transform model order 2/2 (26)	Proposed MPTA model order (2/2)
				50% delay (ps)	*50% delay (ps)*	*50% delay (ps)*
0.1	50	50	0.1	54.4	53.02	53.25
	100	100	0.05	38.36	37.86	37.66
0.5	50	100	0.1	65.98	63.07	64.5
	100	50	0.05	48.38	50.46	49.71
1	50	50	0.1	80.17	74.79	76.64
	100	100	0.05	70.84	66.58	68.14
Average error % w.r.t. HSPICE					4.36	2.99
Maximum error % w.r.t. HSPICE					6.68	4.4

Table 5. Comparisons of tree interconnect 50% delay values of HSPICE W Element, U-transform model and proposed model for various line lengths, source Resistances, load Capacitances and input rise times at node N_4.

L (mm)	R_S (Ω)	C_l (fF)	t_r (ns)	HSPICE	U-transform model order 2/2 (26)	Proposed MPTA model order (2/2)
				50% delay (ps)	*50% delay (ps)*	*50% delay (ps)*
0.1	50	50	0.1	55.47	54.02	54.3
	100	100	0.05	40.22	39.29	39.49
0.5	50	100	0.1	75.39	72.07	73.05
	100	50	0.05	57.3	59.7	58.84
1	50	50	0.1	98.81	93.07	95.25
	100	100	0.05	88.84	83.5	85.46
Average error % w.r.t. HSPICE					4.41	3.03
Maximum error % w.r.t. HSPICE					6.85	4.61

The computational complexity of the proposed model is less as compared to U-transform based model and Pade model, because inverse matrix operation is not needed, which reduced the number of poles required from 5 to 3 at the same approximation order (2/2). As a result the CPU computation time is less as compared to existing models.

Table 6: CPU time comparison of various models and HSPICE.

Pade model [13] (ms)	U-transform based model [26]	Proposed model (ms)	HSPICE W element model (ms)
40	36	28	15

The CPU computation time to calculate the transfer functions of various models into poles and residues is provided in Table 6. The CPU time of proposed model is a onetime expense to find poles and residues for any input switching pattern, whereas HSPICE analysis is based on numerical integration that has to be performed for each input switching pattern, thus proving that the proposed model is computationally more efficient.

5 Conclusions

This paper presents a novel MPTA based closed form model for delay and overshoot estimation of high speed VLSI interconnects in DSM regime. A single line interconnect and tree interconnect have been used for validating the proposed model by comparing with the existing Pade model, U-transform and HSPICE. The delay and overshoot estimations average error percentages are within 1% for the proposed model. In SOC (system on chip) applications, for global lines of lengths 1-5 mm the proposed model is found to be more accurate than existing Pade model. The tree interconnect worst case 50% delay error percentage of the proposed model is within 5% and is much less than existing U-transform based model. In addition, the proposed model is computationally more efficient than HSPICE, Pade model and U-transform.

References:

[1] Semiconductor Industry Association, The International Technology Roadmap for Semiconductors, 1999.

[2] W.C. Elmore, The transient response of damped linear networks with particular regard to wideband amplifiers, *J. Appl. Phys.*, Vol.19, No.1, 1948, pp. 55–63.

[3] T. Sakurai, Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's, *IEEE Trans. Electron Devices*, Vol.40, No.1, 1993, pp. 118–124.

[4] A.B. Kahng, S. Muddu, An analytical delay model for RLC interconnects, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.16, No.12, 1997, pp. 1507−1514.

[5] A.B. Kahng, S. Muddu, Two-pole analysis of interconnection trees, *in 1995 Proc. of IEEE MCMC Conf.(MCMC-95)*, Santa Cruz, California, USA, 1995, pp. 105−110.

[6] Xiaopeng Ji, Long Ge, Zhiquan Wang, Analysis of on-chip distributed interconnects based on Pade expansion, *Journal of Control Theory and Applications*, Vol.7, No.1, 2009, pp. 92–96.

[7] Ren Yinglei, Mao Junfa and Li Xiaochun, Analytical delay models for RLC interconnects under ramp input, *Frontiers of Electrical and Electronic Engineering in China*, Vol.2, 2006, pp. 88-91.

[8] Y.I. Ismail, E.G. Friedman, and J.L. Neves, Equivalent Elmore delay for RLC trees, *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, Vol.19, No.1, 2000, pp. 83–97.

[9] N. Nakhla, A. Dounavis, R. Achar, M. Nakhla, DEPACT: Delay extraction based Passive Compact Transmission line Macromodeling algorithm, *IEEE Transactions on Advanced Packaging*, Vol.28, No.1, pp. 13-23, Feb 2005.

[10] S. Roy and A. Dounavis, Efficient Delay and Crosstalk Modeling of RLC Interconnects using Delay Algebraic Equations, *IEEE Transactions on Very Large Scale Integration Systems*, Vol.2, No.2, 2011, pp. 342-345,

[11] A. Dounavis, R. Achar, and L. Xin, Passive closed-form transmission-line model for general-purpose circuit simulators, *IEEE Trans. Microw. Theory Tech.*, Vol.47, No.12, 1999, pp. 2450–2459.

[12] A. Dounavis, R. Achar, and M. Nakhla, A general class of passive macromodels for lossy multiconductor transmission lines, *IEEE Trans. Microwave Theory Tech.*, Vol.49, No.10, 2001, pp. 1686–1696.

[13] S. Roy and A. Dounavis, Closed-Form Delay and Crosstalk Models for RLC On-Chip Interconnects using a Matrix Rational Approximation, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol.28, No.10, 2009, pp. 1481–1492.

[14] M. Kavicharan, N.S. Murthy and N. Bheema Rao, A Novel Delay and Overshoot Estimation model for VLSI Global Interconnects, *18th international Conference on Circuits, Systems, Communications and Computers*, Greece, Santorini Island, Greece, 2014, pp. 272-276.

[15] M. Kavicharan, N.S. Murthy and N. Bheema Rao, Efficient delay and crosstalk estimation models for current-mode high speed interconnects under ramp input, *Journal of circuits, systems, and computers*, World scientific publishers, Vol.23, No.6, pp. 1-19, July 2014.

[16] Tripati Sharma, K. G. Sharma, B. P. Singh and Neha Arora, Efficient Interconnect Design with Novel Repeater Insertion for Low Power Applications, *WSEAS Transactions on Circuits and Systems*, Vol.9, No.3, 2010, pp. 153-162.

[17] A. Mahdoum, L. Hamimed, M. Louzri, M. Saadaoui, Low-Energy-Transmission of Data on Submicron Interconnects, *WSEAS Transactions on Communications*, Vol.11, No.1, 2012, pp. 16-25.

[18] P. Chandrasekhar and Rameshwar Rao, Computationally Efficient Analytical Crosstalk Noise Model in RC Interconnects, *International Journal of Mathematical Models and Methods in Applied Sciences*, Vol.1, No.1, 2007, pp. 22-32.

[19] J. Rubinstein, P. Penfield and M.A. Horowitz, Signal delay in RC tree networks, *IEEE Transactions on Computer-Aided Design*, Vol.2, No.3, pp. 202–211, July 1983.

[20] K. Yamakoshi and M. Ino, Generalized Elmore delay expression for distributed RC tree networks, *Electronics Letter*, Vol.29, No.7, pp. 617–618, Apr. 1993.

[21] Gupta R, Tutuianu B, Pileggi LT. The Elmore Delay as a Bound for RC Trees with Generalized Input Signals, *IEEE Transactions on Computer-Aided Design*, Vol.16, No.1, 1997, pp. 95–104.

[22] Y. I. Ismail, E. G. Friedman, and J. L. Neves, Equivalent Elmore delay for RLC trees, *IEEE Transactions on Computer-Aided Design*, Vol.19, No.1, 2000, pp. 83–97.

[23] Y. I. Ismail and E. G. Friedman, Fast and accurate simulation of tree structured interconnect, *in Proceedings 43rd IEEE Circuits and Systems Mid-west Symp*., Vol.3, Aug. 2000, pp. 1130–1134.

[24] Guoqing Chen, Friedman E.G, An RLC interconnect model based on fourier analysis, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol.24, No.2, 2005, pp.170-183.

[25] X.-C. Li, J.-F. Mao, and H.-F. Huang, Accurate Analysis of Interconnect Trees with Distributed RLC Model and Moment Matching, *IEEE Transactions on Microwave Theory and Techniques*, Vol.52, No.9, 2004, pp. 2199–2206.

[26] M. Kavicharan, N.S. Murthy and N. Bheema Rao, An Efficient Distributed Tree Structure Modelling for VLSI circuits, *in Proceedings of the 2014 International Conference on Circuits, Systems, Signal Processing, Communications and Computers (CSSCC '14)*, Venice, Italy, 2014, pp. 61-65.

[27] C. Brezinski, *Pade-Type Approximation and General Orthogonal Polynomials*. Birkhäuser, Basel, 1980.

[28] C. Q. Gu, Matrix Pade-type approximant and directional matrix Pade approximant in the inner product space, *J Comput. Appl. Math*. 2004, Vol.164-165, pp. 365-385.

[29] E. G. Friedman (Ed.), *High Performance Clock DistributionNetworks*, Norwell, Massachusetts: Kluwer Academic Publishers, 1997, ISBN # 0-7923-9967-6.