A 1.8V 22mW 10 bit 165 MSPS Pipelined ADC for Video Applications

D.S.SHYLU[1*], D.JACKULINE MONI[2]

[1]Electronics & Communication Engineering, School of Electrical Sciences, Karunya University
Coimbatore, 641114, Tamil Nadu, India.Phone:09487224478.
INDIA.
e-mail: mail2shylu@yahoo.com. Fax: 0422-2615615.

[2]Electronics & Communication Engineering, School of Electrical Sciences, Karunya University
Coimbatore, 641114, Tamil Nadu, India, Phone: 09443577599.
INDIA.
e-mail: moni@karunya.edu .Fax:0422-2615615.

*Corresponding author.

Abstract:- In analog to digital converter, power consumption is considered as a major challenge to improve the performance. In this paper double sampling MDAC and amplifier sharing techniques are used to reduce power consumption for video applications.Since the requirements of high frame rate video capturing instruments and other video systems are successfully matched with that of the presented pipelined data converter, it is suitable for such applications. Use of dynamic comparators in the 1.5 bit stage architecture causes further reduction in power consumption.A 10 bit 165 MSPS Pipelined ADC which consumes 22mW of power was designed. The ADC was designed in a 0.18μm CMOS process and achieves 64 dB SFDR,56.1 dB SNDR, 9.02 ENOB and 0.25PJ/step FOM for a 1-V differential input signal and 9 MHz Input frequency from a 1 .8V supply voltage. From the results it was observed that this 10 bit Pipelined ADC was suitable for Video applications.

Key-Words:- Pipelined ADC, Low power, Video application, Dynamic Comparator, Amplifier sharing, Sample-and-Hold.

1 Introduction

In electronic industry digital audio and video have created a great need for cost-effective data converters with higher speed, low power and high resolution. The specifications required by these systems continually challenge the analog designers to improve and develop new ADC architectures. Among the various ADC architectures available the Pipeline ADCs are the best choice to use in low power high speed, medium-high resolution applications[1].Today, the low-power CMOS pipelined converter is the ADC of choice, for the video market. If the speed of the converter is increased or its supply voltage is decreased very high values of SNR will not be achievable since the gain performance of the amplifiers degrades with the increasing value of current [2].Reduction of the power dissipation looks more challenging in low-voltage analog to digital converters as there will be less room for the signal and to keep the same signal-to noise-ratio, power is to be increased. The power consumption is also increased when the operating speed is increased [3].Thus low power techniques are of great importance to achieve higher resolution, speed and supply-voltage performance with the same technology. In order to reduce the power consumption of Pipelined ADC various techniques are incorporated. One such technique is op-amp sharing technique. Since the required accuracy gradually decreases in the later stages of the pipeline architecture, the power consumption can be reduced by properly scaling the capacitor sizes, op-amp transistors sizes (W/L) and bias current, without degrading the resolution of the ADC. Sharing the op-amp between two successive stages can further reduce power consumption and has been demonstrated to achieve good performance for low power operation[4].But in op-amp sharing technique the non reset op-amp summing nodes induce a memory effect on residue signals. Bias-and-input interchanging (BII) technique is used to remove the memory effect of residue signals in pipelined ADCs [5]. But the accuracy of the ADC with BII technique is limited by the quantization error. The power consumption can be significantly reduced by partial switched op-amp technique in which the second stage of the two-stage op-amps in the SHA and subsequent pipelined stages are switched off during one of two non overlapping phases. But the number of active op-amps is more than that of switched op-

amp technique [6-8].Also the Time shifted CDS technique reduces the power consumption but has other problems such as signal dependent offset and requirement of a half rate sample and hold amplifier[9-10].According to this method when an amplifier is shared between the first and the second stages, the capacitor scaling cannot be effectively used along the ADC. Also, the additional switches introduce series resistance which, when combined with the input capacitance, degrades the settling behavior of the pipelined stage and there is no time to reset the op-amp and the previous sample affects the current input sample. To solve this problem, a modified op-amp sharing technique and double sampling technique was developed [11-12].Here two parallel sets of capacitors are used to increase the speed. Also double sampling technique was used to reduce the power dissipation and to increase the speed of conversion. In addition the stage scaling was done more effectively.

At the same time, there is a greater demand on high-speed signal processing applications such as HDTV analog front-ends and high frame rate video instruments .There are certain specifications to be met for an ADC used for video applications. The ADC must have resolution in the range of 8 to 10 bits, to avoid the distortions in the output signals and also support high frame rate operations. But for these applications the sampling rates must be greater than 100 MSPS [13].Digital crosstalk must also be considered while designing ADCs for video applications because ADCs are integrated with digital systems [14].The ADC must operate at low voltages while dissipating the least power. This requires development of ADCs which meet the characteristics of low supply voltage, low power consumption with 10 bit resolution and more than 160 MSPS sampling frequency.

The above mentioned literature reveals that the double sampling and amplifier sharing technique was not applied for video applications and also the power consumption was found to be quite higher. In this paper, a low power 10 bit pipelined ADC with a sampling frequency of 165MSPS is presented. The novelty in this paper is the integration of two low power reduction techniques suitable for video applications, and also the power consumption is reduced to 28% when compared with the conventional techniques. In addition the memory effect in the amplifier sharing MDAC is eliminated by adding additional clock-resetting phase and by using differential input pair op-amp. By properly scaling the capacitor sizes, operational amplifier transistors size (W/L) and proper design of bias current, the power consumption of the pipelined ADC is significantly reduced. Since the op-amp has the differential pair, when one input pair is being used for amplification, the other input pair is reset to common mode voltage avoiding the memory effect. As a consequence, additional switches are not required to design op-amp-sharing MDAC. With the modified op-amp sharing MDAC and the double sampling MDAC, the power consumption of the designed 10-bit Pipelined ADC is 22mW from a 1.8V supply voltage and the design is implemented in CMOS 0.18μm CMOS process. Op-amp sharing technique reduces the number of active op-amps and double sampling technique enhances the speed.

2 Architecture of 10 Bit Pipelined ADC.

Pipelined ADC exploits the concept of pipelined system in digital circuits. Each stage of the pipelined ADC consists of a sample and hold circuit, sub-ADC, DAC and operational amplifier. All the stages process the samples concurrently at any given time, and each stage performs the same function with different samples. Each pipeline stage performs an analog-to-digital conversion and passes the amplified residue to the next stage. First of all, the sample and hold circuit samples the residue from the previous stage and the sub-ADC converts the residue into a digital code. The residue is generated by converting the quantization result back to the analog (this is done by sub-DAC block) and subtracting it from the input signal. The residue formation and its precise amplification are performed by a multiplying digital-to-analog converter (MDAC)[11].Each stage operates alternately, that is, if one stage is in the sampling mode, the next stage is in the amplification mode. Thus, high resolution can be obtained at a high sampling rate. The pipeline converter is widely used for high-speed and medium-resolution applications. But, the power dissipation of a pipelined ADC is remarkably raised as its sampling rate and resolution increase. Here, two effective ways to reduce the power consumption in high speed pipelined ADCs by using two power reduction techniques known as op-amp sharing and double sampling is discussed.

The architecture for the 10-bit pipeline ADC with Double Sampling and Op-amp sharing technique suitable for video applications with 1.5-bit per stage is presented in **Fig.1**.The 0.5-bit redundancy in each stage of the 10-bit Pipelined ADC is used for digital correction to relax the comparator offset. Double Sampling technique (DS) is used in the first two stages and in the Sample-and-hold amplifier (SHA).Each of the stages has its

amplifier which is active for both the phases of non-overlapping clock pulses and hence the power is approximately halved in comparison with the conventional Pipelined ADC. Also the power consumption of the designed front-end sample-and-hold amplifier was low, which further reduces the power consumption of Pipelined ADC.

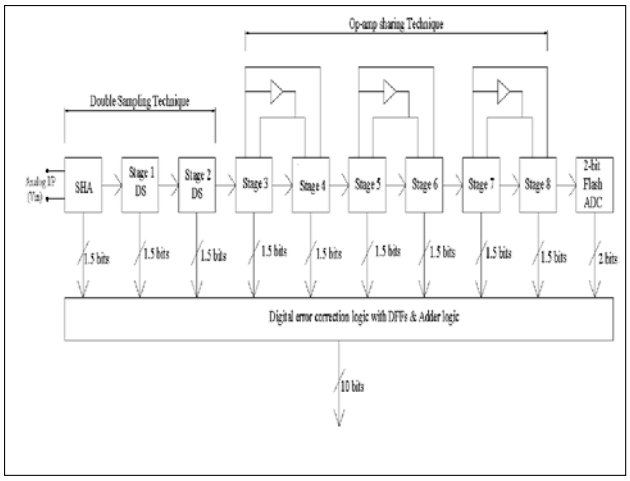

Fig.1 Architecture of the 10-bit pipelined ADC

The size of sampling capacitors used in each stage depends on the noise signals occurring in that stage and matching characteristics with the predecessing and successing stage. In the last stages of pipelined ADCs, the size of the optimum sampling capacitors will remain same for the two successive stages. Therefore, an amplifier can be shared between these two consecutive stages optimally. Because of this fact, the double sampling technique is not preferable for the last stages. Moreover, the double sampling technique uses more switches and capacitors which make this technique inefficient in terms of area. Therefore double sampling technique is used in first two stages and the op-amps are shared in the third and fourth , fifth , sixth, seventh and eighth stages. Therefore, the number of op-amps used in this designed pipelined ADC is reduced compared to that of a pipelined ADC where all the stages are using the double sampling technique. Thus the power consumption of the designed Pipeline ADC is also reduced when compared with the conventional Pipelined ADCs.

3 Description of Sub-Circuits

The designed Pipelined ADC uses double sampling technique for the front end sample and hold circuit to increase its sampling rate. This 10 bit Pipelined ADC was designed in Cadence Software using 180nm CMOS technology. The Various sub-circuits needed to realize the circuits shown in **Fig.1** are Sample-and Hold Circuit, two-stage class A/AB OTA, dynamic comparator, double sampling and op-amp sharing MDAC, sub ADC and 2-bit Flash ADC.

3.1 Double Sampling MDAC.

Double sampling is a technique used to enhance the sampling speed. Double sampling technique takes advantage of the fact that the op-amp is not active during sampling phase where the sampling capacitors play the major role. So two parallel paths are created with inverse timing which makes it possible to take advantage of the op-amp in both of two phases. Two parallel sets of capacitors are used to enhance the speed. Those are switched alternatively between the sampling and holding phase [11].Thus two parallel paths provided by the sets of capacitors introduce parallelism and enhance the speed of conversion of the Pipelined ADC. Double sampling technique not only reduces the power consumption of the amplifier due to its reduced unity-gain-bandwidth, but also makes it possible to use the optimum amplifier in each stage. **Fig.2** shows the double sampling MDAC configuration used in 1.5-bit per stage. Opposite phase clocks are used to control the two parallel paths. During the first phase capacitor CS1+, CF1+ and CS1-, CF1- are charged to the input voltage and CF2+ and CF2- are connected in feedback. CS2+ and CS2- are connected to a reference voltage generated by sub-DAC which in turn is determined by the digital output of sub-ADC. **Fig.3** shows the timing diagram of double sampling MDAC.

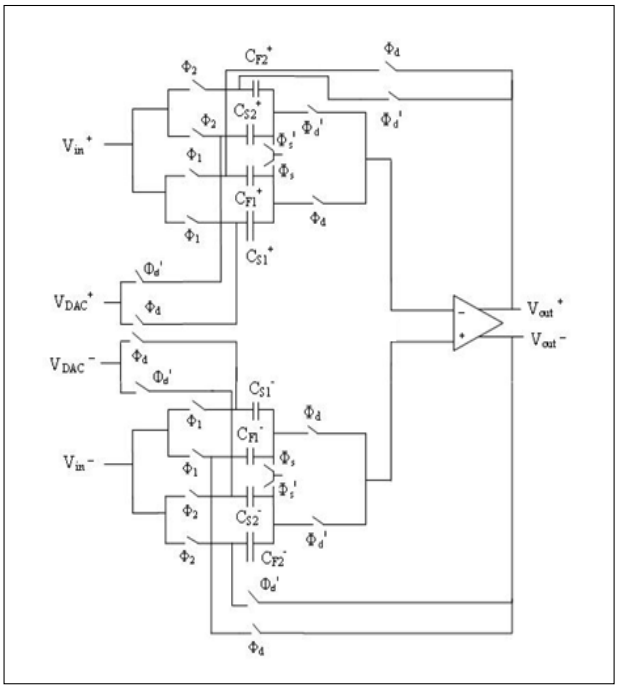

Fig.2 Circuit Diagram of the double sampling MDAC.

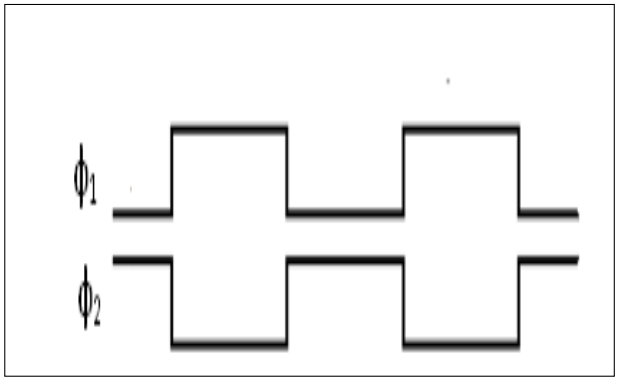

Fig. 3 Timing diagram of the double sampling MDAC.

3.2 Amplifier Sharing MDAC.

Amplifier sharing technique involves sharing the amplifiers between two successive stages along a single pipeline ADC. In the conventional op-amp sharing technique the number of amplifiers is halved, but the total power dissipation is reduced by one third, because the capacitor scaling cannot be efficiently applied to the ADC [12]. In the designed Pipelined ADC the optimum unit capacitor for stage 3 is same that of stage 4 and the same is true for stage 5 and stage 6, stage 7 and stage 8 of the pipeline ADC. Hence, an op-amp can be shared between two adjacent conversion stages. Thus the amplifiers in the last stages of the pipeline ADC are shared between two adjacent conversion stages instead of double sampled.**Fig.4** describes the amplifier sharing technique for the last stages. (stage 3 and stage 4, stage 5 and stage 6 and stage 7 and stage 8).Since the amplifier is not needed during the sampling phase, it will be active during the half clock period. Op-amp can be used for stage N when first clock is high, otherwise it can be used for stage N+1.The two sets of capacitors, C_{S13}-C_{F13} and C_{S23}-C_{F23}, sample the input signal to stage 3 in Φ_1 and Φ_2, respectively. Also these two parallel set of capacitors are used to increase the speed and these capacitors are these two parallel paths are controlled by opposite phase clock. All the switches are designed by nMOS transistors.**Fig.5** shows the timing diagram of amplifier sharing MDAC. These capacitors are connected to the amplifier in only half of the next clock phase (Φ_2 or Φ_1), which is Φ_{23} and Φ_{13}.The amplifier of stage 3 functions in Φ_3 and it can be used for stage 4 in Φ_4. The op-amp is shared between stage 3 and stage 4 in Φ_3 and Φ_4, while the input signal to stage 3 is sampled in Φ_1 and Φ_2.Simulation results show that there is significant power reduction in the amplifier sharing technique and hence it is used for video applications.

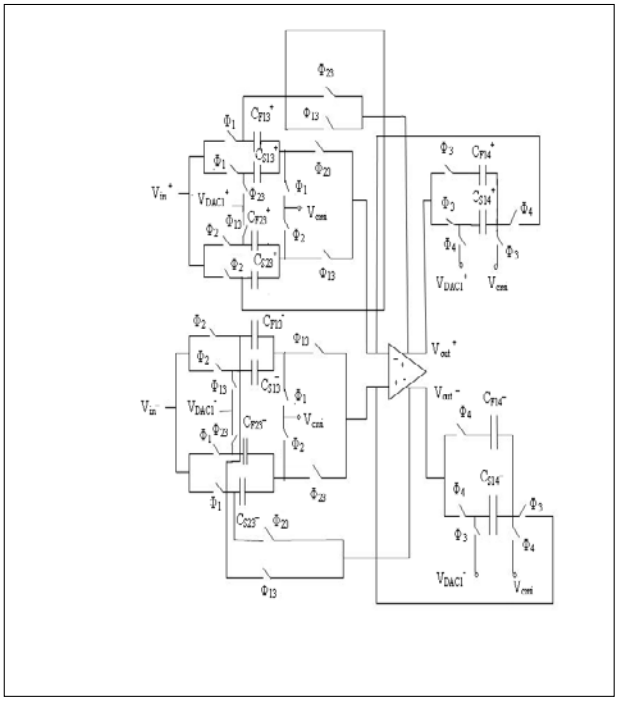

Fig. 4 Circuit Diagram of the amplifier sharing MDAC.

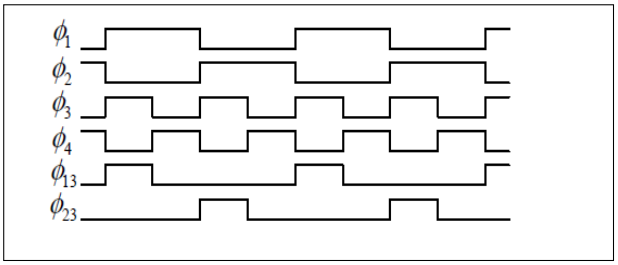

Fig.5 Timing Diagram of the amplifier sharing MDAC

3.3. SAMPLE AND HOLD CIRCUIT

In order to improve the accuracy and speed of ADC, sample and hold circuit was used. **Fig. 6** shows the circuit diagram of Sample and Hold Circuit. The sample and hold circuit operating in Φ_1 and Φ_2 uses the timing skew insensitive double sampled architecture [11].The sample & hold circuit is required to capture a wideband input signal, and drive the large load capacitance of the next stage of the pipelined ADC with low distortion. This has to be achieved without too much of noise or consuming high power. It should be able to handle inputs with various common mode ranges. The double sampling technique increases the sampling rate and also reduces the power consumption by increasing the settling time of the op-amp. Since the op-amp is the component which limits the speed and power of the sample-and-hold circuit and in this application op-amp is used

efficiently. Op-amp is shared with two parallel paths which is possible because the op-amp is needed only during one half of the clock cycle.

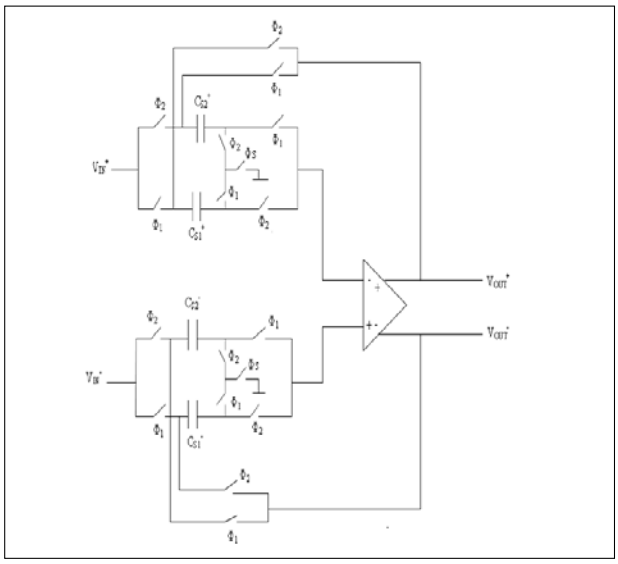

Fig. 6 Circuit diagram of Sample and Hold circuit.

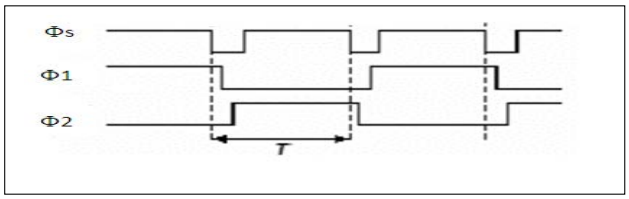

Fig.7 Timing diagram of Sample and Hold circuit.

Due to the inherent parallelism in the circuit, the Double sampling MDAC becomes more susceptible to timing skew. To overcome this problem two additional switches are required to act as multiplexer, which shares the sampling switch to the circuits. The sampling is taken by applying a short zero pulse to the sampling switch as shown in the timing diagram in **Fig.7**. Each pulse is generated with same edge of a full speed clock signal and thus any systematic error between the channels is avoided. Due to the large signal swings the MOS-switch on-resistance is a limitation on the tracking speed and the settling time. The on resistance has a nonlinear voltage dependence which produces distortion when tracking continuous time signals. These effects are very much well-defined in the input switches of the S/H.

3.4. Dynamic Comparator.

Pipelined architecture gives large correction range of offset errors of comparators and allows the use of dynamic comparators**. Fig.8** shows the circuit diagram of Dynamic comparator. **Fig.9** shows the timing diagram of Dynamic comparator. This comparator has no static power consumption. By using the clock signal clk_{2p}, which falls earlier than the signal clk_2, the sampling of reference voltage is done. When clk_{1p} goes high, the comparator's outputs are reset. When signal clk_{1p} goes low, the transistor Mc turned on, and the outputs are generated by the positive feedback of M3- M6. By using clk_{1p} as a latch clock, the comparators' outputs are generated without the settling behavior of the pipelined stage being affected.

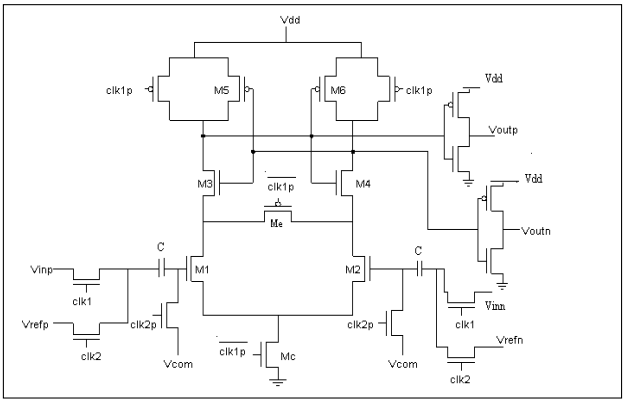

Fig.8 Circuit diagram of Dynamic Comparator.

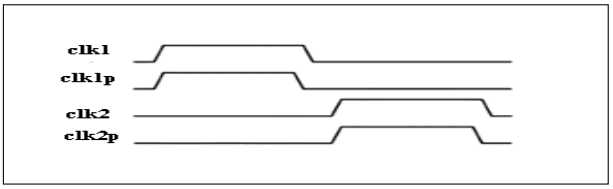

Fig. 9 Timing diagram of Dynamic Comparator.

3.5 Sub-ADC and Sub-DAC

The sub-ADC quantizes the input signal and generate the intermediate bits for each stage. For 1.5 bits per stage architecture the sub-ADC generates any one of the three binary states as its output: 00, 01and 10. The sub-ADC consists of two differential comparators with reference voltages set at +VR/4 and –VR/4 ,where +VR and –VR represent the range of the differential input signal to the comparator.The outputs of the sub-ADC are sent to a logic block which generates the controls sigmals for the sub-DAC.This logic block along with the sub-DAC will generate the three allowable binary states for the 1.5 bit per stage architecture.The architecture of the SUB-ADC and SUB-DAC is depicted in **Fig.10**.The role of the sub-DAC is to supply the residue amplifier and the gain stage with an analog voltage level that represents the quantized portion of the input signal that was fed to the 1.5 bit stage architecture. The quantized portion of the input signal is subtracted from the original input signal to create a residue voltage that will be sent to the next stage. The sub-DAC calculates the residue

voltage for that stage according to the outputs from the sub-ADC. For architecture with 1.5 bits per stage, the sub-ADC can have one of the three binary outputs: 00, 01, and 10. These correspond to the sub-DAC outputs of –VR/2, 0, +VR/2 respectively.

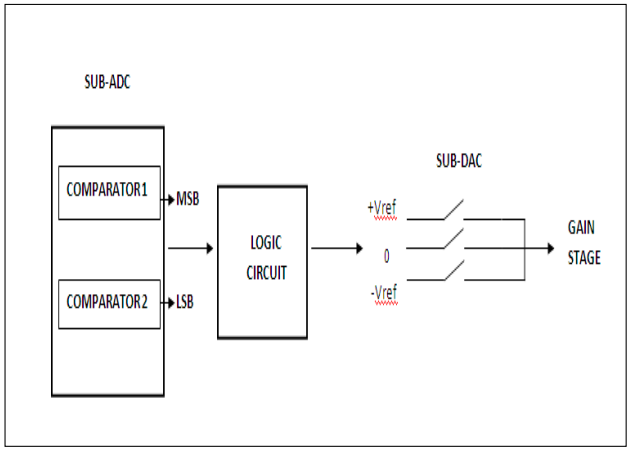

Fig. 10 The Sub-ADC and Sub-DAC

3.6. Operational Tran conductance Amplifier.

A novel cascode compensation scheme called hybrid cascode compensation has been introduced in [6, 7] by the authors. In this method, two distinct capacitors are used between two low-impedance nodes of the first stage and the output node. In turn, this compensation technique merges Ahuja [13] and improved Ahuja style [15] compensation methods. This scheme of compensation yields a higher amplifier bandwidth compared to the standard Miller and conventional cascode compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier. This technique also offers all advantages of the cascode compensation technique such as high PSRR, etc. A low-voltage and low-power two-stage class AB amplifier based on an OTA is being designed. **Fig.11** shows a two-stage class A/AB OTA composed of a folded-cascode as the first stage and the class AB amplifier with active current mirrors as the second stage that employs the hybrid cascode compensation technique. The class AB structure of the second stage reduces the OTA's power consumption and the hybrid cascode compensation enhances its speed. The first stage is a folded cascode amplifier with PMOS input transistors. The second stage is a class AB amplifier with active current mirrors. Two separate capacitors, C1 and C2, have been used for compensation of the op-amp where C1 is used in a signal path and C2 in a non-signal path. The second stage is a class AB amplifier with active current mirrors similar to [15].

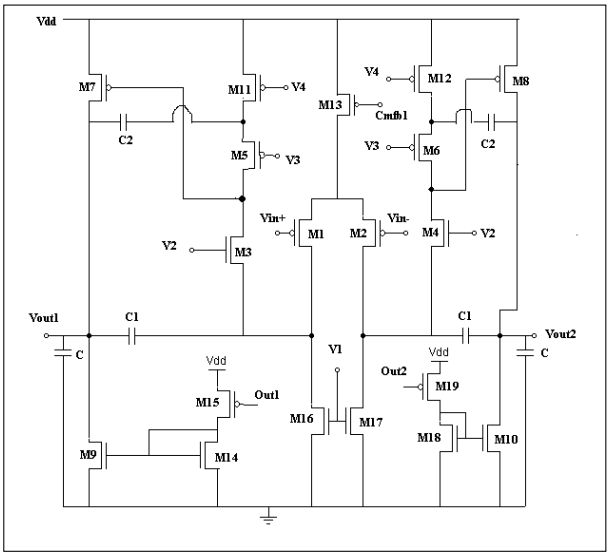

Fig. 11 The OTA used for the MDACs and sample and hold circuits.

The last stage of the pipeline ADC is a 2-bit flash ADC [15]. This 2-bit flash ADC resolves the last two bits of the ADC since the 1.5-bit stage calibration cannot be used on the final stage as this stage has no following stage.

For a supply voltage of 1.8V an initial power budget of 2.5mW was allotted, which gives total biasing current of 1666µA. This is the total current from rail to rail which should be divided into five branches. Then 600µA was distributed for differential input amplifier pair, 300µA for single side common source output stage amplifiers and 233µA for each branch of current mirror circuit. Here the targeted output differential swing was 1.8V, whereas total output swing is equal to twice of (Vdd – Vod4 –Vod5). Therefore, the total overdrive voltage,Vod4 + Vod5 <= 0.5 V. The initial assumption is to start with Vod4 = 1.35 V, Vod5 = 0.45 V after a careful analysis. Initial W/L values (in µm) can be chosen by using the current expression in saturation region operation.The initial assumption is such that $\mu_n * C_{ox} = 150\ \mu A/V^2$ and $\mu_p * C_{ox} = 60\ \mu A/V^2$ for first iteration. The saturation region current expression helps us in calculating the aspect ratios (W/L) of transistors as the current through them is known and overdrive voltage is assigned.

$$I_d = \frac{\mu n Cox}{2}\left(\frac{W}{L}\right)[Vgs - Vt]_2 \qquad (1)$$

Here I_d is the biasing current, μ_n and C_{ox} are process parameters, W/L is the aspect ratio of a transistor, V_{gs} is gate-source voltage and V_T is threshold voltage of device. The circuits were simulated in a 0.18µm CMOS technology. The OTAs were designed with load capacitances 3.5pF

for a 9MHz input signal. The body terminal of all NMOS and PMOS transistors were connected to the V_{SS} and V_{DD}, respectively. Table 1 shows the Performance Summary of the OTA.

Table 1 Performance Summary of OTA.

Input Range	1 Vpp Differential
Power Supply	1.8 V
Load Capacitor	3.5pF
Technology	0.18 µm
DC gain	43dB
Power Consumption	2.46mW
Settling Time	1µs
PSRR	58 dB
CMRR	98 dB

4 Results and Discussion.

The 10 bit Pipelined ADC was designed and implemented in 0.18µm CMOS process with a differential input signal of 1Vp-p,9MHz input frequency, and the supply voltage of 1.8V.Simulation results show that the measured power consumption of the 10-bit 165MS/s ADC is 22mW at 1.8V supply voltage.Differential non linearity (DNL) is the deviation in the width of a certain code from the value of 1LSB. DNL(k) is a vector that quantifies for each code k the deviation of this width from the "average" width (step size). DNL(k) is a measure of uniformity. Integral Non Linearity (INL) was obtained based on the deviation of the output code of a converter from the straight line drawn through zero and full-scale. The obtained differential and integral nonlinearities (DNL and INL) are illustrated in **Fig.12 &Fig.13.** The DNL is within +0.41/-1 LSB, the INL is within+ 0.6/-1 LSB at 165 MSPS. The obtained power consumption is 22mW with a 165 MSPS at 1.8 V. The obtained output fast Fourier transform (FFT) spectrum with a 9 MHz sinusoidal input at 1.8V and 165MS/s is plotted in Figure 14. The obtained the spurious free dynamic range (SFDR) is about 63 dB, the signal-to-noise-and-distortion ratio (SNDR) is about 56.10 dB, Figure of merit is 0.25 pJ/step and the effective number of bits (ENOB) is about 9.02. The obtained dynamic performance versus input frequency is shown in Figure 15 and Figure 16. Effective number of bits (ENOB) is a measure of the quality of a digitized signal. ENOB specifies the number of bits in the digitized signal above the noise floor. A figure of merit (FOM) is a quantity used to characterize the performance of a device, system or method, relative to its alternatives.

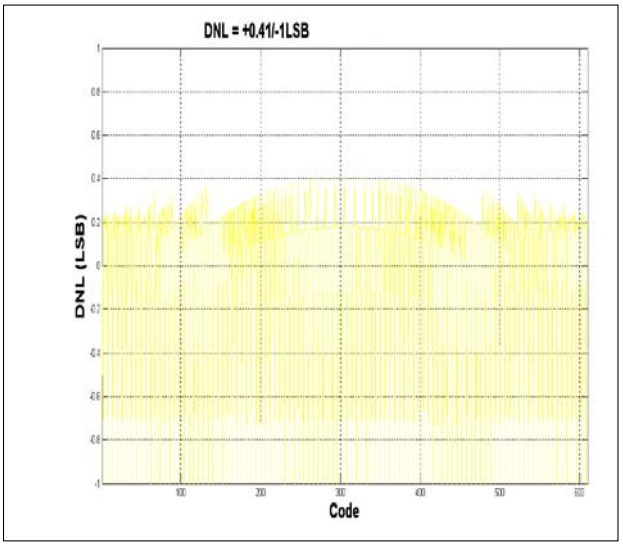

Fig.12 DNL plots. (f_s = 165 MHz, f_{in} = 9MHz)

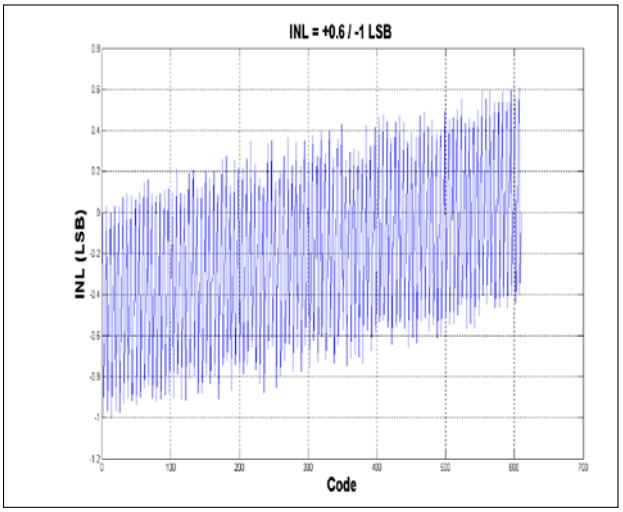

Fig. 13 INL plots. (f_s = 165 MHz, f_{in} = 2MHz)

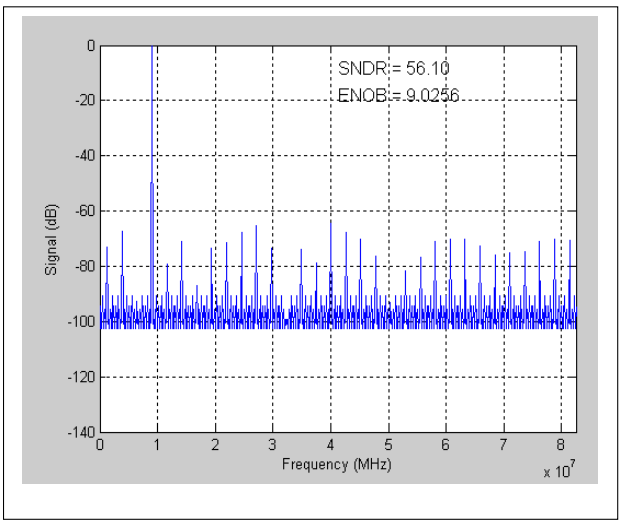

Fig. 14 FFT Spectrum of 10 bit Pipelined ADC

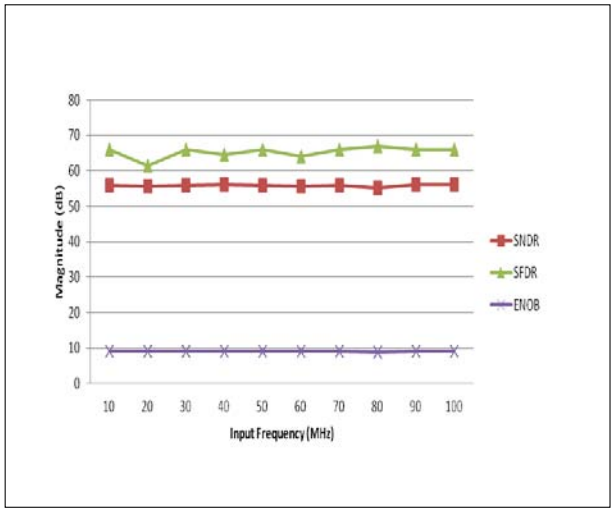

Fig. 15 Obtained SNDR, SFDR & ENOB with Input Frequency.

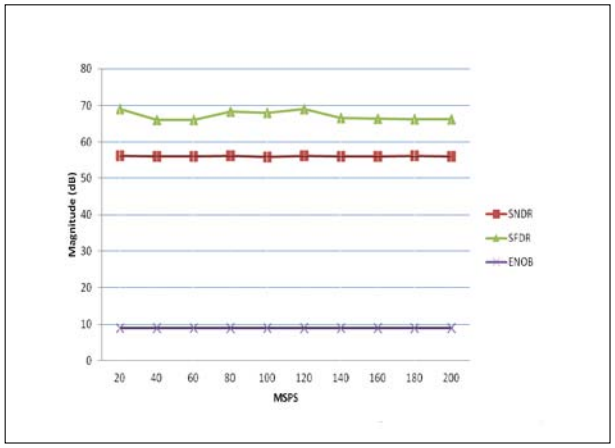

Fig. 16 Obtained SNDR, SFDR & ENOB with MSPS.

The ADC was designed in a 0.18µm CMOS process and achieves 64 dB SFDR,56.1 dB SNDR, 9.02 ENOB and 0.25PJ/step FOM for a 1-V differential input signal and 9 MHz Input frequency from a 1 .8V supply voltage. From the results it was observed that this 10 bit Pipelined ADC was suitable for Video applications.

Table 2 Performance Summary of the 10 Bit Pipelined ADC.

Power Supply	1.8 V
Input Frequency	9 MHz
Input Range	1Vpp
Power Dissipation	22mW
Sampling rate	165 MSPS
DNL	+0.41/-1 LSB
INL	0.6/-1 LSB
SFDR	64 dB
SNDR	56.1dB
FOM	0.25pJ/step
Conversion Time	10ns

Table 3 Comparison with some reported ADCs.

Ref.	**Tech. (nm)**	**V_{DD} (V)**	**Input Freq. ($_{Fin}$) (MHz)**	**Sample Freq. (MSPS)**	**Power (mW)**	**SNDR (dB)**	**SFDR (dB)**	**ENOB**	**DNL/INL**	**FOM (PJ Conv./ step)**
[1]	90	0.9	124	250	29	54.5	-	8.76	-	0.27
[4]	180	1.8	4.84	80	26	57.2	64.7	9.21	-	0.55
[8]	180	1.8	99	100	67	54	65	8.6	0.8/1.6 LSB	1.7
[5]	180	1.8	-	200	30	47.3	55.8	7.5	-0.44/+0.27LSB/ -0.44/+0.34LSB	0.82
[11]	90	0.9	9.37	200	30.9	58.5	-	9.0	-	0.22
[16]	180	1.8	50	80	36	53.2	66.7	8.5	-0.921/1.3 LSB -3.11/3.06 LSB	1.24
Current Work	180	1.8	9	165	22	56.1	64	9.02	-1/+ 0.41 LSB -1/ +0.6 LSB	0.25

4. Conclusion

This paper describes a 10 bit 165MSPS pipelined analog to digital converter for HDTV and high frame rate video instruments application. This architecture employs both double sampling and operational amplifier sharing techniques in the MDAC circuits for power reduction. The sub circuits of various stages were integrated to form the single bit stage which was then cascaded to form the 10 bit pipelined ADC. A 2 bit flash ADC which is used as the last stage of the 10 bit pipelined ADC was designed using a resistor divider branch and three clocked dynamic comparators. To correct the output of analog chain which generates 18 bits, delay elements and full adders are included, as the digital correction which generates the final 10 bit output. The INL and DNL were calculated to be -1/+ 0.41 LSB and -1/+0.6 LSB. Positive value of DNL shows the ADC to be monotonic and an SNDR of 56.1dB shows that it is noise resistant. Simulation results show that this Pipelined ADC achieves a 64 dB SFDR and 0.25pJ/step FOM for a 1V $9MH_z$ differential input signal. Since this ADC achieves a very good FOM and conversion time this ADC is very suitable for high performance video applications.

ACKNOWLEDGEMENT

The authors are grateful to the management of Karunya University and VLSI Centre of Excellence of the School of Electrical Sciences, ECE Department, and Karunya University for facilitating this research work. The authors would like to thank Ms.Neetha C.John for her help in working with the software tool.

References:

[1] Mohammad Reza Ashraf, Mohammad Javari, A 10-bit 250MS/s Pipelined ADC With a Merged S/H & 1st Stage Using an Optimal Op-amp Sharing Technique, 19th Iranian Conference on Electrical Engineering (ICEE), Tehran , 17-19 May 2011,pp.1-5.

[2]RezaLotfi,MohammadTaherzadeh-Sani,M.Yaser Azizi,Omid Shoaei, Low-power design techniques for low –voltage fast settling operational amplifiers inswitched-capacitor applications, INTEGRATION ,the VLSI Journal,36,2003,pp.175-189.

[3] Reza Latfi, Mohammad Taherzadeh-Sani, Omid Shoaei, Power Consumption Issues in High-Speed High-Resolution Pipelined A/D Converters, IEEE International Symposium on Circuits and Systems, 5,Japan, 23-26 May 2005, pp.4618 – 4621.

[4]Naga Sasidhar, Youn-Jae Kook, Seiji Takeuchi, Koichi,Hamashita, Kaoru Takasuka, Pavan Kumar Hanumolu, Un-Ku Moon, A Low Power Pipelined ADC Using Capacitor and Op-amp Sharing Technique With a Scheme to Cancel the Effect of Signal Dependent Kickback, IEEE J. Solid-State Circuits, 44,(2009) (9), pp.2392 – 2401.

[5] Chun-Hsien Kuo, Tai-Haur Kuo, and Kow-Liang Wen., Bias-and-Input Interchanging Technique for Cyclic/Pipelined ADCs with Op-amp Sharing, IEEE transactions on circuits and systems, 57(3),2010,pp.168- 172.

[6] C. Kim, D.-K. Jeong, and W. Kim,A partially switched-op-amp technique for high- speed low-power pipelined analog-to-digital converters, IEEE Trans. Circuits Syst. I, Reg. Papers, 53(4), 2006,pp. 795–801.

[7] Hwi-Cheol Kim, Deog-Kyoon Jeong, A Partially Switched-Opamp Technique for High-Speed Low-Power Pipelined Analog-to-Digital Converters,IEEE Transactions on Circuits and Systems—I: Regular Papers, 53(4),2006,pp.795-780.

[8]M. Waltari, K. A. I. Halone,1-V 9-bit pipelined switched-op-amp ADC, IEEE J.Solid-State Circuits, 36(1) ,2001,pp.129–134.

[9]J. Li, U. K. Moon,A 1.8 V 67 mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS Technique,IEEEJ.Solid-StateCircuits, 39(9),2004,pp.1468–1476.

[10]Liviu Chiaburu, Svante Signell,A Method To Reduce Power Consumption In Pipelined A/D Converters ,Proceedings of the 2003 International Symposium on Circuits and Systems. ISCAS '03, Bangkok, Thailand, (1)25-28 May 2003,pp. I-845 - I-848.

[11] S. Haider et al.,A 160MSPS 8-bit pipeline based ADC, in Proc. 18th International Conf. on VLSI Design, Kolkata, India, 3-7 Jan. 2005, pp.313-318.

[12]Sahel Abdinia, Mohammad Yavari, A New Architecture for Low-Power High-Speed Pipelined ADCs Using Double-Sampling and Opamp-Sharing Techniques, Proceedings of 16th IEEE International Conference on Electronics, Circuits, and Systems, Yasmine Hammamet, Canada, 13-16 Dec. 2009 ,pp.395 – 398.

[13] Cheng-Ta Chiang, Yu-Chung Huang,A 10-bit Pipelined ADC for High Frame-Rate Video/Image Capturing Instruments and System,Proceedings of IEEE Symposium on Industrial Electronics and Applications,(2), Kuala Lumpur, 4-6 Oct. 2009,pp.881-884.

[14] Martin Trojer, Mauro Cleris, A 1.2V 56mW 10 bit 165Ms/s Pipeline-ADC for HDVideo Applications, 34th European Solid-State Circuits

Conference, Edinburgh, 15-19 Sept. 2008,pp,270-273.

[15]K. A. Shehata ,H. F. Ragai , H. Husien, Design And Implementation of A High Speed Low Power 4-Bit Flash ADC, International Conference on IEEE Design & Technology of Integrated Systems in Nanoscale Era, DTIS. , Rabat,2-5 Sept. 2007, pp. 200 – 203.