A 12-bit CMOS Dual-ladder Resistor String D/A Converter Integrated with Self-adjusted Reference Circuit

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Abstract: This paper presents a 12 bit dual-ladder resistor string digital to analog converter (DAC) with the power supply of ±5V which adopts a self-adjusted reference circuit and a class-AB output buffer. A self-adjusted reference circuit is used to provide differential reference voltages for obtaining better accuracy and symmetry. The DAC reuses the resistors of the differential reference voltages circuit as the dual-ladder resistor string, which saves a considerable chip area. Class-AB output stage is employed to reduce the setup time and enhance the load-driving capability. The 12 bit DAC is fabricated in a standard 0.5μm CMOS process. The measured results show that the integral non-linearity (INL) and differential non-linearity (DNL) are less than 2 LSB and 0.25 LSB, respectively. The proposed DAC features the characteristics of high precision, good monotonicity and excellent symmetry.

Key-Words: digital-to-analog converter; DAC; dual-ladder; class-AB; INL; DNL; self-adjusted reference circuit.

1 Introduction

The DAC is used to generate a steady voltage to cancel the effect of gravity for a MEMS accelerator, which is equivalent to two 200 pF dynamic capacitances. A DAC with high resolution, low DNL and excellent symmetry is preferable for the MEMS accelerator, and it plays an important role in the MEMS accelerator system. One of the most basic DAC architectures is the resistor string DAC, typically suitable for mid-accuracy applications [1-2]. They are of special importance in processes with no high-quality capacitors available. The obvious advantages are monotonicity, simple design and no need of active circuitry [3]. The simplest resistor-string AC architecture is the traditional resistor string DAC as shown in Fig.1. This kind of architecture needs 2^N resistors and switches for N-bit resolution DAC. However, as the resolution increasing, the chip requires a large area due to the need of a large number of passive components, and the accuracy is obviously related to the matching among unit resistors [4]. And the static performances of resistor string DAC also depend on the unit resistors matching in the array [5]. The unit resistors are exactly the same in the ideal resistor array. But in reality, the process mismatch of resistor will introduce random errors, the chip internal temperature, and the unevenness of film thickness will result in systematic errors [6].What's more, it's very difficult to get better matching for layout because of the larger area. So the general resistor string DAC is limited in practice to implement no more than an 8 bit of accuracy.

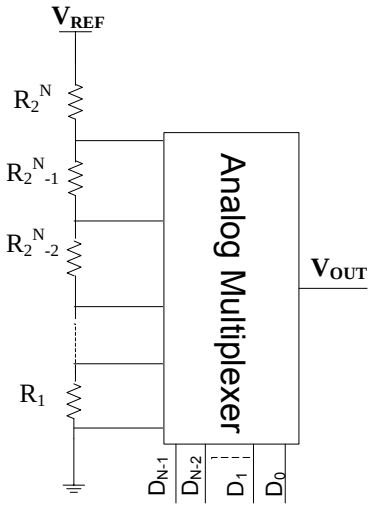


Fig.1 The traditional resistor string DAC

In order to improve the accuracy of the DAC, a dual 12 bit current-steering DAC is presented in paper [7]. In this architecture, the seven most significant bits (MSBs) are thermometer encoded with unary current sources and the five least significant bits (LSBs) converted using binary-

weighted current sources. It needs to get the best matching between 4096 current sources in the layout so that it will take larger area than the traditional architecture. And the monotonicity and DNL of this architecture is worse than the resistor string DAC.

This paper introduces the 12 bit dual-ladder resistor string DAC with self-adjusted reference circuit which significantly improves the precision and symmetry than the traditional resistor string DAC; it has better monotonicity, linearity and smaller area than the current-steering DAC. In section 2, the architecture and principles of the designed DAC are described. The self-adjusted reference circuit and the output buffer are detailed. The simulation and measured results are given in section 3. And four different DAC architectures are compared. Finally, a brief summary concludes our discussion in the last section.

2 Design Considerations

2.1 DAC Architecture

The architecture of the proposed DAC with self-adjusted reference is depicted in Fig.2. The architecture mainly consists of four blocks including a self-adjusted reference circuit, a dual-ladder resistor string block, 6-64 decoding circuits for MSBs and LSBs and an output buffer. The dual-ladder structure is adopted to overcome the issue of layout matching and improve the accuracy. And in order to get symmetrical differential reference voltages Vrefp and Vrefn, a self-adjusted reference circuit is applied. As the DAC will drive the MEMS accelerator, which equivalents to two 200pF dynamic capacitance loads an output buffer with class AB output stage is used to enhance the capability of load driving and stabilize the DAC's output signal in 300 milliseconds.

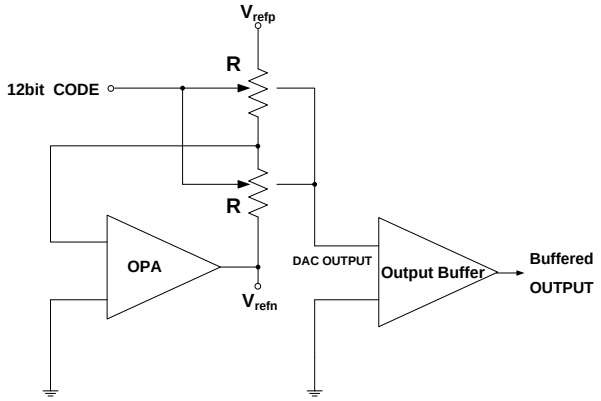


Fig.2 Block diagram of the proposed DAC

The dual-ladder structure is illustrated in Fig.3. Every LSB ladder step includes an LSB resistor and a switch. The resistor string is divided into two parts: 6 bit coarse array and 6 bit fine array. As long as MSBs and the LSBs reach to 6 bit, the DAC will satisfy the target of 12 bit. The resistance R1, "fine" ladder array is intermeshed (paralleled across) each coarse resistor section, each of the 64 fine ladder sections is tapped at 63 nodes. The greater resistance of the unit resistor will get the better matching characteristics. In this way, getting better accuracy and reducing the difficulty of layout are taken for granted. So several advantages accrue with this architecture, separate but intermeshed ladders simplify layout, minimize parasitism, allow optimum impedance levels to both sections, and assure monotonicity since the two ladders are common at all MSB/LSB splicing nodes[8]. The dual-ladder structure is consisted of 4160 resistors and takes over a considerable chip size. Luckily, the resistors of the self-adjusted reference circuit, which will illustrate in the next section, can be reused as the dual-ladder resistors string.

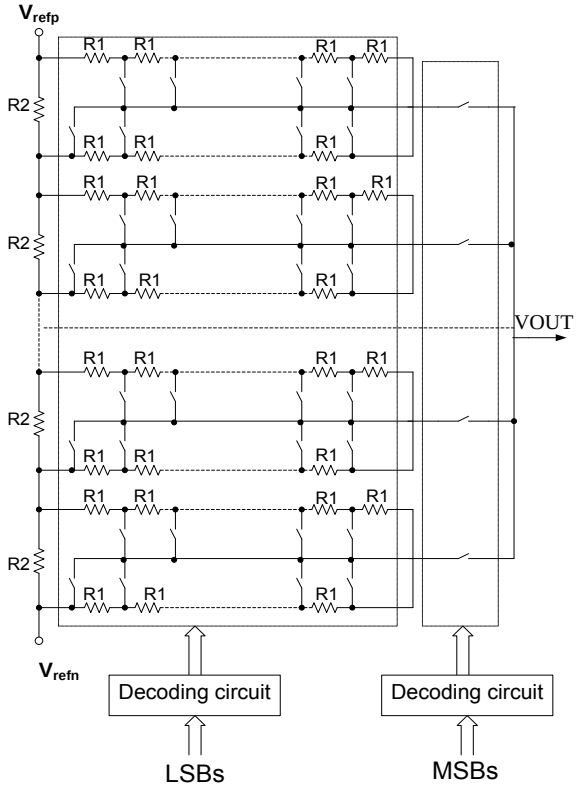


Fig.3 Circuit of the dual-ladder structure

Firstly, the voltage (Vrefp-Vrefn) is equally divided into 64 portions by the coarse resistor array R2. The 6-64 decoding output controls the switches using a binary code. Basing on the coarse dividing, the voltage (Vrefp-Vrefn)/64 is divided into 64 equal portions by the fine resistor array R1. Then the voltage (Vrefp-Vrefn) is equally divided into 4096 portions. Vrefp and Vrefn are generated from the self-adjusted reference circuit. Finally, the DAC

is binary coded such that the decimal equivalent K, of an N bits digital code produces an output voltage given by:

$$V_{OUT} = \frac{K \times (V_{refp} - V_{refn})}{2^N} - V_{refn} \quad (1)$$

Because of the existence of parasitic capacitance, the RC time constant of the capacitor charging and discharging will be increased with the increasing the unit resistance. Meanwhile, the power consumption must be as low as possible. For these considerations, the coarse resistor array consists of 64 24.37K Ohm unit resistors R2, the fine resistor array includes a matrix of 64×64 14.89K Ohm unit resistors R1.

2.2 Self-adjusted reference circuit

Reference circuit is needed to supply differential reference voltages Vrefp and Vrefn. The traditional voltage references circuit is shown in Fig.4. From the architecture, we can know the voltages equations are (2) and (3).

$$Vrefp = (Vbg - VSS)(1 + \frac{R1}{R2 + R3}) + VSS \quad (2)$$

$$Vrefn = (Vbg - VSS)\frac{R3}{R2 + R3} + VSS \quad (3)$$

According to the formula (2) and (3), the Vrefp and Vrefn can be obtained with the suitable R1, R2 and R3. There are two shortcomings using the conventional structure to generate differential reference voltages [9]. Firstly, the generated differential reference voltages are not accurate enough because of the mismatch of actual devices in the process, and the systematic offset in the design. Secondly, systematic mismatch in this structure would result in asymmetry of the two voltages. That is to say, as soon as the voltage Vbg changes, the Vrefp and Vrefn will change with different amplitude, respectively. This will degrade the performance of the DAC system.

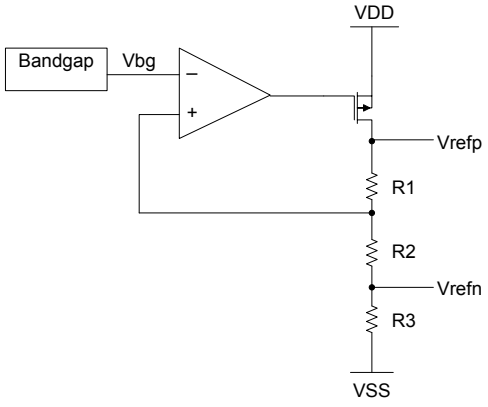


Fig.4 Traditional voltage references circuit

In order to overcome the above shortcomings, a self-adjusted reference circuit is presented in Fig.5. It's mainly composed of a bandgap, a buffer, an Opamp with feedback resistors. The Vbg which is generated by the bandgap circuit is buffered to Vrefp, 3.7V, and then Vrefn is generated by the feedback so that Vrefp and Vrefn are correlated. The main advantage of the solution is that, exploiting the ground as a reference voltage could help improving the symmetry. Ignoring the mismatch of resistors, as the voltage Vrefp changes, Vrefn will change in the opposite direction with the same amplitude. When Vrefp changes ΔV, Vrefn will change -ΔV. The structure can provide completely symmetrical differential reference voltages Vrefn = -Vrefp. The resistors mismatch can be neglected when the resistors R is in large size. As mentioned above, the large size resistor will be reused as the dual ladder resistor string. What's more, the high feedback resistance won't attenuate the loop gain of the OPA, which can help to decrease the offset of the OPA and improve symmetry. Considering saving area, the feedback resistors (R) is reused as the ladder string resistors.

The simulation result of the self-adjusted reference circuit is given in Fig.6. Vbg is 1.329V, Vrefp and Vrefn is completely symmetrical valued 3.697V and -3.697V through simulation.

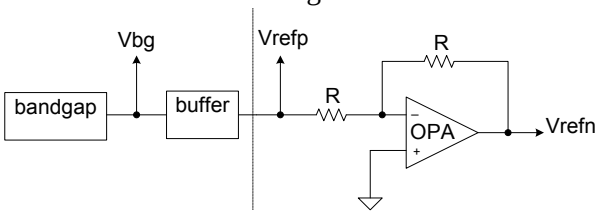


Fig.5 Self-adjusted reference circuit

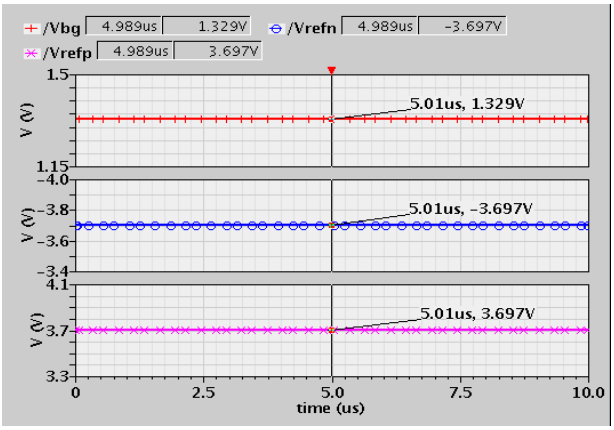


Fig.6 Simulation results of self-adjusted reference circuit

2.3 Output buffer

The MEMS accelerator equivalents to two dynamic 200pF capacitances and consumes a large amount of charge during every signal readout period. The DAC output buffer with a low-pass filter (LPF) is

implemented in order to supplement the large amount of charge consumed by the MEMS accelerator and keep the DAC output voltage stable. The LPF is consisted of a small resistor (160 Ohm) and a large capacitor (330μF). The output signal swing of DAC is -3.7V to +3.7V. The settling time of the DAC without output buffer is about 2.56s. In order to decrease the settling time of the output voltage and confine it within 300ms, the two stage operational amplifier with class-AB output stage is shown in Fig.7. The first stage is a folded cascade topology for large gain. And the second stage uses class-AB output to provide large transient current so that the output can be stable rapidly.

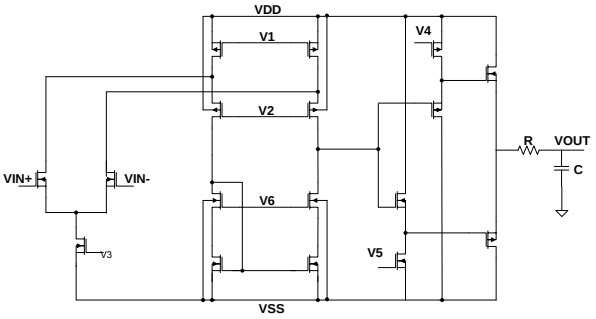


Fig.7 Output buffer's schematic

The output stage should satisfy three conditions as below [10]. First, when driving large load, the output stage has minimum static current and the majority of the output current will flow into the load. That is to say, the ratio of the maximum current I_{MAX} and the static current I_q must be large to improve the efficiency of the output stage. Second, the minimum current of output stage cannot be far less than static current so as to avoiding the high-frequency distortion. Lastly, in order to avoid the low-frequency distortion, it should have a smooth AB transient characteristic.

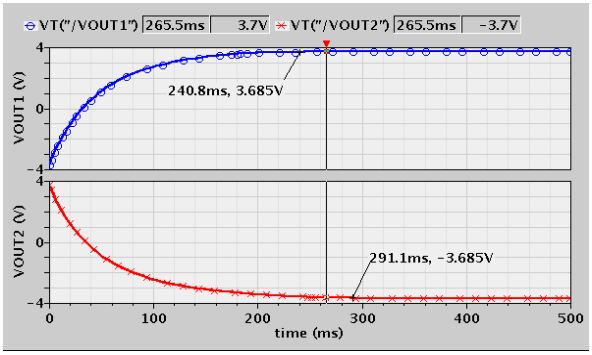


Fig.8 The output waveform of settling time

The simulation result of settling time is plotted in Fig.8. The settling time is 240.8ms and 291.1ms, when the output of DAC rising from -3.7V to 3.7V and falling from 3.7V to -3.7V, respectively, which are much less than 2.56s. So the settling time of DAC is reduced significantly with the class-AB output buffer. Because of the low static current, the static power is very low by using this architecture.

3. Simulation and Measured Results

3.1 Simulation results

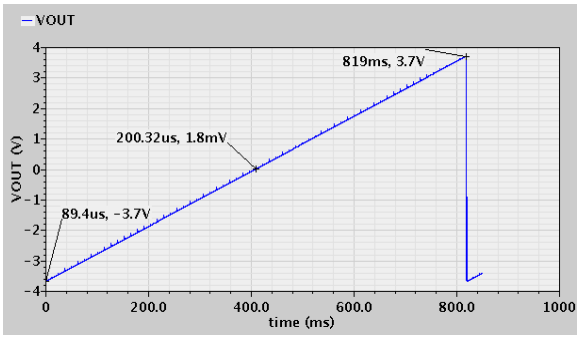


Fig.9 Output waveform when sampling period is 100ns and the details

The output simulation result is shown in Fig.9. It shows the simulated output and the details when the sampling period is 100ns. The simulated LSB step is close to the calculated LSB step, which is 1.8mV. The minimum and the maximum voltage are -3.7V and 3.7V, respectively. It indicates that the Vrefn is absolutely symmetric with Vrefp.

3.2 Measured results

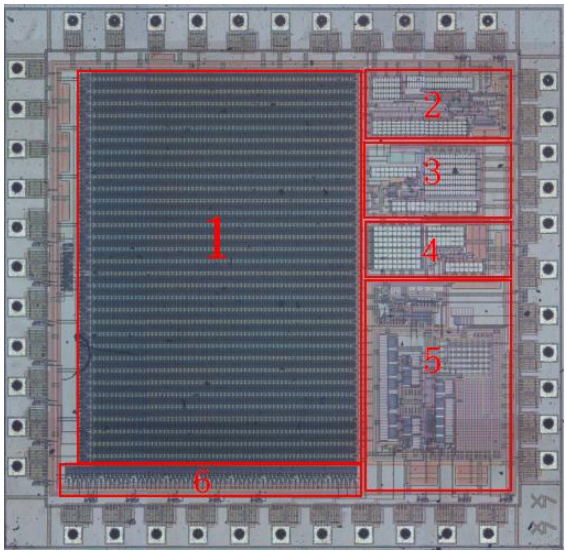
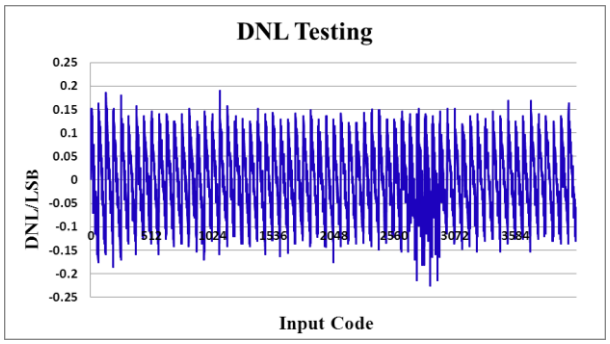


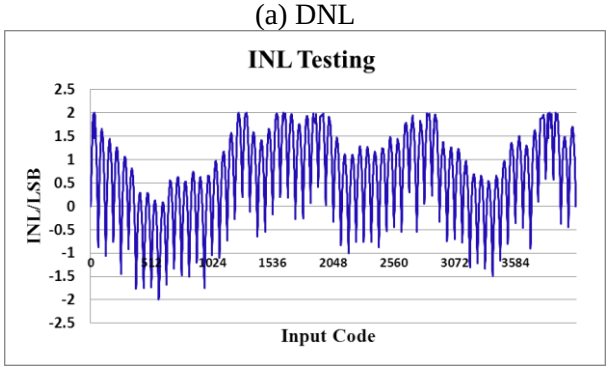
Fig.10 Chip micrograph (1. resistor string array and switches; 2. output buffer; 3.buffer_BG; 4.OPA; 5.bandgap; 6.decoding circuit)

The proposed 12 bit dual-ladder resistor string DAC has been fabricated in a MXIC 0.5μm CMOS process, and the whole chip micrograph is shown in Fig.10. The resistor string array and switches are shown on the left side with the 6-64 decoding circuit right below. The output buffer, buffer_BG, OPA of the self-adjusted reference circuit and the bandgap

are shown from top to bottom on the right side of the micrograph. The package of the chip adopts CLCC48.



(a) DNL



(b) INL

Fig.11 Measured results of both DNL and INL

The measured result of differential non-linear (DNL) is below 0.25 LSB, as depicted in Fig.11 (a). The integral non-linear (INL) is below 2 LSB, as depicted in Fig.11 (b), respectively. The good DNL performance exactly proves the use of difference buffer in the dual ladder DAC structural works well. For further saving the chip size, the unit resistor of the fine ladder is rather small. And this affects the matching performance of the local unit resistors, which slight affect INL performance. However, the testing INL performance meets the MEMS accelerator's requirement. The simulation results of INL and DNL are nearly 0LSB. However, the mismatch of resistors and MOSFET, the matching errors of the layout and the process, and the variation of processing parameters make the main difference between the simulation and measured results. The noise of the MOSFETs and resistors, the random noise of other devices also makes the test result worse than the simulation result. What's more, in the 12 bit DAC test system, the error caused by the background noise is considerable. The measured results meet 12-bit DAC requirements that are guaranteed to be monotonic and have high precision.

With the help of the multimeter, the port of Vrefn is measured -3.7V when Vrefp is set at 3.7V. It shows that the generated Vrefn is absolutely symmetric with Vrefp, which is accord with the theory of self-adjusted reference circuit.

Table 1 summarizes the performance comparison of the proposed DAC with those of the other DACs published previously [3, 7, 9]. It shows that the resolution is higher than the previously [3, 9]. The DNL of the proposed DAC is the best of all the works previously [3, 7, 9]. It shows that the dual ladder resistor string DAC has better DNL performance than the Dual current-steering and Resistive DAC structure and resistor Capacitive DAC structure as [7] and [9] referred to. As described in [3], the small area of MSB resistors deteriorate the INL performance , and it can also affected DNL performance .The INL performance is not so good as [3] and [9], as mentioned above, the use of small fine ladder unit resistor deteriorate the matching performance of the local unit resistors for chip size saving. And The DAC in this work is especially good at DNL when get to 12bit resolution. The INL of this work is similar with the dual 12bit current-steering DAC in the paper [7].

Table 1 Comparison with other papers

Source	Architecture	Process	Resolution	DNL (LSB)	INL (LSB)	Supply voltage
[3]	Dual-ladder without self-adjusted reference	0.35	10bit	0.4	0.7	3.3V
[7]	Dual current-steering without self-adjusted reference	0.13	12bit	1	2	3.3V
[9]	Capacitive and resistive with self-adjusted reference	0.5	10bit	0.43	0.54	±5V
This work	Dual-ladder with self-adjusted reference	0.5	12bit	0.25	2	±5V

4. Conclusions

In this paper, a 12 bit dual-ladder resistor string DAC has been presented in a 0.5μm CMOS technology. The DAC employs an accurate method for getting absolutely symmetric differential reference voltages. The measured results show that the proposed self-adjust reference circuit and output buffer are very efficient. The use of self-adjusted architecture can improve the accuracy. It also can simplify traditional DAC topologies to reuse the resistors of the differential reference voltages circuit as the dual-ladder resistor string. And it also adopts an output buffer with class-AB stage for fast setup time. The 12 bits dual ladder resistor DAC achieves INL and DNL of 2LSB and 0.25LSB, respectively. The presented DAC features the advantages of high precision, good monotonicity, and excellent symmetry, which is ideal for the application of MEMS accelerator system to generate a steady voltage.

Acknowledgment

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