Diagnosis of Resistive-Open Defects using I_{DDT} in Digital CMOS Circuits

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Abstract: - A resistive-open defect is an imperfect circuit connection that can be modeled as a defect resistor between two circuit nodes that should be connected. Resistive-open defects will not cause function fault immediately, but it will cause the delay fault, and cannot use the method of voltage to survey. In this paper, we propose a test method of transient power supply current (IDDT) for resistive open faults, and use wavelet analysis to location the fault. The experimental results show that the effectiveness of IDDT methods uses the RMS values of the wavelet transforms of the transient power supply or ground currents. The delay faults test process to be very effective in all cases.

Key-Words: - Resistive-open defects, Transient power supply current (I_{DDT}), Digital circuit, Wavelet analysis.

1 Introduction

The rapid development of technology in the area of the digital CMOS circuits results in an increase in the size of circuits, severe leakage, very large process variations, more process defects and new defects that are not yet modeled or detected by traditional testing techniques. There has been an increase a need for new more efficient testing techniques [1].

Traditional testing techniques include voltage testing and static power supply current (I_{DDQ}) testing [2] [3]. Transient power supply current (I_{DDT}) testing for resistive open faults has been researched in domestic and foreign for the past ten years [4][5][6]. This test method able to detect the resistive-open defects, while the static power supply current (I_{DDQ}) testing is invalidation on research. Some resistive-open defects do not cause failure of the circuits function immediately, but it will introduce a noticeable delay in the output, and cannot use the traditional testing method of voltage testing to detect effectively. They are the latent unreliability factor that will make functionality expiration during sometimes later. Thus the resistive-open defects will reduce the product the reliability.

Influence within kind of testing condition for test result on resistive-open defects such as supply voltage, test speed, test temperature has been presented in [7]; However, the research on the diagnosis technology of the resistive-open defects based on transient power supply current(I_{DDT}) has been limited.

In this paper, we will study the resistive-open defects on CMOS circuits. From extensive SPICE simulation, we make an inverter chain example to detect the resistive-open defect within the test method of transient power supply current (I_{DDT}). Then make the fault diagnosis and setup defect dictionary after using wavelet analysis.

The rest of the paper is organized as follows: In Section II we provide a theoretical analysis about the resistive-open defects based on transient power supply current (I_{DDT}) summarized as related work. In Section III we explain the diagnosis method used, describe our experimental setup, and show the simulation results of resistive-open defects. Finally, we conclude our work in section 4.

2 Related work

2.1 Model of resistive-open defects

Previous research classified opens into strong opens (>10MΩ) and weak opens (≤10MΩ) [8]. Strong opens cause stuck-at faults and therefore, can be detected by regular stuck-at patterns. Weak opens cause delay faults and therefore, may not be detected by regular stuck-at patterns [9][10]. Rodriguez-Montanes and Gyvez [7] showed that in modern deep sub-micron technology, the percentage of weak opens is high enough to require delay fault testing.

A resistive-open defect is defined as an imperfect circuit connection that can be modeled as a defective resistor between the circuit nodes that should be connected [11]. Fig. 1 shows a defective wire that can be modeled by a resistive open defect (r_0). Examples of resistive-open defects are thin wires, ill-formed contacts (visa), or cracks in silicides.

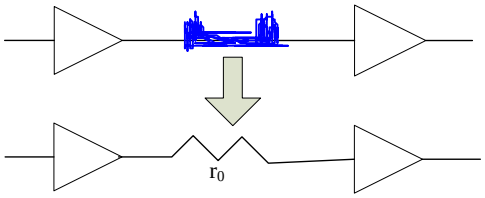

Fig. 1. Resistive-open defects

It is difficult to detect resistive-open defects, because they have timing-dependent test results, which means the test results change with the test speed.

The time-delay resistive-open defects model is shown in Figure 2. In this model, a resistive-open defects is represented by a resistor r_o in a net at the location where the open defect may occur. RC network is transistor of open resistance and circuit of distributed capacitance and load capacitance.

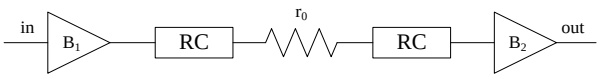

Fig.2 Model of resistive-open defects

The input buffer B_1 and output buffer B_2 represent arbitrary CMOS gates. From extensive SPICE simulation, we found the delay increases almost linearly with the open resistance [12].

2.2 The test technique for resistive-open defects based on transient power supply current (I_{DDT})

In the resistive-open defects test, static power supply current (I_{DDQ}) hasn't a remarkable change because the extra delay caused by defects is in order of nanoseconds. This extra delay is too short to caused any I_{DDQ} current. The overall conclusion is that, I_{DDQ} testing is not guaranteed to be effective for resistive opens [8].

I_{DDT} testing (measuring the transient current of the chip as a function of time) was shown to be more effective than I_{DDQ} testing in detecting resistive open defects in simulation [13], a single NAND gate with resistive open was shown to have elevated I_{DDT} current, which is different form the I_{DDT} current of a good NAND gate. Practically, in a large, a large number of gates are switching simultaneously which makes it difficult to distinguish the effect of a defect. Research in applying I_{DDT} testing for detecting resistive open defects is being carried out.

2.2.1 The IDDT curve on resistive-open defects

In order to study the relationship between resistive-open defects and I_{DDT}, the example setup as Figure 3.

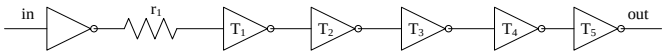

Fig3.Five Inverter Chains

First, determine insert r_1 with scanning method between inverter chains. From Fig.2, The output signal can increase the delay depending on the input resistive-open defects resistance with RC delay. Then decrease half of delay time on output single to 50% input pulse width, the insert resistive-open resistance take the non-action resistance on circuit processing(input plus width = 2 ns, resistance = 500 kΩ).

Based on the above analysis, we found the I_{DDT} is regular in Figure 4. We can distinguish the large difference on defect form normal curve in Figure 4; nevertheless there is not any fault on Functional Test for this circuit. The regular in Figure 4 is differ from the second peak value. No resistive-open defects resistance circuit isn't have the second peak value; contrarily insert resistive-open defects resistance circuits not only have second peak value but also decreasing with the distance of inserted circuit pole. In other words, the sequence of second peak current value is $T_1>T_2>T_3>T_4>T_5$, and so that phenomenon show the position information for the resistive-open defects to make a positioning tool for the defects.

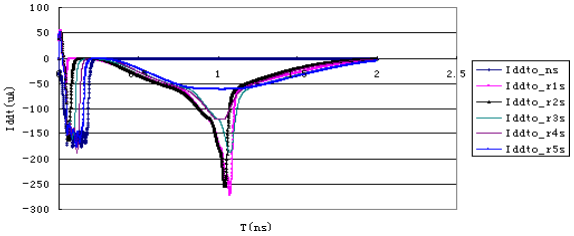

Fig.4 I_{DDT} cure

2.2.2 Relation between resistive-open defects and delay time

Second step in this research is finding the change on I_{DDT} about different resistive-open defects resistance in inverter chains circuit. In order to take this consequence, we scan parameters for inserting resistive-open defects resistance on SPICE (Fig. 5).

Figure 5 show the regular that more large about the inserted resistance more distance of second current peak presenting in the circuit.

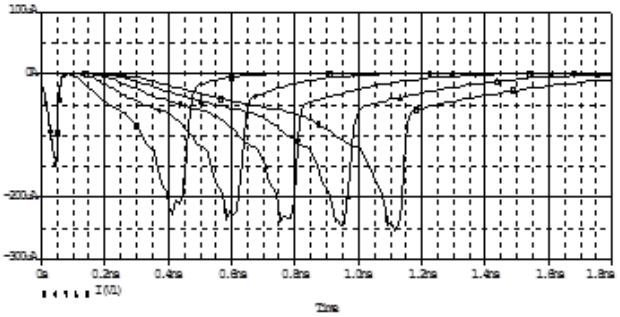

Fig.5 T_1 I_{DDT} curve

2.2.3 Relation between Position of resistive-open defects and I_{DDT} Curve

Fig.6 show the different form inserted resistive-open defects resistance position of T_1 and T_5.

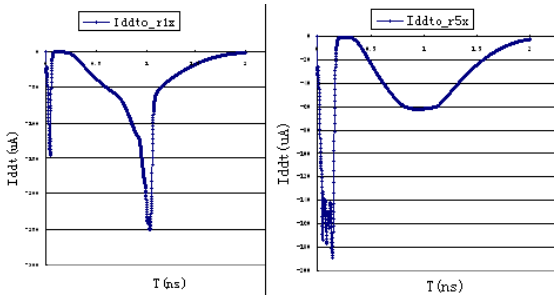

Fig.6 T_1 and T_5 I_{DDT} curve

The curve of I_{DDT} can be put into a one-to-one correspondence with the inserted resistive-open defects resistance position. It means there are two current peaks in SPICE simulation. The first current peak show the number of former phase reverser that present on numbers small current peak; the second current peak consequent for the delay by resistive-open defects on circuit. The second current peak value is direct proportion with the latter part in circuit.

Furthermore, there is only one peak in the first current peak. The simulation example also shows the first current peak value is the min value and the second peak is the max value in all resistive-open defects resistance inserted while the defect has been inserted on T_1. Then there are two peaks in first current peak and the second peak only smaller than the former condition when the resistance insert in T_2. So the T_5 inserted includes 5 peaks in first current peak and the value is the Maximal, the second current peak value is the minimal in all resistive-open defects inserted condition.

To sum up, the I_{DDT} testing adapts to detect and position the resistive-open defects extremely. Through the test we are able to get the resistive-open defects position information by the current curve versus time. Because of the simulation take the phase reverser as examples, so the test is keep working on gate array and combinational logic circuit.

3 Experimental setup

3.1 Wavelet analysis

The defects position information couldn't be detect by using average transient current, so the method of Signal Analysis and Processing is necessarily.

Wavelet transform based on the Fourier analysis. It is localization in space and time domain and the localization form adapt to frequency automatically. For example the wavelet transform gets a narrow time window on High-Frequency and gets a wide on Low-Frequency to the contrary. These characteristics are suited to processing nonstationary signal. In the research, wavelet transform uses to pretreat sampling data for get fault signature in fault diagnosis of integrated circuits.

The wavelet transform divides a low-frequency signal and a signal of high frequency fine appearance based on a real/complex valued continuous time function. It uses to wavelet function and flexibility to achieve the translation. The CWT or the Continuous Wavelet Transform of a function $f(t)$ with respect to a wavelet $\psi(t)$ is defined as follows:

$$W(a,b) = \int_{-\infty}^{+\infty} f(t)\psi_{a,b}^{*}(t)dt \qquad (1)$$

$$\psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\psi(\frac{t-b}{a}) \qquad (2)$$

Where a is a positive real number that represents the scale, b is the translational value, and $*$ indicates complex conjugate. $W(a, b)$ is the transform coefficient of $f(t)$ for given a, b. Thus the wavelet transform is a function of two variables. For a given $a, \psi_{a,b}(t)$ is a shift of $\psi_{a,0}(t)$ by an amount b along time axis. The variable b represents time shift or translation. Since a determines the amount of time-scaling or dilation, it is referred to as scale or dilation variable. If $a > 1$, there is stretching of $\psi(t)$ along the time axis whereas if $0 < a < 1$ there

is a contraction of $\psi(t)$ **.** Each wavelet coefficient W(*a, b***)** is the measure of approximation of the input waveform in terms of the translated and dilated versions of the mother wavelet.

3.2 Faults Feature Extraction based on wavelet transform

As Figure 2 shows the SPICE simulation on inverter chains, the transient current through power will be changed, and therefore the current signal amplitude-frequency characteristic and phase-frequency characteristics will have varying degrees of change when the resistive-open defects emergence. Circuit at different levels has a different output current on different pole inserted resistance. We detect the defects by analysis the characteristics of different current peak within wavelet transform. Haar wavelet function of the discontinuity characteristics make compactly supported and of zero to reconcile. Therefore, Haar wavelet is well suited from a narrow width and the rapidly changing characteristics of the signal to extract features, and a simple calculation. So it is used in the transient currents test in CMOS circuit.

Based on the above analysis, in fault diagnosis of the defects signal in wavelet analysis can be broadly divided into the following steps:

1)*step1*. Sample transient defects current information through PSPICE simulation in circuit.

2)*step2*. Make the transient current wavelet decomposition through Matlab wavelet tools.

3)*step3*. Extract wavelet coefficients and setup fault dictionary.

3.3 Experimental results and analysis

We have performed fault simulations of CMOS gate circuits using Monte Carlo analysis in PSPICE with complete process variations. Below are the results for

In the research the r_1-r_5 (resistive-open defects resistance, 500 kΩ) has been inserted between T_1-T_5. Simulation uses PSPICE with 0.18μm Process Parameters into MATLAB7.0. In order to close to the actual situation, Resistance to obey the normal distribution of Monte-Carlo simulation has been process 50 times and get 50 group current signal. Then process wavelet packet decomposition respectively, and 10 samples group of each set of data failure. The root mean square value defined in (3) as testing standards [14].

$$RMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{F_i - G_i}{G_i}\right)^2} \qquad (3)$$

It computes the root mean square of the difference between the coefficients for golden circuit response (G_i) and those for the DUT (F_i) as a fraction of the golden circuit coefficient (G_i) and can be considered **as** the direct measure of sensitivity. The Table 1. shows the fault direction within r_1-r_5.

Table 1. Fault dictionary

Fault model	**RMS**
Resistive-open r_1	0.058
Resistive-open r_2	0.431
Resistive-open r_3	0.946
Resistive-open r_4	0.375
Resistive-open r_5	0.424

In Fault diagnosis period, take the other 40 group sampling data as testing data, then calculates non-fault circuit G_i and F_i to detect fault location through the fault direction in Table 1. The result as Table 2. shows.

Current signal after wavelet packet decomposition has a good rate of fault diagnosis. The average rate of correct diagnosis gets 95%.

Table 2. diagnosis result

Fault model	total	Fault number	Percentage
Resistive-open r_1	40	35	87.5
Resistive-open r_2	40	36	90
Resistive-open r_3	40	40	100
Resistive-open r_4	40	39	97.5
Resistive-open r_5	40	40	100

4 Conclusion and future work

In this paper, we propose a test method of transient power supply current (I_{DDT}) for resistive open faults by simulation. Our effective analysis results show that I_{DDT} testing is able to present the defects information as a location tools. At the same time, we take fault feature extraction and setup the fault dictionary within wavelet analysis. The combination of transient current (I_{DDT}) and wavelet technology in digital circuit for testing resistive open defects effectively.

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References:

[1] International Technology Roadmap for Semiconductors,2009 Edition, available at the following URL http://www.itrs.netLinks/2009 ITRS/Home2009.htm.

[2] A. C. Miller, IDDQ Testing in Deep Submicron Integrated Circuits, *Int. Test Conf.*, pp.724-729,1999.

[3] H.Manhaeve, Current Testing for nanotechnologies: A Demystifying Application Perspective, *IEEE International Workshop on Current and Defect Based Testing (DBT 2005)*,pp. 49-56, 2005.

[4] Hamieh L, Mehdi N, Omeirat G, et al. The effectiveness of delay and IDDT tests in detecting resistive open defects for nanometer CMOS adder circuits, *Design and Test Workshop (IDT), 2011 IEEE 6th International. IEEE*, 2011: 53-57.

[5] Gyepes G, Arbet D, Brenkus J, et al. Application of IDDT test towards increasing SRAM reliability in nanometer technologies, *Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2012 IEEE 15th International Symposium on. IEEE*, 2012: 167-170.

[6] Gyepes G, Stopjaková V, Arbet D, et al. A new IDDT test approach and its efficiency in covering resistive opens in SRAM arrays, *Microprocessors and Microsystems*, 2014, vol.38, No.5: 359-367.

[7] James Chien-Mo Li, Edward J. McCluskey, Diagnosis of Resistive-Open and Stuck-Open Defects in Digital CMOS ICs, *IEEE Transaction on Computer-aided Design of Integrated Circuits and Systems*,vol.24,No.11,Nov.2005.

[8] R.Rodriguez-Montans and J. P. de Gyvez, Resistance characterization for weak open defects ” , *IEEE Design and Test* , Sept.2002,pp:18-25 .

[9] W. Moore, G. Gronthoud, K. Baker and M.Lousberg, Delay-fault testing and defects in sub-micron Ics-does critical resistance really mean, anything?, *ITC*,2000,95-104.

[10] C. F. Hawkins, J.M.Soden, A.W.Righter, F.J.Ferguson, Defect classes-an overdue paradigm for CMOS IC testing, *ITC*, 1994， 413-425.

[11] James C. M, Li, Chao-Wen Tseng, E.J. McCluskey, Testing for Resistive Opens and Stuck Opens , *ITC*,2001,1049-1058 .

[12] ZhuoLi,XiangLu,Wangqi Qiu,Weiping Shi, D.M.H.Walk- er, A Circuit Level Fault Model for Resistive Opens and Bridges, *Proceedings of the 21st IEEE VLSI Test Symposium (vts'03)*,2003.

[13] Kruseman, B, Comparison of Defect Detection Capabilities of Current-based and Voltage-based Test Methods, *Proc. European Test Workshop*, 2000,175-180.

[14] S. Bhunia, K. Roy, A novel wavelet transform-based transient current analysis for fault detection and localization, *IEEE Transcations on Very large Scale Integration (VLSI) Systems*,2005,13(4):503-507.