Testing of N-Stage 1 bit per stage Pipelined ADC using Test Input Regeneration

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Abstract: - Analog-to-Digital Converters (ADCs) became an integral part in most systems. The Pipelined ADC (PADC) is one of the preferred ADCs; it is perfect for applications requiring high speed and medium resolution. Hence, the test of ADCs in general as well as PADCs is not only interesting but mandatory; the need for a low cost and efficient test technique in order to test the PADC is increasing. The focus in this paper is on proposing a new efficient test technique fitting an N-stage PADC test. The proposed technique depends on the selection of test inputs that can be applied to the first stage of the PADC and it is guaranteed that they can be regenerated at the input of next stages in the PADC. This proposed technique does not use complex hardware and there is no need to access the input or output of each individual stage. It will be shown that only two DC test inputs are able to detect all catastrophic faults in the N-stage PADC producing 100% fault coverage. The simulation results are based on circuit-level simulations using the Eldo simulator provided by Mentor Graphics.

Key-Words: - PADC, Test Input Regeneration, N-stage, Catastrophic, Fault model, Structural test.

1 Introduction

Mixed analog and digital signal integrated circuits became the most mandatory part in most systems. One of the most famous blocks in mixed signal devices are Analog-to-Digital Converters (ADCs). Among many ADC types, the Pipelined ADC (PADC) is usually preferred for high speed and reasonable resolution applications (e.g., HDTV, WLAN and ADSL data channels) [1, 2]. Hence, the need for a time efficient and low cost test to detect all faults in ADCs in general and PADCs in particular became indispensable. The ADCs specifications are divided into static parameters and dynamic parameters. The ADCs static parameters include accuracy, differential nonlinearity (DNL), and integral nonlinearity (INL) while the dynamic parameters include effective number of bits (ENOB), signal to noise and distortion ratio (SNDR), and total harmonic distortion (THD). Many tests were developed to measure these parameters such as the histogram test which is used to measure the linearity (INL and DNL) of the ADC [3]. In addition, the fast Fourier transform is used to measure the SNDR, ENOB, and THD of the ADC [3]. In [4], a test approach based on the oscillation-test method is applied in order to test the ADC. The oscillation test method is based on converting the ADC under test to an oscillator. Then, depending on the oscillation frequencies and amplitudes, some ADC parameters can be determined.

In addition, testing the Flash ADC is investigated in [5]; test inputs were generated using an Autonomous Linear Feedback Shift Register (ALFSR). These generated digital test inputs were then converted to analog by the use of a DAC. The test set consists of the analog values producing correct outputs even in the presence of noise. Moreover, in [6], the test of a first order delta-sigma converter was considered. The circuit includes mixed analog and digital signals. It was proven that two analog test inputs can detect all faults. In [7], the test of an N-stage PADC is investigated using Built-in-Self-Test (BIST), one stage at a time. Many DC test values are selected in order to test each stage. Both analog and digital outputs of each stage are utilized to detect faults by comparing them to correct outputs generated by BIST circuitry. Nevertheless, no specific fault model is presented.

Besides, a DC input value is required for each probable digital output value. In [8], the study of a SIMULINK (MATLAB) behavioral model of a 3-stage PADC is considered. It presents a system including a module able to model the ADC behavior, another module executing the device dynamic testing, and a database providing the data sharing among remote users and virtual instruments developed in Java to control the system functions remotely.

Although functional tests are often used in PADCs production testing, such tests are expensive and time consuming due to the need for complex equipments able to handle the large amount of data required to measure the most important parameters, like the DNL and the INL [7]. Structural tests (which are the subject of this paper) are time efficient and low cost. They could be used before the functional tests so as to exclude the defected ICs. Moreover, structural tests can be performed at the customer's premises during the incoming inspection because of the low cost test setup requirements [9].

This paper focuses on introducing a new test technique in order to test N-stage PADC. This test technique aspires to achieve the test without adding complex extra hardware. Moreover, the proposed test technique depends on observing the available digital output. This technique depends on the selection of a test input that can be applied to the first stage of the PADC and can be regenerated at the input of next stages in the PADC. It will be shown that only two DC test inputs are enough to detect all catastrophic faults in the N-stage PADC producing 100% fault coverage. The results are based on circuit-level simulations using the Eldo simulator provided by Mentor Graphics.

This paper is organized as follows. Section 2 discusses the PADC architecture and operation and then it explains the one stage (1 bit per stage) PADC. Section 3 presents the previous works. In Section 4, the proposed test technique to test the N-stage PADC is explained and illustrated using simulation results. Finally, Section 5 concludes the paper.

2 Pipelined Analog-to-Digital Converter (PADC)

The PADC is preferred over other ADC types in case of applications that require high speed and reasonable resolution [10]. One of the most famous architectures of PADC is the 1 bit per stage PADC; this is due to its simplicity and easiness to achieve a high resolution [11].

2.1 Circuit Architecture and Operation

The architecture of the N-stage PADC is shown Fig. 1. It consists of N-1 identical stages and a last stage which is a simple flash ADC. Each of the N-1 stages includes of a sub-ADC and a multiplying DAC (MDAC); the MDAC consists of a sub-DAC, a subtractor and an amplifier. In the N-1 stages, the analog input signal is digitized through the sub-ADC, generating the digital output for this stage. This digital output is converted back into analog by the sub-DAC; this analog signal is subtracted from the original input signal producing the analog difference output, which is called the residual signal. This residual signal is amplified to the full scale through an amplifier. Then, the amplified residual signal is passed to the next stage and the same procedure is repeated. This procedure occurs parallel in every stage; this is why the circuit is called PADC [12].

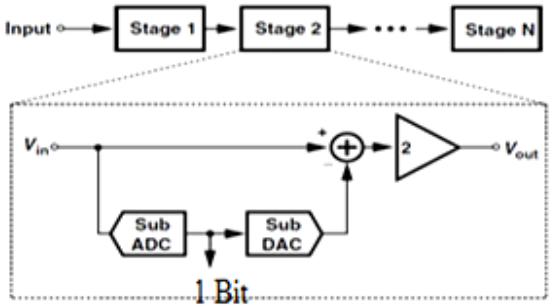

Fig. 1 Pipelined Analog-to-Digital Converter

Note that the PADC provides time efficiency since each stage processes its input concurrently. Hence, at the same moment, each stage is processing a different sample. Therefore, in order to align the digital output of each stage, there is a need for a time alignment circuit. After surpassing the time alignment circuit, the digital output is the output of the same sample. The circuit of the time alignment is shown in Fig. 2 [13]; it consists of latches to align the outputs.

According to [13], the number of latches L used in time alignment can be deduced to be:

If N is even:

$$L = \frac{N}{4}(N + 4) \quad (1)$$

And if N is odd:

$$L = \left(\frac{N-1}{4}(N+3)+1\right) \quad (2)$$

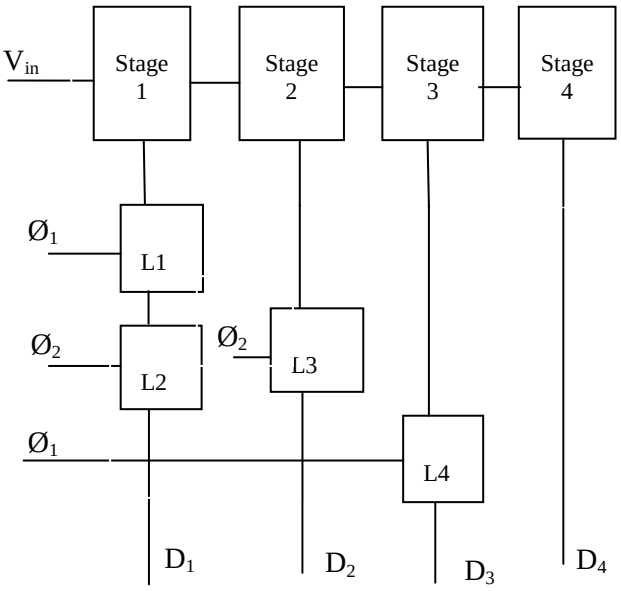

Fig. 2 Time alignment circuit

2.2 One Stage (1 bit per stage) PADC

The one stage PADC circuit is shown in Fig. 3.

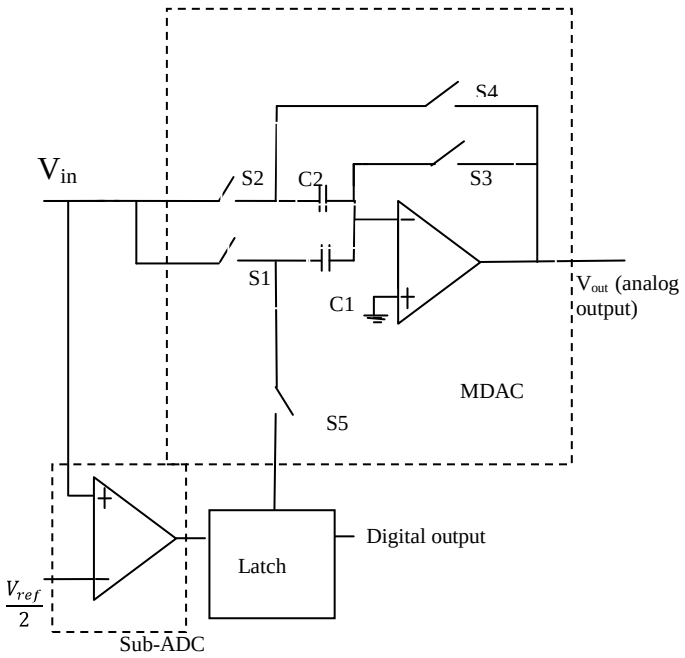

Fig. 3 One stage (1 bit per stage) PADC

This circuit produces 1 bit per stage [11]. This stage consists of two main parts:

- Sub ADC: The sub ADC is a comparator; the positive terminal of the comparator is connected to the analog input, while its negative terminal is connected to V_{ref} /2. The output of the comparator is KV_{ref}, where K= 1 if $V_{in} > V_{ref}$ /2 and K=0 if $V_{in} < V_{ref}$ /2. This is the stage digital output.
- Multiplying DAC (MDAC): The MDAC consists of a switched capacitor circuit [12, 14, 15]. This switched capacitor circuit consists of an operational amplifier (Op Amp), two capacitors with equal values, and five transmission gates realizing the switches. Three switches (S1, S2, S3) are controlled by Φ_1 and the remaining two switches (S4 and S5) are controlled by Φ_2, where Φ_1 and Φ_2 are non-overlapped clocks.

The function of the circuit, shown in Fig. 3 is depicted in [16]:

- In the sampling mode (during Φ_1), the total charge stored on C_1 and C_2 is equal to:

$$Q_{Sampling} = (C_1 + C_2)\, V_{in} - (C_1 + C_2 + C_x)V_x \quad (3)$$

where C_x is the input capacitance of the Op Amp and V_x is the voltage at the inverting input of the op amp.

- In the amplification mode (during Φ_2), the sub-ADC is clocked, C_2 is connected across the op amp and the left terminal of C_1 is connected to the output of the comparator. The total charge existing on C_1, C_2 and C_x in this mode is given by:

$$Q_{Ampification} = C_1KV_{ref} + C_2V_{out} - (C_1+C_2+C_x)V_x \quad (4)$$

Since, conservation of charge requires that $Q_{Amplificationn} = Q_{Sampling}$, the following equation can be obtained:

$$C_2V_{out} = (C_1 + C_2)V_{in} - C_1KV_{ref} \quad (5)$$

and since $C_1 = C_2$, therefore:

$$V_{out} = 2V_{in} - KV_{ref} \quad (6)$$

where K = 1 if $V_{in} > V_{ref}$ /2 and K = 0 if $V_{in} < V_{ref}$ /2.

3 Previous Works

3.1 Testing of One Stage PADC

In [17], the test of a one stage (1 bit per stage) PADC shown in Fig. 3 (excluding the latch), is studied. A single catastrophic fault at a time is considered [18]. The test applied to the circuit is a DC test where V_{ref} = V_{DD} =1V and V_{SS} = 0V. Simulations were run in the range of 0V to 1V with a 0.02V increment. It was proven that two test inputs are enough to detect all faults in the fault set. Simulations showed that one test input can be selected from the range $0.52V \leq V_{in} \leq 0.78V$ and this test input detects all the faults in the stage except the comparator output stuck-at-V_{DD} and the comparator output stuck-at-V_{pos} (where V_{pos} is the positive saturation voltage). The second input is selected from the range $0V \leq V_{in} \leq 0.48V$ to perform the full coverage test. An example test set is shown in Table 1.

Table 1. Test set example in [17]

Fault	V_{in}=0.4V		V_{in}=0.6V	
	Digital output	Analog output (V)	Digital output	Analog output (V)
Fault-free	0	1	1	0.354
Op- amp output	0	0	1	0
Op-amp output	0	1	1	1
Op-amp output	0	0.78	1	0.78
Op-amp output	0	0.22	1	0.22
Comparator	0	1	0	0.996
Comparator	1	0.153	1	0.361
Comparator	1	0.141	1	0.354
Comparator	0	0.999	0	1
C1 is open	0	0.388	1	0.571
C1 is shorted	0	0.184	1	0
C2 is open	0	1	1	0
C2 is shorted	0	0.071	1	0
S1 stuck-On	0	0.448	1	0.452
S1 stuck-Off	0	0.519	1	0.565
Shorted S1	0	0.464	1	0.462
S2 stuck-On	0	0.884	1	0.07
S2 stuck Off	0	0.999	1	0.01
Shorted S2	0	0.869	1	0.06
S3 stuck-On	0	0.031	1	0.019
S3 stuck-off	0	1	1	0.545
Shorted S3	0	0.032	1	0.022
S4 stuck-On	0	0.08	1	0.023
S4 stuck-Off	0	1	1	0
Shorted S4	0	0.076	1	0.02
S5 stuck-On	0	0.458	1	0.459
S5 stuck-Off	0	0.388	1	0.562
Shorted S5	0	0.444	1	0.462

The detected faulty digital outputs and faulty analog outputs are underlined. The detection of most faults depends on observing the analog output of the stage which is not an accessible output.

3.2 Testing of N-stage PADC using Extra Hardware

In [19], the main target is to find a test procedure in order to test the N-stage PADC by monitoring only the available digital outputs. It was concluded in [19] that 3 DC test inputs are needed to perform a full coverage test of one stage PADC. The test of one stage is performed by monitoring the digital outputs of the stage itself and its succeeding stage. This conclusion is the main key to test the whole N-stage PADC. The circuit diagram of the N-stage PADC including the extra switches needed to facilitate the test is shown in Fig. 4.

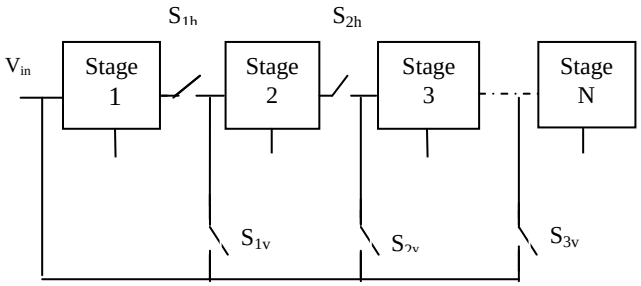

Fig. 4 The proposed test technique in [19]

In Fig. 4, a switch is inserted between each 2 consecutive stages (horizontal switch). In addition, a switch is inserted between V_{in} and each stage input (vertical switch). The controls of horizontal switches which control odd stages are connected together, while the controls of horizontal switches which control even stages are connected together. By analogy, the controls of vertical switches which control odd stages are connected together, while the controls of vertical switches which control even stages are connected together. The test rationale is based on testing the odd stages at the same time, then testing the even stages at the same time. In order to test the odd stages, a test value is applied at V_{in} and the controls of the switches are adjusted so that each odd stage is connected to its following even stage and this pair is disconnected from the following stage; then, by monitoring the digital outputs of each pair, the detection of the faults can be achieved. Only eleven DC test inputs are needed to detect all faults in the N-stage PADC as well as the extra hardware circuitry.

4 New Test Technique of an N-Stage PADC

The purpose of this paper is to introduce a new test technique in order to test N-stage PADC. This test technique aims to avoid the use of extra hardware in order to access each stage input as in [19]. In addition, the proposed test depends on monitoring the available digital output without the need to monitor each stage analog output as in [17]. The proposed technique depends on the choice of a test input that can be applied to the first accessible stage of the PADC and can be regenerated at the input of next stages in the PADC.

4.1 Fault Model

The catastrophic fault models for each component in each stage shown in Fig. 3 are as follow:

- Op-amp faults are modeled by their outputs stuck-at-V_{DD}, outputs stuck-at-V_{SS}, outputs stuck-at-V_{pos} and outputs stuck-at-V_{neg} (where V_{DD} is the positive supply of the Op-amp, V_{SS} is the negative supply of the op-amp, V_{pos} is the positive saturation voltage and V_{neg} is the negative saturation voltage) [20].
- Comparator faults are modeled by their outputs stuck-at-V_{DD}, outputs stuck-at-V_{SS}, outputs stuck-at-V_{pos} and outputs stuck-at-V_{neg} (where V_{DD} is the positive supply of the Op-amp, V_{SS} is the negative supply of the op-amp, V_{pos} is the positive saturation voltage and V_{neg} is the negative saturation voltage) [20].
- The latch fault is modeled by its output stuck-at-V_{DD} and stuck-at-V_{SS} [21].
- The capacitor is modeled by both open fault and short fault. The open fault is modeled by a large resistance in series with the capacitor; while a short fault is modeled by a small resistance across the capacitor [22].
- Switches are realized by transmission gates which have the following fault-model: stuck-on fault shown in Fig. 5; it is modeled by swapping the faulty switch with the ON resistance of the switch R_{ON}.

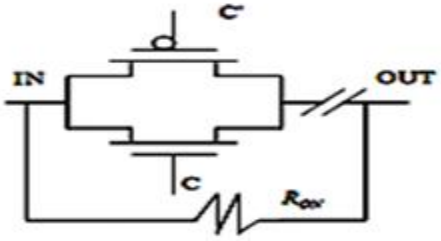

Fig. 5 Switch stuck-on fault

In addition, the stuck-open fault is shown in Fig. 6; it is modeled by swapping the faulty switch with the OFF resistance of the switch R_{OFF}.

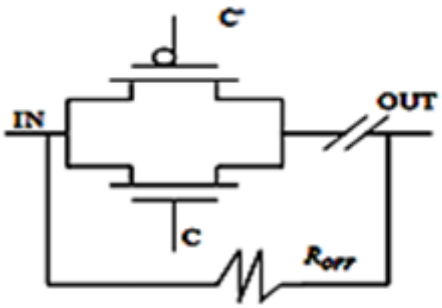

Fig. 6 Switch stuck-open fault

Finally, a shorted switch is shown in Fig. 7; the switch works normally but a resistive impedance R_{short} is added between its input and output terminals [22, 23].

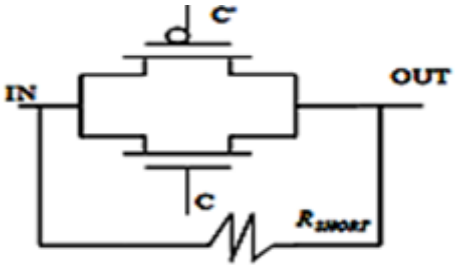

Fig. 7 Shorted switch fault

Table 2 illustrates the catastrophic fault models of each component. Note that $V_{neg}=V_{SS}+V_{THN}$ and $V_{pos}=V_{DD}-|V_{THP}|$, where $V_{THN} =|V_{THP}|= 0.22V$ for 90nm CMOS technology [24, 25].

A single catastrophic fault at a time is assumed as in [18]. Since there are four faults for both op-amp and comparator, two faults for the latch, two faults for both capacitors, and three faults for each of the 5 switches, the total number of faults in each stage of stage 1 is 29 faults. In addition, each latch in the time alignment circuit is modeled by 2 faults. A summary of the components fault names and models is shown in Table 2.

Table 2. Catastrophic fault models

Fault name	Fault model
F1 and F3	Capacitor C_1 and C_2 open (R_{open} in series with the capacitor)
F2 and F4	Shorted capacitor C_1 and C_2 (R_{short} in parallel with the capacitor)
F5, F9	Op amp , comparator output s-a-V_{DD} (s-a-1V)
F6, F11	Op amp, comparator output s-a-V_{pos} (s-a-0.78V)
F7, F12	Op amp, comparator output s-a-V_{SS} (s-a-0V)
F8, F14	Op amp, comparator output s-a-V_{neg} (s-a-0.22V)
F10	Latch output s-a-V_{DD} (s-a-1V)
F13	Latch output s-a-V_{SS} (s-a-0V)
F15, F18, F21, F24, F27	Switches S1, S2, S3, S4, S5 stuck on (the switch is replaced by R_{ON})
F17, F20, F23, F26, F29	Switches S1, S2, S3, S4, S5 stuck open (the switch is replaced by R_{OFF})
F16, F19, F22, F25, F28	Shorted switches S1, S2, S3, S4, S5 (R_{short} in parallel with the switch)
FL1, FL2, FL3, FL4	Time alignment latches output s-a-V_{DD} (s-a-1V)
FL5, FL6, FL7, FL8	Time alignment latches output s-a-V_{SS} (s-a-0V)

4.2 Test Input Regeneration

The proposed technique determines a test input that can be applied to the first stage of the PADC and can be regenerated at the input of other stages in the PADC. The number of test inputs is related to the input range as follows: Since the input is compared to (V_{ref} / 2) as shown in Fig. 3, hence, the range of inputs can be divided into 2 regions: region A: V_{in} < 0.5V and region B: V_{in} > 0.5V. Since the range of inputs is divided into 2 regions, then at least 2 test inputs are needed. Let us assume a test input T1 in range A and a test input T2 in range B. According to Equation (6), if both T1 and T2 can generate each other, then, they will follow the equations:

$$T1 = 2T2 - V_{ref} \quad (7)$$

$$T2 = 2T1 \quad (8)$$

The previous equations can simply be written in a matrix form as follows:

$$\begin{bmatrix} T1 \\ T2 \end{bmatrix} = \begin{bmatrix} 0 & 2 \\ 2 & 0 \end{bmatrix} \begin{bmatrix} T1 \\ T2 \end{bmatrix} + \begin{bmatrix} -1 \\ 0 \end{bmatrix} V_{ref} \quad (9)$$

By solving (9), the following values are obtained: T1 = 1/3 V and T2 = 2/3 V. For example, if the input voltage to stage 1 in Fig. 8 is V_{in} = T1 = 1/3 V (range A), then the analog and digital outputs of stage 1 will be T2= 2/3 V and '0' respectively. In addition, if the input of stage 2 is V_{in} = T2 = 2/3 V, then the analog and digital outputs of stage 2 will be T1 = 1/3 V and '1' respectively. It is obvious from Fig. 8 that both T1 and T2 can reach the input of any stage of the N-stage. In case of starting with T1, the digital output pattern will be P1='0101……'.

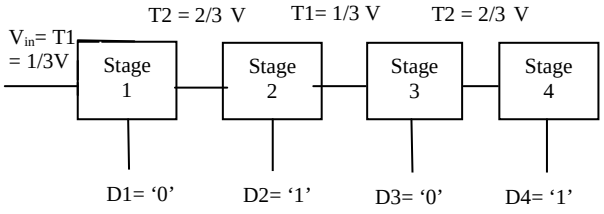

Fig. 8 Test input regeneration starting with T1

In addition, in case of starting with T2, the digital output pattern will be P2='1010…..' as shown in Fig. 9.

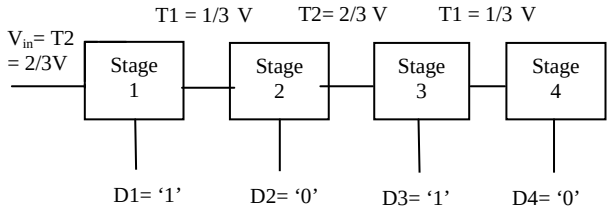

Fig. 9 Test input regeneration starting with T2

4.3 Simulation Setup and Results

As mentioned in Section 4.1, each stage of the N-stage PADC has 29 faults. In order to test the 4-stage PADC shown in Fig. 8, the following are used: Both capacitors C_1 and C_2 have the same capacitance value of 1PF [26]. The macro-model of the Op-Amp has an open loop gain A of 10^3, its positive supply voltage is 1V and its negative supply voltage is 0V [27, 28]. Switches are clocked with a 100MHZ clock as in [10], and they are implemented

in 90nm MOS model provided from MOSIS. All switches have the same ON and OFF resistances; R_{ON} is found by simulation to be 870Ω and R_{OFF} is 80MΩ [29]. Moreover, R_{short} is considered to be equal to R_{ON} as in [23]. By similarity, both short and open faults of the capacitor are modeled using the same values of R_{ON} and R_{OFF} of the switch, respectively [30]. The DC operations of the fault-free and faulty circuit are verified using Eldo simulator provided by Mentor Graphics. The test applied is a DC test where V_{ref} = 1V. Simulations of a 4-stage PADC shown in Fig. 8 were run using the 2 test inputs T1 and T2. It was proven that these 2 test inputs are able to detect all catastrophic faults in the first stage. It is important to note that the detection of faults in the first stage using T1 can be divided into categories: detected faults by monitoring the digital outputs of the first stage and one succeeding stage as shown in Table 3, detected faults by monitoring the digital outputs of first stage and two succeeding stages as shown in Table 4, and detected faults by monitoring the digital outputs of the first stage and three succeeding stages as shown in Table 5. Note that for the time alignment circuit, the input to any time alignment latch is the output coming from the latch inside the stage; hence, the same test input able to detect the faulty latch (inside the stage) can detect the faulty time alignment latch.

Table 3. Faults detected using T1 and observing D1 and D2

	V_{in} = T1 = 1/3V
Fault free	'D1D2' = '0 1'
F1, F2, F4, F7, F8, F15, F16, F17, F21, F22, F24, F25, F29	'D1D2' = '0 0'
F9, F10, F11	'D1D2' = '1 0'

Table 4. Faults detected using T1 and observing D1, D2, and D3

	V_{in} = T1 = 1/3V
Fault free	'D1D2D3' = '0 1 0'
F3, F18, F19, F20, F26	'D1D2D3' = '0 1 1'

Table 5. Faults detected using T1 and observing D1, D2, D3, and D4

	V_{in} = T1 = 1/3V
Fault free	'D1D2D3D4' = '0 1 0 1'
F27, F28	'D1D2D3D4' = '0 1 0 0'

The same categories exist for detected faults using T2, as shown in Tables 6, 7, and 8.

Table 6. Faults detected using T2 and observing D1 and D2

	V_{in} = T2 = 2/3V
Fault free	'D1D2' = '1 0'
F1, F5, F17, F23, F29	'D1D2' = '1 1'
F12, F13, F14	'D1D2' = '0 1'

Table 7. Faults detected using T2 and observing D1, D2, and D3

	V_{in} = T2 = 2/3V
Fault free	'D1D2D3' = '1 0 1'
F3, F20, F26	'D1D2D3' = '1 0 0'

Table 8. Faults detected using T1 and observing D1, D2, D3, and D4

	V_{in} = T2 = 2/3V
Fault free	'D1D2D3D4' = '1 0 1 0'
F27, F28	'D1D2D3D4' = '1 0 1 1'

For better illustration, consider the fault F1 (C_1 open) injected in stage 1 shown in Fig. 4 (a). If V_{in} = T1 = 1/3 V, then according to the analysis of the circuit shown in Fig. 2: during the sampling mode, only C_2 is charged via V_{in}. Then, during the amplification mode, V_{analog} will be connected to the left plate of C_2. Therefore:

$$V_{analog} = V_{in} = T1 = 1/3 \text{ V} \quad (10)$$

Then, the analog output of stages 2, 3, and 4 will be 1/3 V, 2/3 V, and 1/3 V respectively. Therefore, the digital output of stages 1, 2, 3, and 4 will be '0', '0', '1', and '0' respectively which is different than the fault free pattern. Note that the fault is detected by monitoring only D1 and D2. Fig. 7 shows the faulty digital output in case of F1.

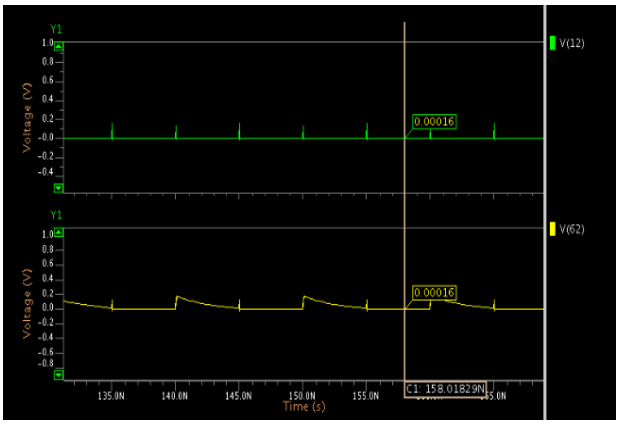

Fig. 10 The faulty case (F1) digital output (C_1 open)

However, the fault free output in case of using test input T1 will be as shown in both Table 3 and Fig. 11.

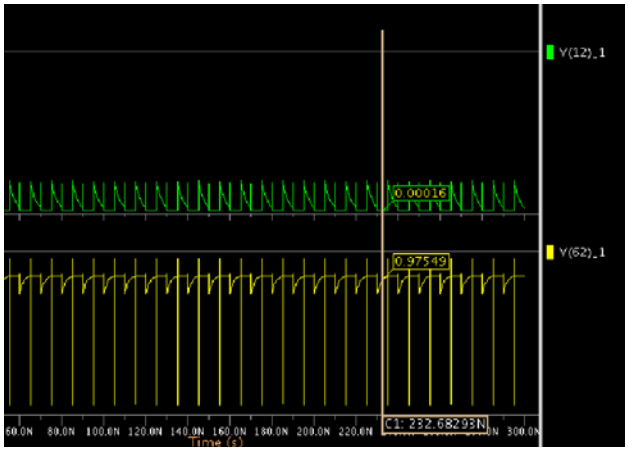

Fig. 11 The fault free case digital output using T1

4.4 Extension of the Proposed Technique for an N-Stage PADC

For an N-stage PADC, the proposed technique can be extended as shown in the following:

- For any stage starting from stage 1 up to stage N-3: The proposed test can detect all the 29 faults in each stage by monitoring the digital outputs of the stage under test and its succeeding stage.
- For stage N-2: The proposed test can detect only 27 faults by monitoring the digital outputs of stages N-2, N-1, and N. There are 2 faults in stage N-2 cannot be detected because in order to detect these 2 faults, the stage must be followed by 3 stages.
- For stage N-1: The proposed test can detect only 22 faults by monitoring the digital outputs of stages N-1 and N. There are 7 faults in stage N-1 that cannot be detected because the stage is not followed by enough stages to detect these faults.
- For stage N: The last stage of the PADC is a simple flash ADC followed by a latch. It consists of 6 faults (4 faults of the comparator and 2 faults of the latch). Hence, it needs 2 test inputs (one test input < V_{ref} /2 in order to detect the s-a-V_{DD} faults, and one test input > V_{ref} /2 in order to detect the s-a-V_{SS} faults). Therefore, T1 and T2 are enough to detect the faults of this stage by monitoring its digital output.

Hence, the Fault Coverage (FC) of the N-stage PADC (excluding the time alignment circuit) can be calculated according to the following equation:

$$\text{FC Percentage} = \frac{29N-32}{29N-23} * 100\% \qquad (11)$$

i.e., for a 10-bit PADC, the fault coverage will be 96.6%. In addition, the Fault Coverage (FC) of the N-stage PADC (including the time alignment circuit) will be as follow:

If N is even:

$$\text{FC Percentage} = \frac{N^2+120N-128}{N^2+120N-92} * 100\% \qquad (12)$$

And if N is odd:

$$\text{FC Percentage} = \frac{N^2+118N-127}{N^2+118N-91} * 100\% \qquad (13)$$

i.e., for 10-bit PADC, the fault coverage including the time alignment circuit will be 97 %

In order to reach 100% fault coverage, it is suggested to add an analog output pin before the last stage so that the 7 undetected faults in stage N-1 and the 2 undetected faults in stage N-2 can be detected by measuring the analog output at the output of the penultimate stage and comparing the faulty analog output with the fault free analog output; the output is considered faulty if it deviates by more than ±10% of the fault free value [31].

5 Conclusion

In most systems, mixed analog and digital signal integrated circuits became an essential part (such as ADCs). The PADC is useful in applications requiring high speed and medium resolution. The need for an efficient test technique in order to test the PADC became important.

This paper focuses on proposing a new test technique in order to test an N-stage PADC. The proposed technique depends on choosing test inputs that can be applied to the first stage of the PADC and it is guaranteed that they can be regenerated at the input of next stages in the PADC. It is shown that only two DC test inputs are able to detect all faults in the N-stage PADC producing 100% fault coverage. The results are based on circuit-level simulations using the Eldo simulator provided by Mentor Graphics.

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