Novel Comprehensive Analytical Probabilistic Models of The Random Variations in MOSFET's High Frequency Performances

RAWID BANCHUIN
Department of Computer Engineering
Siam University
235 Petchakasem Rd., Phasi-charoen, Bangkok 10163
THAILAND
rawid_b@yahoo.com

Abstract: - In this research, the probabilistic models of the random variations in MOSFET's high frequency performance defined in terms of variations in gate capacitance and transition frequency, have been proposed. Both random dopant fluctuation and process variation effects which are the major causes of the MOSFET's high frequency characteristic variations have been taken into account. The short channel MOSFET has been focused. The proposed models which take the form of the comprehensive analytical expressions have been derived by using the alpha-power law which is more comprehensive than the conventional square law. The up to dated physical level fluctuation model has been adopted as the basis instead of the classical one. So, the model of gate capacitance variation has been refined. These probabilistic models have been verified based on the IBM 90nm RF CMOS technology by using the Monte-Carlo SPICE simulations and the Kolmogorov-Smirnof goodness of fit tests. They are very accurate since they can fit the Monte-Carlo SPICE based data and distributions with 99% confidence. Hence, the proposed models have been found to be the potential mathematical tool for the statistical/variability aware analysis /design of various MOSFET based high frequency applications.

Key-Words: - Gate capacitance, High frequency, MOSFET, Short channel, Statistical design, Transition frequency, Variability aware design.

1 Introduction

Recently, the subthreshold (weak inversion) region MOSFET has been adopted in many high frequency circuits, system and applications such as active inductor, active transformer, high frequency filter, optical front ends, clock/data recovery circuits and Bluetooth devices. Of course, the performances of these high frequency equipments are mainly determined by the high frequency performances of their intrinsic MOSFET which can be determined by two major MOSFET's parameter entitled gate capacitance, C_g and transition frequency f_T.

Obviously, imperfection in MOSFET's properties for example random dopant fluctuation, line edge roughness and gate length random fluctuation cause the random variations in MOSFET's physical parameters such as threshold voltage which are crucial in the statistical/variability aware design of MOSFET based applications. This is because the MOSFET's circuit level parameters such as drain current, I_d and transconductance, g_m are randomly fluctuated due to the cited random variations at the physical level. By this motivation, there are many previous researches on the modeling of such variations in the circuit level parameters for example, [1-4]. The resulting models take the form of the comprehensive analytical expressions which have been found to be the convenient mathematical tools for the statistical/variability aware analysis/design of various MOSFET based applications. However, these researches did not mention anything about the variations in C_g and f_T even though they also exist. Furthermore, such C_g and f_T greatly determine the high frequency performances of the MOSFET as mentined above. So, it can be seen that these previous models lack of some important information for high frequency applications.

Fortunately, there are previous studies in the characteristics of random variations in both C_g and f_T for example [5-7] etc. The results of these previous studies are the graphical plots and numerical measurement of such variations. Unfortunately, such results are not generic since they are obtained from a certain technological basis. Furthermore, none of any related comprehensive analytical expressions that display the variation characteristics of both C_g and f_T has been derived. However, it has been pointed out in [7] that random dopant fluctuation and process variation effects such as line edge roughness and gate length random fluctuation are the major causes of random

variations in high ftrequency characteristics of MOSFET including C_g and f_T. In [8], simple formulas on f_T and the relationship between the variance of C_g and that of f_T have been given. Unfortunately, these formulas are incomprehensive since they do not display the physical level variation causes and their relationships with the resulting variations in C_g and f_T. According to the importance of both C_g and f_T along with their possibility to be randomly fluctuated as mentioned above, the comprehensive analytical modeling of their variations similarly to the modeling of the other parameters proposed in the previous researches such as [1-4], must be urgently performed.

Fortunately, the cited comprehensive analytical model of random variation in C_g has been proposed in [9]. However, this model has been derived based on the classical model of variation [10] which is being replaced by the state of the art ones such as that proposed in [11], so, a refinement is necessary. Furthermore, the similar modeling on f_T which is as important as that of C_g has not been performed yet. Hence, due to the above motivation, the probabilistic models of random variations in MOSFET high frequency performance defined in terms of variations in C_g and f_T have been proposed in this research. Both random dopant fluctuation and process variation effects which are the major causes of the random viriations in the MOSFET's high frequency characteristics as stated in [7], have been taken into account. The short channel MOSFET has been focused since it reigns the universe of the CMOS technology nowadays. The proposed models which take the form of the comprehensive analytical expressions have been derived by using the alpha-power law [12] which is more comprehensive than the conventional square law. This alpha-power law has also been previously adopted in [1], [4] and [9]. The up to dated physical level fluctuation model proposed in [11] has been adopted as the basis instead of the classical one proposed in [10] which has been adopted in [9] as aforementioned. So, the model of variation in C_g has been refined. The proposed models have been verified by using the Monte-Carlo SPICE simulations based on the IBM 90nm RF CMOS process technology and the Kolmogorov-Smirnof goodness of fit tests. The verifications have been performed based on both NMOS and PMOS technologies. These models are very accurate since they can fit the Monte-Carlo SPICE based data and distributions with 99% confidence. Hence, the proposed models have been found to be the potential mathematical tool for the statistical/variability aware analysis/design of various MOSFET based high frequency applications.

2 The Proposed Model

In this section, the proposed models will be discussed. Before proceeds further, it is worthy to give some foundation on the alpha-power law of MOSFET's characteristic. According to [1], [4], [9] and [12], this law which is more comprehensive than the classical square law stated that I_d can be given by

$$I_d = \frac{\mu}{2} C_{ox} \frac{W}{L} (1 + \lambda V_{ds})(V_{gs} - V_t)^{\alpha} \quad (1)$$

where μ, C_{ox}, V_t, α and λ denote the carrier mobility, the gate oxide capacitance of the transistor, practical thresold voltage which is affected by random dopant fluctuation and process variation, velocity saturation index [12] and channel length modulation parameter respectively.

With such I_d, the alpha-power law based g_m is

$$g_m = \alpha \frac{\mu}{2} C_{ox} \frac{W}{L} (1 + \lambda V_{ds})(V_{gs} - V_t)^{\alpha - 1} \quad (2)$$

At this point, the derivation of the proposed model can be started. Firstly, the analytical expression of C_g has been derived. Similarly to [9] and according to [13], C_g can be given by

$$C_g = \frac{dQ_g}{dV_{gs}} \quad (3)$$

where Q_g denotes the gate charge [13]. As in [9], according to [14], Q_g can be given by

$$Q_g = \frac{\mu W^2 L C_{ox}^2}{I_d} \int_0^{Vgs-Vt} (V_{gs} - V_c - V_t)^2 dV_c - Q_{B,\max} \quad (4)$$

where $Q_{B,max}$ denotes the maximum bulk charge [14]. By using (1) and (4), alpha-power law based Q_g is [9]

$$Q_g = \frac{2}{3} \frac{WL^2 (V_{gs} - V_t)^{3-\alpha}}{1 + \lambda V_{ds}} - Q_{B,\max} \quad (5)$$

So, C_g can be given by using (3) and (5) as follows [9]

$$C_g = \frac{2}{3} \frac{WL^2 (3 - \alpha)(V_{gs} - V_t)^{2-\alpha}}{1 + \lambda V_{ds}} \quad (6)$$

Hence, the alpha-power law based f_T can be given by using (2) and (6) as

$$f_T = \frac{3}{8\pi}\frac{\alpha\mu C_{ox}(1+\lambda V_{ds})^2(V_{gs}-V_t)^{2\alpha-3}}{(3-\alpha)L^3} \quad (7)$$

By taking both random dopant fluctuation which is assumed that it gives the number of dopant atoms that obeys the Poisson distribution [15], and process variation effects into account, the variations in MOSFET's properties existed. These fluctuations include the random variations in both C_g and f_T [7]. Such variations are denoted by ΔC_g and Δf_T respectively. Of course, both C_g and f_T become randomly varied due to these variations which can be defined as follows

$$\Delta C_g = C_g - C_{g,Nom} \quad (8)$$

and

$$\Delta f_T = f_T - f_{T,Nom} \quad (9)$$

So, it can be seen that these variations can be defined in terms of the different between their actual randomly varied values and their corresponding nominal counterparts denoted by $C_{g,Nom}$ and $f_{T,Nom}$ respectively. These nominal values which can be ideally obtained by neglecting all imperfections of the MOSFET are obviously deterministic. With (6)-(9), ΔC_g and Δf_T can be given as follows

$$\Delta C_g = \frac{2}{3}\frac{WL^2[(V_{gs}-V_t)^{2-\alpha}-(V_{gs}-V_{TH})^{2-\alpha}]}{(1+\lambda V_{ds})(3-\alpha)^{-1}} \quad (10)$$

and

$$\Delta f_T = \frac{3}{8\pi}\frac{\alpha\mu C_{ox}[(V_{gs}-V_t)^{2\alpha-3}-(V_{gs}-V_{TH})^{2\alpha-3}]}{(1+\lambda V_{ds})^{-2}(3-\alpha)L^3} \quad (11)$$

where V_{TH} denotes the nominal threshold voltage.

By using the state of the art model of physical level variation proposed in [11] and the principle of random variable transformation with (10) and (11) as mapping functions, the probability density functions of ΔC_g and Δf_T can be derived with the emphasis on the short channel MOSFET. These probability density functions are

$$pdf_{\Delta Cg}(\delta C_g) = \frac{3\sqrt{3}\varepsilon_{ox}(1+\lambda V_{ds})(V_{gs}-V_{TH})^{\alpha-1}}{2\sqrt{2\pi}T_{INV}qW^{0.5}L^{1.5}\sqrt{N_{sub}W_{dep}}(2-\alpha)(3-\alpha)^2} \times \exp\left[-\frac{27\varepsilon_{ox}^2(1+\lambda V_{ds})^2(V_{gs}-V_{TH})^{2\alpha-2}\delta C_g^2}{8qT_{INV}^2N_{sub}W_{dep}WL^3(2-\alpha)^2(3-\alpha)^2}\right] \quad (12)$$

and

$$pdf_{\Delta fT}(\delta f_T) = \frac{8\sqrt{3\pi}\varepsilon_{ox}W^{0.5}L^{3.5}(3-\alpha)}{[3\sqrt{2}\mu C_{ox}qT_{INV}(1+\lambda V_{ds})^2(V_{gs}-V_{TH})^{2(\alpha-2)} \times\sqrt{N_{sub}W_{dep}}\alpha|3-2\alpha|]} \times\exp\{-\frac{96\pi^2\varepsilon_{ox}^2WL^7(3-\alpha)^2\delta f_T^2}{[9\mu^2C_{ox}^2q^2T_{INV}^2N_{sub}W_{dep} \times(1+\lambda V_{ds})^4(V_{gs}-V_{TH})^{4(\alpha-2)}\alpha^2|3-2\alpha|^2]}\} \quad (13)$$

where δC_g, δf_T, q, ε_{ox}, N_{sub}, T_{INV}, W, W_{dep} and L denote any sampled value of ΔC_g, that of Δf_T, electron charge, gate oxide permittivity, channel impurity concentration, electrical gate dielectric thickness, channel width, depletion width and channel length respectively [11].

Hence, it can be stated that the proposed model which probabilistically describes the random dopant fluctuation and process variation effects induced random variation in C_g and the similar variation in f_T can be given by (12) and (13) which many physical parameters have been incorporated. At this point, the probabilistic models of random variations in MOSFET's high frequency performance which can be defined in terms of variations in C_g and f_T have been derived in the form of the probability density functions which are the comprehensive analytical expressions including many physical level parameters. Compared to the previous studies such as those in [5-7] which presents the study results of variation in C_g in terms of graphical plots and numerical measurements obtained from a certain technological basis, the proposed model is a more analytic, comprehensive and generic result as it is an analytical expression in term of many physical variables without any reference to a certain technology node but to the general CMOS technology. These models are more comprehensive than that proposed in [8] as they contain several physical level parameters so, the physical causes of such high frequency performance variation have been revealed. This clarifies the exploration of the cited high frequency performance variation. These models are also as comprehensive as those in [2] and [3] but they emphasize on the high frequency operation. Finally, the proposed models are more complete and up to dated than that proposed in [9] which mention nothing on the variation in f_T, and also relies on the outdated physical level fluctuation model [10]. For fitting of the variation in C_g, part of the proposed models for this variation is more accurate than that mentioned in [9] due to the better Kolmogorov-Smirnof test statistic obtained from the

data fitting using a part of the proposed ones as will be seen later.

As this model takes the form of the probability density function, much meaningful statistical information of the variations in C_g and f_T can be obtained. For examples, it can be seen that both variations in C_g and f_T have the following means and variances

$$\overline{\Delta C_g} = \int_{-\infty}^{\infty} \delta C_g \, pdf_{\Delta C_g}(\delta C_g) d\delta C_g = 0 \tag{14}$$

$$\begin{aligned}\sigma^2_{\Delta Cg} &= \int_{-\infty}^{\infty} \left(\delta C_g - \overline{\Delta C_g}\right)^2 pdf_{\Delta C_g}(\delta C_g) d\delta C_g \\ &= \frac{4qT^2_{INV} N_{sub} W_{dep} WL^3 (2-\alpha)^2 (3-\alpha)^2}{27\varepsilon^2_{ox}(1+\lambda V_{ds})^2 (V_{gs}-V_{TH})^{2\alpha-2}}\end{aligned} \tag{15}$$

and

$$\overline{\Delta f_T} = \int_{-\infty}^{\infty} \delta f_T \, pdf_{\Delta fT}(\delta f_T) d\delta f_T = 0 \tag{16}$$

$$\begin{aligned}\sigma^2_{\Delta fT} &= \int_{-\infty}^{\infty} \left(\delta f_T - \overline{\Delta f_T}\right)^2 pdf_{\Delta f_T}(\delta f_T) d\delta f_T \\ &= \frac{9\mu^2 C^2_{ox} q^2 T^2_{INV} N_{sub} W_{dep} \alpha^2 |3-2\alpha|^2 (1+\lambda V_{ds})^4}{192\pi^2 \varepsilon^2_{ox} WL^7 (3-\alpha)^2 (V_{gs}-V_{TH})^{4(2-\alpha)}}\end{aligned} \tag{17}$$

where $\overline{\Delta C_g}$, $\sigma^2_{\Delta Cg}$, $\overline{\Delta f_T}$, and $\sigma^2_{\Delta fT}$ denote mean and variance of C_g along with those of f_T respectively. Furthermore, the analytical expressions of many other meaningful statistical parameters such as moments of various orders, skewness and kurtosis can also be obtained by simply apply the conventional mathematical statistic to the proposed model with the required mathematics can be performed even by hand calculation. These are the major benefits of this model. For the desinging with electronic CAD tools, this model can serves as the mathematical basis for the desired simulations. The required computational effort is potentially smaller than that of the brute force Monte-Carlo analysis based on the random variations of the parameters at the physical level which is time expensive as mentioned in [16]. Hence, the proposed models have been found to be the potential mathematical tool for the statistical/variability aware analysis/design of various MOSFET based high frequency applications. In the subsequent section, the verification of the proposed model will be discussed.

3 The Verification

Similarly to [2, 3, 9], the verification of the proposed model has been performed in both qualitative and quantitative aspects. In the qualitative sense, the estimated distributions of random variations in C_g and f_T obtained from the models have been graphically compared to their counterparts obtained from the Monte-Carlo SPICE simulations of the benchmark circuits. On the other hand for the quantitative point of view, numbers of Kolmogorov-Smirnof goodness of fit test (KS-test) have been performed by using the cumulative distributions of such random variations obtained from the same set of Monte-Carlo SPICE simulations for the qualitative verifications. It should be mentioned here that both NMOS and PMOS technologies have been considered. The verification has been performed based on the up to dated IBM 90nm RF CMOS technology by the model parameterization with the IBM 90nm RF CMOS process parameters and the usage of the BSIM4.3 based benchmark circuits parameterized by the SPICE parameters extracted from such IBM 90nm RF CMOS process. These necessary parameters are provided by the MOSIS.

Since the KS-test relies on the cumulative distributions, it is worthy to derive the cumulative distribution function forms of the proposed models at this point. With the conventional mathematical statistic, they can be given by

$$\begin{aligned}CDF_{\Delta C_g}(\delta C_g) &= \int_{-\infty}^{\delta C_g} pdf_{\Delta C_g}(u) du \\ &= \frac{1}{2}\left\{1 + erf\left[\left[\frac{8qT^2_{INV} N_{sub} W_{dep} WL^3 (2-\alpha)^2 (3-\alpha)^2}{27\varepsilon^2_{ox}(1+\lambda V_{ds})^2 (V_{gs}-V_{TH})^{2\alpha-2}}\right]^{-\frac{1}{2}} \delta C_g\right]\right\}\end{aligned} \tag{18}$$

and

$$\begin{aligned}CDF_{\Delta f_T}(\delta f_T) &= \int_{-\infty}^{\delta f_T} pdf_{\Delta f_T}(u) du \\ &= \frac{1}{2}\left\{1 + erf\left[\left[\frac{9\mu^2 C^2_{ox} q^2 T^2_{INV} N_{sub} W_{dep} \alpha^2 |3-2\alpha|^2 (1+\lambda V_{ds})^4}{96\pi^2 \varepsilon^2_{ox} WL^7 (3-\alpha)^2 (V_{gs}-V_{TH})^{4(2-\alpha)}}\right]^{-\frac{1}{2}} \delta f_T\right]\right\}\end{aligned} \tag{19}$$

Note that $erf(x)$ denotes the error function of any arbitrary variable, x which can be mathematically defined as

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x \exp(-u^2) du. \tag{20}$$

According to [17, 18], the strategy of the KS-test is to performed the comparison of the K-S test statistic (KS) and the critical value (c) where it can be stated that any model fits its target data set if and only if its KS is not exceed its c [17, 18]. For this research, KS can be defined as

$$KS = \max_{\delta x}\{\left|CDF_{\Delta x}(\delta x)\right|_{circuit}\right| - \left|CDF_{\Delta x}(\delta x)\right|_{model}\right|\} \quad (21)$$

where x can be either C_g or f_T while $CDF_{\Delta x}(\delta x)\big|_{model}$ and $CDF_{\Delta x}(\delta x)\big|_{circuit}$ represent the cumulative distribution of any x obtained from the proposed models and the counterpart obtained from the simulation of the benchmark circuit respectively. Furthermore, as the confidence level of the test is 99%, c can be given by [18]

$$c = \frac{1.63}{\sqrt{n}} \quad (22)$$

where n denotes the number of runs for the Monte-Carlo SPICE analysis.

Similarly to [9], it should be mentioned here that the model verification has been performed by using n = 3000 which yields c = 0.0297596. In the upcoming subsections, the verification of the model based on NMOS technology and the PMOS counterpart will be respectively discussed.

3.1 NMOS based model verification

As in [9], for the verification the model's accuracy in the prediction of random variation in C_g, the chosen benchmark circuit is a single MOSFET with both drain and source have been ac grounded where as the gate terminal has been fed by the ac input voltage. The input admittance which takes C_g into account can be seen by looking into the input terminal of this benchmark circuit. This methodology of finding the MOSFET's input admittance by using SPICE analysis has also been used in [19]. For NMOS technological basis, the core of this circuit can be depicted in Fig.1. As the input conductance is extremely small for conventional MOSFETs, C_g can be approximately given as follows [9]

$$C_g = \frac{Y_{in}}{j\omega} = \frac{1}{j\omega}\frac{I_{in}}{V_{in}} \quad (23)$$

where Y_{in}, I_{in} and V_{in} denote the input admittance, input current and input voltage respectively. Similarly to [9], the variation in the formerly defined C_g above obtained from the Monte-Carlo SPICE simulation of this circuit at 1 GHz has been adopted as the circuit based ΔC_g for NMOS technology.

On the other hand, the chosen benchmark circuit for verifying the model's accuracy in the prediction of random variation in f_T is also a single MOSFET but both drain and gate have been fed with their own ac voltages where as the source terminal has been ac grounded. These ac voltages applied at the gate and drain are V_{gs} and V_{ds} respectively. For NMOS technological basis, the core of this circuit can be depicted in Fig.2. From this circuit, f_T can be defined as the frequency which the current gain is unity. Alternatively, it is the frequency which the magnitude of the small signal input current is equal to that of the output one. This methodology has also been adopted in finding f_T of EPC's enhancement mode GaN power transistor with SPICE simulation [20]. Of course, the corresponding variation in f_T obtained from the Monte-Carlo SPICE simulation of this circuit has been adopted as the circuit based Δf_T for NMOS technology. It should be mentioned here that these benchmark circuit uses the nominal channel length (L) of 100nm which is closed to the minimum allowable value along with the nominal aspect ratio (W/L) of 50. For both circuits, the dc supplies of ±0.5 v have been used. Finally, these simulation strategies, parameters setting and biasing condition have been used for the PMOS based model verification.

By proceed in the similar manner to the model verifications in [2, 3, 9], the graphical comparisons for the distributions ΔC_g and Δf_T with respected to their nominal values, denoted by $\Delta C_g/C_{g,Nom}$ and $\Delta f_T/f_{T,Nom}$ respectively are depicted in Fig. 3 and Fig.4 for the qualitative NMOS based verification. For this NMOS case, it can be seen that strong agreements between the predicted distributions obtained from the proposed model and the counterparts obtained from the Monte-Carlo SPICE analysis of the benchmark circuits can be observed. Hence, proposed model has been qualitatively verified as highly accurate for NMOS technology.

For the quantitative verification, it can be seen by using (19) that the resulting KS for $x = C_g$ can be found as KS = 0.0246539 and that for $x = f_T$ is KS = 0.0297046 which are both smaller than c = 0.0297596. This means that the proposed model can fit the variations in C_g and f_T obtained from the NMOS based benchmark circuits with 99% confidence. Furthermore, a good agreement can also be seen from the comparative plots for the cumulative distributions of $\Delta C_g/C_{g,Nom}$ and $\Delta f_T/f_{T,Nom}$ depicted in Fig.5 and Fig.6 respectively. At this

point, the proposed model verified as highly accurate for NMOS technological basis.

3.2 PMOS based model verification

For the model verification based on PMOS technology, the benchmark circuits similarly to those depicted in Fig.1 and Fig.2 can be used. These circuits can be depicted in Fig.7 and Fig.8 which are adopted for verifying the model's accuracy to predict the variation C_g and the accuracy for the prediction of such variation in f_T respectively. It should be mentioned here that C_g, f_T and their variations in this case can be determined from the benchmark circuits in the similar manner to those of the NMOS based verification. Furthermore, the similar verification methodology, parameters setting and biasing condition applied to the previous NMOS based scenario can also be used for this PMOS based case.

Also similarly to the NMOS based case, the graphical comparisons for the distributions of $\Delta C_g/C_{g,Nom}$ and $\Delta f_T/f_{T,Nom}$ respectively are depicted in Fig.9 and Fig.10 for the qualitative PMOS based verification which strong agreements between those obtained from the proposed model and the counterparts obtained from the Monte-Carlo SPICE analysis of the benchmark circuits has also been observed. Hence, proposed model has been qualitatively verified as highly accurate for PMOS technology.

For the quantitative verification, it can be seen that KS for $x = C_g$ can be found as KS = 0.0081163 and that for $x = f_T$ is KS = 0.0294916 which are also smaller than c = 0.0297596. This means that the proposed model can fit the variations in C_g and f_T obtained from the PMOS based benchmark circuits with 99% confidence. Similarly to the NMOS based case, a good agreement can also be seen from the comparative plots for the cumulative distributions of $\Delta C_g/C_{g,Nom}$ and $\Delta f_T/f_{T,Nom}$ depicted in Fig.11 and Fig.12 respectively. At this point, the proposed model is verified as also highly accurate for PMOS technology.

Before leaving this section, it should be mentioned here that the resulting KS statistics for the model of variation in C_g proposed in this research given by KS = 0.0246539 for the NMOS based verification and KS = 0.0081163 for the PMOS based one as mentioned above are lower than their corresponding counterparts formerly proposed in [9] given by KS = 0.0267486 and KS = 0.0090026 for NMOS based data fitting and PMOS based one respectively. According to [17, 18], this means that the refined model for the variation of C_g proposed in this research is better fit to both NMOS based data and PMOS based one due to its lower statistics so, it is more accurate than the previous model for the variation in C_g proposed in [9]. This is a result of the refinement in the model for C_g variation.

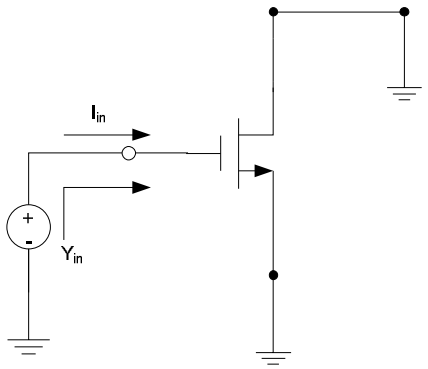

Fig.1. NMOS benchmark circuit for verifying the model of ΔC_g

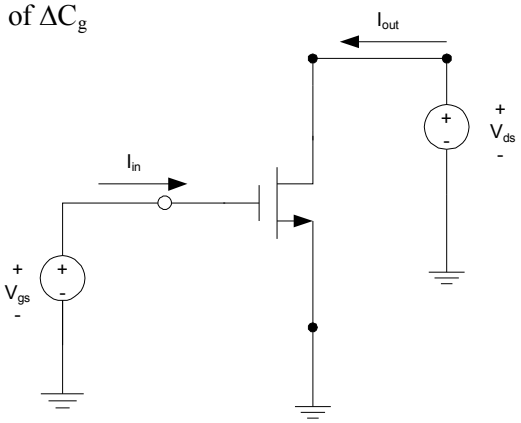

Fig.2. NMOS benchmark circuit for verifying the model of Δf_T

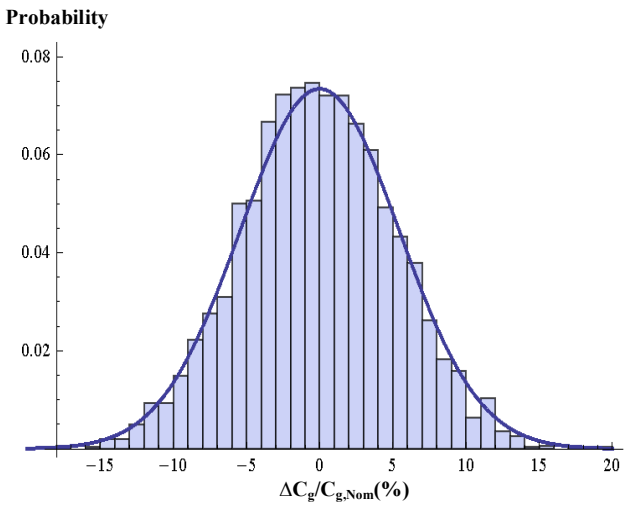

Fig.3. NMOS based comparative distribution plots for $\Delta C_g/C_{g,Nom}$: The model based (line) v.s. The benchmark circuit based (histogram)

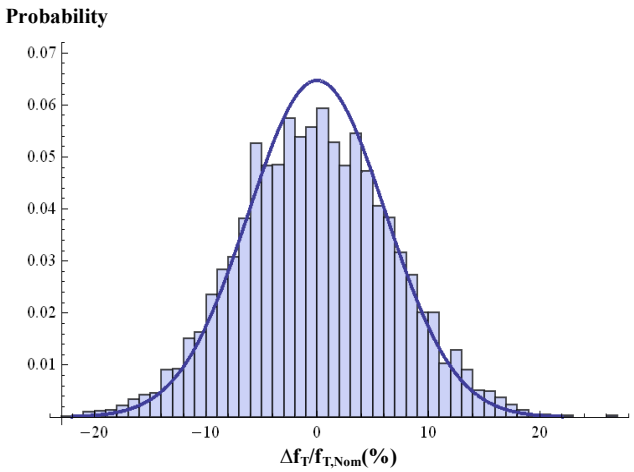

Fig.4. NMOS based comparative distribution plots for $\Delta f_T/f_{T,Nom}$: The model based (line) v.s. The benchmark circuit based (histogram)

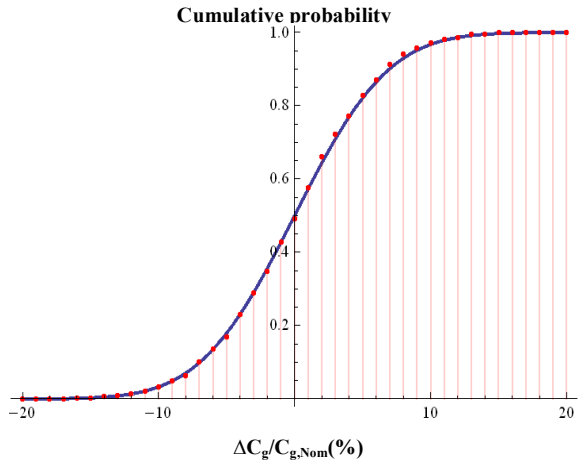

Fig.5. NMOS based comparative cumulative distribution plots for $\Delta C_g/C_{g,Nom}$: The model based (line) v.s.The benchmark circuit based (dots)

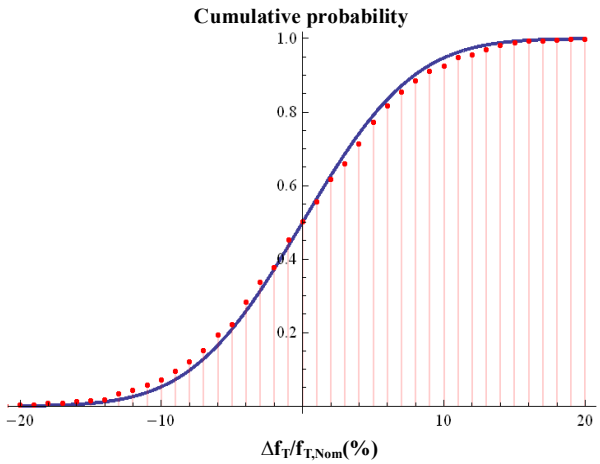

Fig.6. NMOS based comparative cumulative distribution plots for $\Delta f_T/f_{T,Nom}$: The model based (line) v.s. The benchmark circuit based (dots)

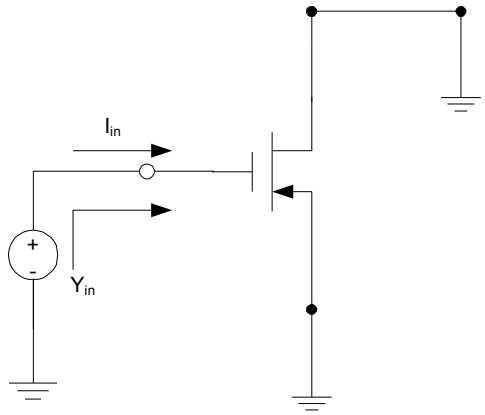

Fig.7. PMOS benchmark circuit for verifying the model of ΔC_g

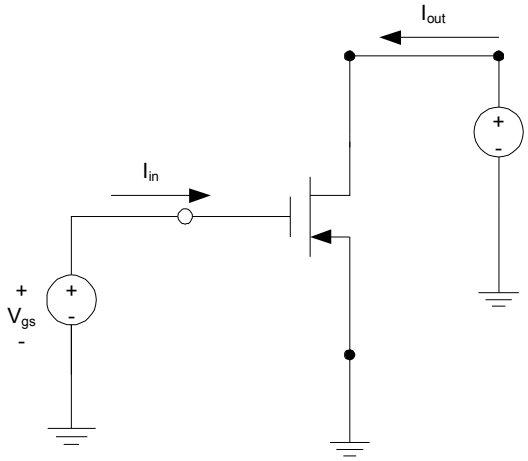

Fig.8. PMOS benchmark circuit for verifying the model of Δf_T

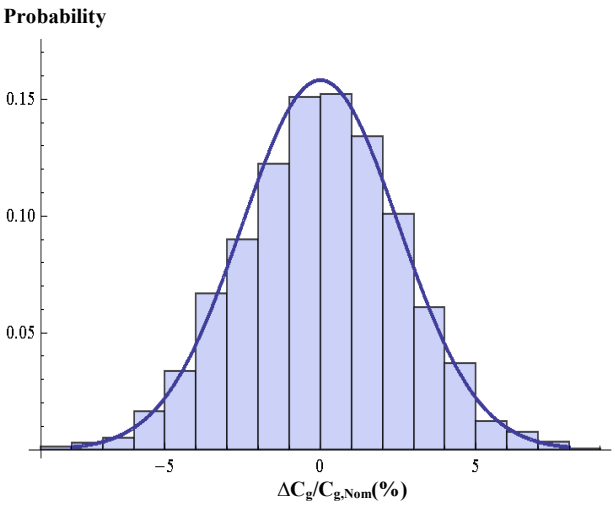

Fig.9. PMOS based comparative distribution plots for $\Delta C_g/C_{g,Nom}$: The model based (line) v.s. The benchmark circuit based (histogram)

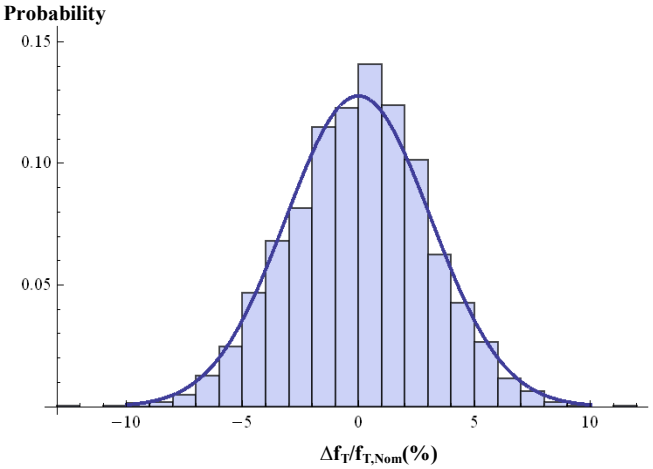

Fig.10. PMOS based comparative distribution plots for $\Delta f_T/f_{T,Nom}$: The model based (line) v.s. The benchmark circuit based (histogram)

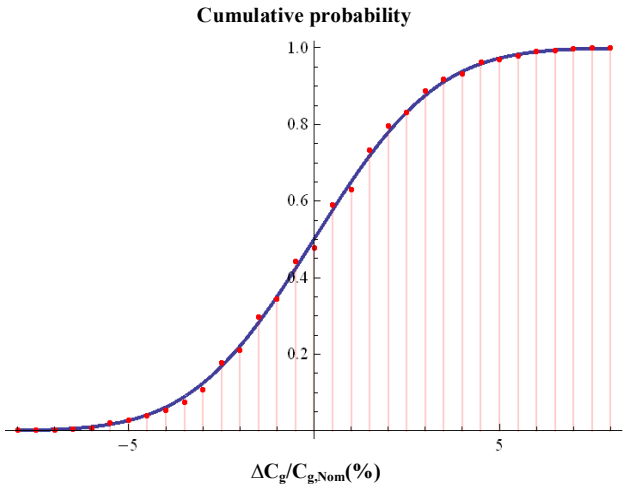

Fig.11. PMOS based comparative cumulative distribution plots for $\Delta C_g/C_{g,Nom}$: The model based (line) v.s. The benchmark circuit based (dots)

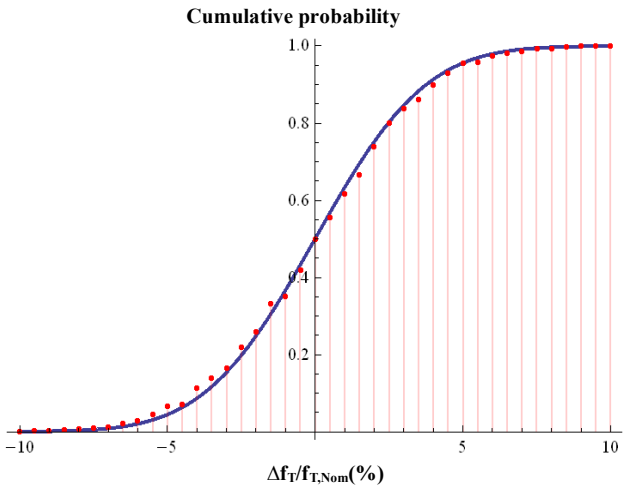

Fig.12. PMOS based comparative cumulative distribution plots for $\Delta f_T/f_{T,Nom}$: The model based (line) v.s. The benchmark circuit based (dots)

4 Discussion

In this section, some discussion regarding to the proposed model, some interesting applications of this model and the results obtained from the model verification will be given. Firstly, it can be obviously seen from the proposed models that many physical level parameters have been incorporated. Since these models describe the behavior of high frequency performance variations and these physical level parameters are depended on the fabrication technology of the MOSFET, it can be seen that such technology significantly affects the high frequency performance variation.

As mentioned above, C_g and f_T become randomly varied due to ΔC_g and Δf_T. Mathematically, they become random variables. By using (8), (9) and the proposed models, their probability density functions can be simply derived as follows

$$pdf_{C_g}(c_g)=\frac{3\sqrt{3}\varepsilon_{ox}(1+\lambda V_{ds})(V_{gs}-V_{TH})^{\alpha-1}}{2\sqrt{2\pi}T_{INV}qW^{0.5}L^{1.5}\sqrt{N_{sub}W_{dep}}(2-\alpha)(3-\alpha)^2} \times\exp\left[-\frac{27\varepsilon_{ox}^2(1+\lambda V_{ds})^2(V_{gs}-V_{TH})^{2\alpha-2}(c_g-C_{g,Nom})^2}{8qT_{INV}^2N_{sub}W_{dep}WL^3(2-\alpha)^2(3-\alpha)^2}\right] \quad (24)$$

and

$$pdf_{fT}(\phi_T)=\frac{8\sqrt{3\pi}\varepsilon_{ox}W^{0.5}L^{3.5}(3-\alpha)}{[3\sqrt{2}\mu C_{ox}qT_{INV}(1+\lambda V_{ds})^2(V_{gs}-V_{TH})^{2(\alpha-2)} \times\sqrt{N_{sub}W_{dep}}\alpha|3-2\alpha|] \times\exp\{-\frac{96\pi^2\varepsilon_{ox}^2WL^7(3-\alpha)^2(\phi_T-f_{T,Nom})}{[9\mu^2C_{ox}^2q^2T_{INV}^2N_{sub}W_{dep} \times(1+\lambda V_{ds})^4(V_{gs}-V_{TH})^{4(\alpha-2)}\alpha^2|3-2\alpha|^2]}\} \quad (25)$$

where c_g and $_T$ denotes any sample values of C_g and f_T respectively.

Furthermore, it can be observed from (15) and (17) which have been derived from the proposed model that

$$\sigma^2_{\Delta Cg} \propto WL^3 \quad (26)$$

$$\sigma^2_{\Delta Cg} \propto \frac{1}{(1+\lambda V_{ds})^2} \quad (27)$$

$$\sigma^2_{\Delta fT} \propto \frac{1}{WL^7} \quad (28)$$

and $$\sigma^2_{\Delta fT} \propto (1+\lambda V_{ds})^4 \quad (29)$$

So, it can be seen that shriking the transistor dimension can reduce the variation in C_g with

increasing of variation in f_T as a penalty. Furthermore, application of the trendy low voltage designing methodology which uses low supply voltage yields the reduction in f_T variation with increasing in C_g variation as a price to pay. So, these trade-off issues must be taken into account in the designing of MOSFET based high frequency applications.

For the in depth exploration of the statistical relationship between the variation in C_g and the one in f_T, their correlation coefficient denoted by $\rho_{\Delta Cg,\Delta fT}$ must be investigated. Such $\rho_{\Delta Cg,\Delta fT}$ can be defined as

$$\rho_{\Delta Cg,\Delta fT} = \frac{E[(\Delta C_g - \overline{\Delta C_g})(\Delta f_T - \overline{\Delta f_T})]}{\sqrt{\sigma^2_{\Delta Cg}}\sqrt{\sigma^2_{\Delta fT}}} \quad (30)$$

where $E[(\Delta C_g - \overline{\Delta C_g})(\Delta f_T - \overline{\Delta f_T})]$ is the covariance of both variations denoted by $Cov(\Delta C_g, \Delta f_T)$ which in turn can be defined as

$$\begin{aligned} Cov(\Delta C_g, \Delta f_T) &= E[(\Delta C_g - \overline{\Delta C_g})(\Delta f_T - \overline{\Delta f_T})] \\ &= \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(\delta C_g - \overline{\Delta C_g})(\delta f_T - \overline{\Delta f_T})\, pdf_{\Delta Cg,\Delta fT}(\delta C_g, \delta f_T)\, d\delta C_g\, d\delta f_T \end{aligned} \quad (31)$$

and $pdf_{\Delta Cg,\Delta fT}(\delta C_g, \delta f_T)$ which denotes the joint probability density function of both variations can be found from the proposed model by solving the following equations

$$pdf_{\Delta Cg}(\delta C_g) = \int_{-\infty}^{\infty} pdf_{\Delta Cg,\Delta fT}(\delta C_g, \delta f_T)\, d\delta f_T \quad (32)$$

$$pdf_{\Delta fT}(\delta f_T) = \int_{-\infty}^{\infty} pdf_{\Delta Cg,\Delta fT}(\delta C_g, \delta f_T)\, d\delta C_g \quad (33)$$

By using the proposed model along with (14)-(17) which are obtained from this model for $\overline{\Delta C_g}$, $\sqrt{\sigma^2_{\Delta Cg}}$, $\overline{\Delta f_T}$, and $\sqrt{\sigma^2_{\Delta fT}}$ respectively, the magnitude of such correlation coefficient has been found to be unity. This means that there exists a very strong statistical relationship between both variations.

Secondly, apart from obtaining meaningful statistical parameters of ΔC_g and Δf_T as formerly mentioned, the proposed model can serve as a basis for understanding the behavior of the similar variations in other high frequency parameters. For example, the behavior for such variation in the maximum oscillation frequency which is also an important high frequency parameter can be precisely understood by using the proposed model since such frequency is a function of f_T. This point can be demonstrated as follows, the maximum oscillation frequency denoted by f_{max} is a critical high frequency parameter when the gate parasitic resistance has been taken into account. Let such gate parasitic resistance be denoted by R_g, f_{max} can be given as a function of f_T as follows

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{dg} R_g}} \quad (34)$$

where C_{dg} denotes the capacitance from drain to gate which is totally differrent from that from gate to drain denoted by C_{gd} [21]. The reason for this is that C_{dg} and C_{gd} can be given according to [21] by

$$C_{dg} = -\frac{\partial Q_d}{\partial V_g} \quad (35)$$

and

$$C_{gd} = -\frac{\partial Q_g}{\partial V_d} \quad (36)$$

Note that Q_d denotes the drain charge where as V_g and V_d denote the gate and drain voltages respectively [21]. It can be obviously seen from (35) and (36) that $C_{dg} \neq C_{gd}$.

Since Δf_T is undeniably arised due to both random dopant fluctuation and process variation effects, the maximum oscillation frequency can be practically given by

$$f_{\max}(\Delta f_T) = \sqrt{\frac{f_{T,Nom} + \Delta f_T}{8\pi C_{dg} R_g}} \quad (37)$$

where, $f_{\max}(\Delta f_T)$ denotes such practical maximum oscillation frequency which is undeniably fluctuated according to Δf_T induced by random dopant fluctuation and process variation effect while $f_{T,Nom}$ denotes the nominal value of f_T. So, the random variation in the square of such f_{max} denoted by $\Delta f^2_{\max}$ can be simply found as

$$\Delta f^2_{\max} = \frac{\Delta f_T}{8\pi C_{dg} R_g} \quad (38)$$

By using (17) which obtained from the proposed model, the variance of $\Delta f^2_{\max}$ can be simply given by

$$Var[\Delta f_{\max}^2] = \frac{9\mu^2 C_{ox}^2 q^2 T_{INV}^2 N_{sub} W_{dep} \alpha^2 |3-2\alpha|^2 (1+\lambda V_{ds})^4}{12288\pi^4 C_{dg}^2 R_g^2 \varepsilon_{ox}^2 WL^7 (3-\alpha)^2 (V_{gs}-V_{TH})^{4(2-\alpha)}} \quad (39)$$

Hence, it can be seen at this point that the behavior of random variation in f_{max} is now well understood via the above information on the variation of $\Delta f_{\max}^2$ which has been obtained by using the proposed model. For obtaining an in depth insight, the probability density function of $f_{\max}(\Delta f_T)$ denoted by $pdf(\phi_{\max})$ which completely describes the fluctuation in the maximum oscillation frequency analytically, can also be obtained by using the proposed model. Let $\phi_{\max}$ denotes any sampled value of $f_{\max}(\Delta f_T)$, by using the principle of random variable transformation with (37) as a mapping function, $pdf(\phi_{\max})$ can be given by

$$pdf(\phi_{\max}) = 16\sqrt{\frac{\pi}{2}} \frac{C_{dg} R_g \phi_{\max}}{\sqrt{\sigma_{\Delta fT}^2}} \exp[-\frac{(\phi_{\max}^2 - f_{T,Nom})/8\pi C_{dg} R_g}{2(\sqrt{\sigma_{\Delta fT}^2}/8\pi C_{dg} R_g)^2}] \quad (40)$$

where $\sqrt{\sigma_{\Delta fT}^2}$ can be found by using (17) which can be obtained from the proposed model. At this point, it can be obviously seen that $pdf(\phi_{\max})$ which describes the fluctuation in the maximum oscillation frequency, can be simply obtained by using the proposed model.

Furthermore, the proposed model is applicable as the mathematical foundation for the modeling of the high frequency performance mismatch of the globally spaced MOSFETs for example, the mismatch in C_g and f_T of such spaced devices. Let these mismatches be denoted by DC_g and Df_T respectively. Since these transistors have similar local variations and low correlation as they are globally spaced, the distributions of DC_g and Df_T can be simply given by using the proposed model as follows

$$pdf_{DCg}(dC_g) = \frac{3\sqrt{3}\varepsilon_{ox}(1+\lambda V_{ds})(V_{gs}-V_{TH})^{\alpha-1}}{4\sqrt{\pi} T_{INV} q W^{0.5} L^{1.5} \sqrt{N_{sub} W_{dep}} (2-\alpha)(3-\alpha)^2} \times \exp\left[-\frac{27\varepsilon_{ox}^2 (1+\lambda V_{ds})^2 (V_{gs}-V_{TH})^{2\alpha-2} dC_g^2}{16 q T_{INV}^2 N_{sub} W_{dep} WL^3 (2-\alpha)^2 (3-\alpha)^2}\right] \quad (41)$$

and

$$pdf_{DfT}(df_T) = \frac{4\sqrt{3\pi}\varepsilon_{ox} W^{0.5} L^{3.5} (3-\alpha)}{[3\mu C_{ox} q T_{INV} (1+\lambda V_{ds})^2 (V_{gs}-V_{TH})^{2(\alpha-2)} \times \sqrt{N_{sub} W_{dep}} \alpha |3-2\alpha|]} \times \exp\{-\frac{48\pi^2 \varepsilon_{ox}^2 WL^7 (3-\alpha)^2 df_T^2}{[9\mu^2 C_{ox}^2 q^2 T_{INV}^2 N_{sub} W_{dep} \times (1+\lambda V_{ds})^4 (V_{gs}-V_{TH})^{4(\alpha-2)} \alpha^2 |3-2\alpha|^2]}\} \quad (42)$$

where dC_g and df_T denote any sampled values of DC_g and Df_T respectively.

Now, the discussion regarding to the results obtained from the model verification will be given. It can be seen from the formerly shown Monte-Carlo SPICE analysis results that the variations in both gate capacitance and transition frequency follows the Gaussian distribution as depicted in Fig.3, Fig.4, Fig.9 and Fig.10. Similarly to the results proposed in [9], the maximum percentage of variation in C_g denoted by $Max[\Delta C_g/C_g]$ obtained from the NMOS based benchmark circuit for verifying the model of ΔC_g depicted in Fig.1 is higher than its counterparts obtained from the PMOS based one shown in Fig.7. These maximum percentages are similar to those proposed in [9] since they have been generated from the ceteris paribus scenario. Furthermore, the similar relationship can be seen among the maximum percentage of variation f_T denoted by $Max[\Delta f_T/f_T]$ obtained from the NMOS based benchmark circuit for verifying the model of Δf_T shown in Fig.2 and its counterpart obtained from the PMOS based circuit depicted in Fig.8. All of these maximum percentages are concluded in Table I. It can be observed from these percentages that PMOS technology is more robust to the random dopant fluctuation and process variation effects than its NMOS counterpart due to its lower variations. At this point, the validity of the similar conclusion proposed in [9] has been emphasized.

Furthermore, it has been observed that the K-S test statistics for the PMOS based verification are smaller than their NMOS based counterparts as can be seen in Table II. This means that the proposed model is better fit to the PMOS based data than the NMOS based one due to the smaller statisitics. So, it can be seen that this model can predict the variations for PMOS transistor with higher accuracy than the similar prediction for the NMOS one.

Finally, the one of the tentative further researches is to perform the similar modeling with specific orientation to the nanometer level CMOS technology as the modeling for other parameters such as I_d and g_m of the nanoscale MOSFET which have been proposed in [2, 3].

Table 1. Max[$\Delta C_g/C_g$] and Max[$\Delta f_T/f_T$]

Max[$\Delta C_g/C_g$] (%)		*Max[$\Delta f_T/f_T$] (%)*	
NMOS	PMOS	NMOS	PMOS
15.9526	7.5694	20.56	9.37055

Table 2. The comparison of K-S test statistics

From ΔC_g verification		*From Δf_T verification*	
NMOS	PMOS	NMOS	PMOS
0.0246539	0.0081163	0.0297046	0.0294916

6 Conclusion

The probabilistic models of random variations in MOSFET's high frequency performance defined in terms of variations in C_g and f_T have been proposed. Both random dopant fluctuation and process variation effects which are the crucial causes of the MOSFET's high frequency characteristic variations [7] have been taken into account. The state of the art short channel CMOS technology has been focused. These models have been derived by using the alpha-power law which has been proposed in [12] and has also been previously adopted in [1], [4] and [9]. The modern physical level variation model proposed in [11] has been adopted as the modeling basis instead of the classical one in [10]. This gives the significant refinement in the model of variation in C_g compared to the previous one proposed in [9]. The proposed probabilistic models have been verified with both NMOS and PMOS technologies based on the IBM 90nm RF CMOS process by using the Monte-Carlo SPICE simulations along with the KS tests. These models are very accurate since they can fit the Monte-Carlo SPICE based data and distributions with 99% confidence. Hence, the proposed models have been found to be the convenient mathematical tool for the statistical/variability aware analysis/design of various MOSFET based high frequency applications such as active inductor, active transformer, high frequency filter, optical front ends, clock/data recovery circuits and many Bluetooth devices.

Acknowledgement

The author would like to acknowledge Mahodol University, Thailand for online database service.

References:

[1] H. Masuda, T. Kida and S. Ohkawa, "Comprehensive matching characterization of analog CMOS circuits," *IEICE Trans. Fundamental*, Vol. E92-A, No.4, 2009, pp. 966-975.

[2] R. Banchuin, "Process induced random variation models of nanoscale MOS performance: efficient tool for the nanoscale regime analog/mixed signal CMOS statistical/variability aware design," *Proceedings of the 2011 International Conference on Information and Electronic Engineering*, 2011, pp. 6-12

[3] R. Banchuin, "Complete circuit level random variation models of nanoscale MOS performance," *International Journal on Information and Electronic Engineering*, Vol. 1, No.1, 2011, pp. 9-15.

[4] K. Hasegawa, M. Aoki, T. Yamawaki, S. Tanaka, "Modeling transistor variation using a-power formula and its application to sensitivity analysis on harmonic distortion in differential amplifier," *Analog Integrated Circuits and Signal Processing*, 2011.

[5] A. R. Brown and A. Asenov., "Capacitance fluctuations in bulk MOSFETs due to random discrete dopants," *Journal of Computer Electronic (2008)*, Vol.7, 2008, pp. 115-118.

[6] Y. Li and C.H. Hwang, "High-frequency characteristic fluctuations of nano-MOSFET circuit induced by random dopants," *IEEE Transaction on Microwave Theory and Techniques*, Vol. 56, No.12, 2008, pp. 2726-2733.

[7] M.H. Han, Y. Li and C.H. Hwang, "The impact of high-frequency characteristics induced by intrinsic parameter fluctuations in nano-MOSFET device and circuit," *Microelectronics Reliability*, Vol.50, 2010, pp. 657-661.

[8] H.S. Kim, C. Chung, J. Lim, K. Park, H. Oh, and H.K. Kang, "Characterization and modeling of RF-performance (f_T) fluctuation in MOSFETs," *IEEE Electronic Devices Letters*, Vol. 30, No.8, 2009, pp. 855-857.

[9] R. Banchuin, "The novel analytical probabilistic model of random variation in MOSFET's high frequency performance," *Proceedings of the IASTED Asian Conference on Modeling, Identification and Control*, 2012, pp. to be published.

[10] M. J. M. Pelgrom, A. C. J. Duinmaijer, A. P. G.Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, Vol. 24, No.5, 1989, pp. 1433-1440.

[11] K. Takeuchi, A. Nishida and T. Hiramoto, "Random fluctuations in scaled MOS Devices," *Proceedings of the 2009 International Conference on Simulation of Semiconductor Processes and Devices*, 2009, pp. 79-85.

[12] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE Journal on Solid-State Circuits*, Vol. 25, No.2, 1990, pp. 584-594.

[13] H. Abebe, H. Morris, E. Cumberbatch and V. Tyree, "Compact gate capacitance model with polysilicon depletion effect for MOS device," *Journal of Semiconductor Technology and Science,* Vol 7, No.3, 2007, pp. 131-135.

[14] R.T. Howe and C. G. Sodini, *Microelectronics: An Integrated Approach*, Prentice Hall, 1996.

[15] L. Weifeng and S. Lingling, "Modeling of current mismatch induced by random dopant fluctuation in nano-MOSFETs," *Journal of Semiconductor*, Vol. 32, No.8, 2011, pp. 084003-1-084003-5.

[16] G. Cijan, T. Tuma and A. Burmen, "Modeling and simulation of MOS transistor mismatch," *Proceedings of the 6th Eurosim Congress on Modelling and Simulation* , 2007, pp. 1-8

[17] T. Altiok and B. Melamed, *Simulation Modeling and Analysis with ARENA*, Academic Press, 2007.

[18] S.A. Klugman, H.H Panjer and G.E. Willmot, *Loss Models: From Data to Decisions*, Wiley, 2008

[19] C-H Choi, J.S. Goo, T.Y. Oh, R.W. Dutton, A. Bayoumi, M. Cao, P.V. Voorde, D. Vook and C.H. Diaz, "MOS C-V characterization of ultrathin gate oxide thickness (1.3-1.8 nm)," *IEEE Electronic Devices Letters*, Vol. 20, No.6, 1999, pp. 292-264.

[20] R. Beach, A. Babakhani and R. Strittmatter, "Circuit simulation using EPC device models," *Application notes: Circuit Simulation, Device Models*, 2011, pp. 1-12.

[21] D.L. Pulfrey, *Understanding Modern Transistors and Diodes*, Cambridge University press, 2010