Design of Low Power Full Adder Using Active Level Driving Circuit

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Abstract :- CMOS technology is approaching the nano-electronics range nowadays, but experiences some practical limits. High dynamic power dissipation and leakage current in deep submicron technologies contribute a major proportion of total power dissipation in CMOS circuits designed for portable applications. Consequently, identification and modeling of different components is very important for estimation and reduction of power dissipation in scaled CMOS circuits, especially for low power applications. As full adder (FA) forms one of the important unit of digital signal processing architecture , its design implementation is considered. The logic styles used in the design of CMOS full adder circuit have many limitations in terms of power and number of transistors.

Pseudo NMOS-PT adder is designed with carry block in Pseudo NMOS logic for reducing dynamic power dissipation and sum block in pass transistor logic for reducing gate count. An Active Level Driving Circuit(ALDC) is proposed for driving the level restoring weak PMOS pull-up transistor. ALDC charges the gate of pull up PMOS transistor to V_{dd} for active low outputs, turning it to OFF . This reduces the leakage power dissipation thereby decreasing the total power dissipation. The proposed adder is designed using Tanner 7.0 and simulated using TSPICE. Fabrication technology used is 180nm. Performance analysis reveals that the proposed adder design fairs better than conventional static CMOS, CPL, CMOS-BBL and BBL-PT adders in terms of power, delay and power delay product (PDP). Design implementation with Carry Select Adder (CSLA) is considered to measure driving capability.

Key-Words:- CPL, TGA, hybrid adder, BBL-PT, Pseudo NMOS, Portable application.

1 Introduction

Digital signal processors and application specific integrated circuits rely on the efficient implementation of arithmetic circuits to execute dedicated algorithms such as convolution, correlation and digital filtering [1].The execution of the algorithms requires dedicated ALU and MAC architectures. Adders and Multipliers are the key elements of these arithmetic units as they lie in the critical path. The critical path determines the overall performance of the system, and as multiplication operation can be realized using addition operation repeatedly, an investigation of various adders is carried out.

Adder performance can be improved by reducing the delay of carry propagation chain or basic adder cell . This can be addressed by either improving the structure of the 1-bit full adder which is one of the basic cells in adders such as the carry

select or carry skip, as well as the building block of the ripple carry adder (RCA) since an n bit RCA is formed by n 1-bit full-adders, or by using improved fast adder architectures such as conditional sum adders (CSAs) or carry look-ahead (CLA) adders.

Several variant logic styles have been used to design the full adder cells[1]-[7]. Conventional designs of full adders normally use only one logic style for the entire full adder design. Static CMOS full adder(FA) structure is based on the PMOS pull-up and NMOS pull-down transistors. Advantages of static CMOS logic style are its sturdiness against voltage scaling and transistor sizing and thus reliable operation at low voltages. The main drawback of static CMOS logic is the number of large PMOS transistors resulting in high input loads. Another drawback is the weak output driving capability [2]. Complementary pass-transistor logic (CPL) full adder have complementary inputs/outputs using NMOS pass-transistor logic with CMOS output inverters. Although CPL adder cell requires small number of transistors and has high speed operation, it suffers from threshold voltage drop problem [1], [3].

The transmission gate adder (TGA) uses both NMOS and PMOS transistors in parallel for implementing the logic. Like CMOS full adders, TGA requires complementary inputs. However TGA requires lower number of transistors per stack which makes it suitable for high speed operation [1]. Although TGA has fewer transistor count, it suffers from weak driving capability making it unsuitable for complex circuits.

Some full-adder designs use two different logic styles for sum and carry blocks for their implementation. One such adder is the CPL-TG FA[6]. It uses CPL XOR logic to generate the signal P = A xor B. From the generated P, sum and carry are generated using TG logic.The use of CPL circuit reduces the number of transistors, hence reducing the power consumption [6]. However it suffers from weak driving capability. A more restrictive approach for the design of low power low voltage full adder using CMOS and branch- based logic (BBL) was implemented by C.Piguet et al. in [8] , [9] .It is optimized for power dissipation using low power XOR gates[10] by I.Hassoune et al. in [4]. However it suffers from weak driving capability for specific inputs which necessitates a CMOS inverter at the output.

In [4] an adder has been proposed combining Pass Transistor (PT) logic and Branch-Based Logic (BBL) for sum and carry blocks respectively. The logic styles used in this adder are simpler and their combination requires fewer transistors compared to CMOS full adder and CPL full adder [4]. However Branch Based Logic- Pass Transistor (BBL-PT) Full adder has high delay since gate of level restorer PMOS in sum block is driven by complement of output , resulting in step at output[4].

This paper proposes a new structure of hybrid FA that we implemented by combining Pseudo NMOS logic and pass-transistor logic. Also, a new circuit for driving the level restoring weak PMOS has been proposed. A comparison between proposed full adder, active level driving circuit implemented version, and its counterparts viz., static CMOS FA , CPL FA ,CMOS-BBL hybrid FA and BBL-PT FA are carried out using TSPICE with 180nm technology file.

The rest of the paper is organized as follows. In section II the design of adder structure that implements Pseudo NMOS logic and pass-transistor logic is reviewed. Section III presents the design of active level driving circuit(ALDC) for level restoring and its implementation in proposed Pseudo-NMOS logic-PT adder respectively. Also performance comparison of the proposed Pseudo NMOS-PT adder cell, its optimized version Pseudo NMOS-PT with ALDC versus static CMOS FA , CPL FA ,CMOS-BBL hybrid FA and BBL-PT FA is carried out . Section IV discusses about the implementation of proposed Pseudo NMOS-PT with ALDC adder cell in 4 bit Carry select adder (CSLA) block. Comparison between CSLAs based on full adder cells from prior art, proposed Pseudo NMOS-PT FA and its optimized version with ALDC are carried out through analysis of simulation results. Section V gives a brief conclusion of the work.

2 Pseudo NMOS -PT Adder

The major conditions to be satisfied for the low power design are minimum number of transistors in cell and minimum inter-cell node connections. Pseudo NMOS logic design meets these requirements. In Pseudo-NMOS logic, the pull-down network is like that of a static gate but the pull-up network consists of single PMOS transistor with base grounded. In pull down network NMOS transistors are used and the logic is obtained from Karnaugh maps.

The Pseudo NMOS–PT adder is designed by implementing the sum block with Pass Transistor (PT) logic [See Fig.1(a)] and the carry block with the pseudo- NMOS logic [See Fig.1(b)] . Pseudo NMOS logic is chosen for carry block because of its reduced complexity and high speed. In case of multi bit adder the carry out of an adder cell has to be used as an input to next cell. Pseudo NMOS adder

cell generate carry with minimum delay and thus the overall delay of Pseudo NMOS logic based multi bit adders will be minimum compared to other static designs. Pass Transistor (PT) logic is chosen for sum block as it reduces the transistor count to 6.

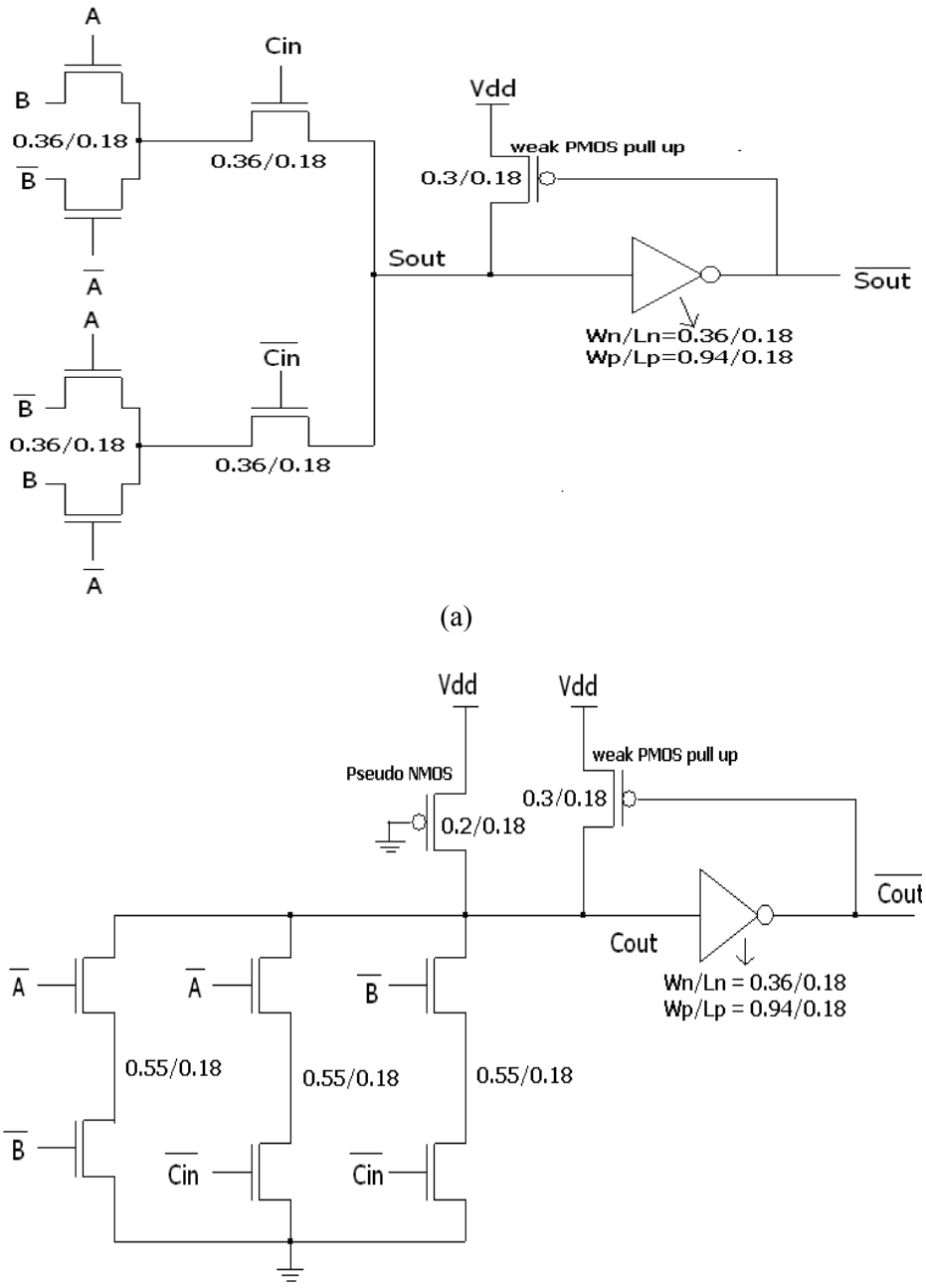


Fig. 1.(a) Sum block (b) Carry block of Pseudo NMOS logic-PT adder with weak PMOS pull-up

The disadvantage of this implementation lies in the resulting weak high output level in pass transistors used in the sum block and low noise margin of the dynamic circuit used in carry block of the proposed full adder. The feedback realized by the pull - up PMOS transistor [see Fig. 1(a)] is used in order to restore the weak logic "1" (i.e., V_{dd} V_{tn}) caused by the pass transistors of sum block and significantly reduce contention[see Fig. 1(b)], in carry block caused by dynamic gates . However , the level

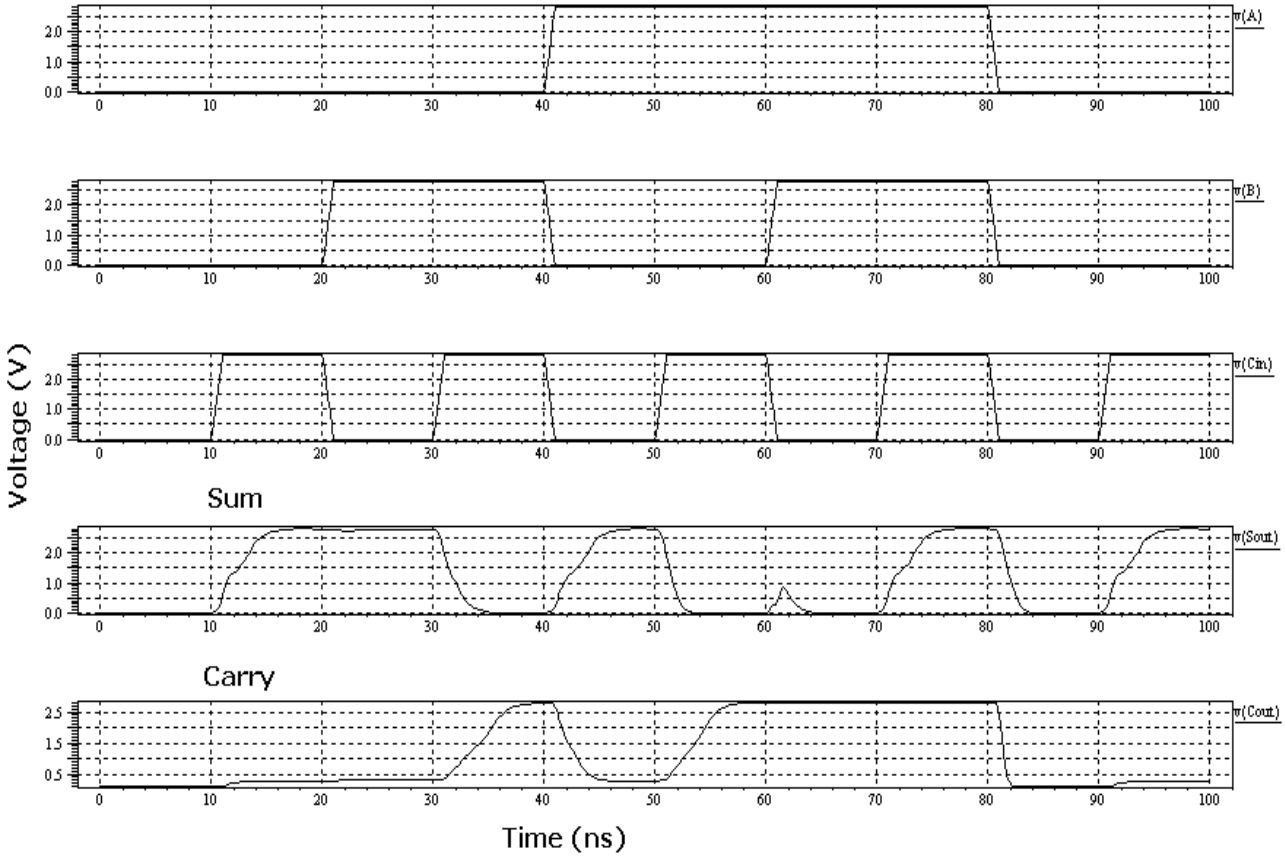


Fig. 2.Pseudo NMOS PT adder output waveform

restoration implemented this way causes a step at the output of node "S_{out}" of sum block during 0(active low) to 1(active high) transition , as shown in Fig. 2 and significant power dissipation in Carry block . This voltage step is due to the threshold voltage drop in the pass transistors and the delay needed by the level restorer to restore the weak logic "1" level . Power dissipation in carry block is due to simultaneous ON of both level restorer PMOS and NMOS transistor of pull down network during the time interval from when the pull-down network starts conducting until voltage at the output node reaches a high voltage.

3 Structural modifications of the Proposed Adder and Implementation

In order to prevent the step that appears in S_{out} during 0 to 1 transitions and to reduce the dynamic power dissipation impaired on the carry out node due to weak PMOS level restorer , an active level driving circuit is proposed and is used to drive the pull-up PMOS transistor of sum and carry block.

3.1 Proposed Active Level Driving Circuit (ALDC)

The driving circuit uses a NMOS transistor connected to the inverted output and a PMOS transistor connected to V_{dd} for driving the gate of the pull-up level restoring PMOS transistor. The proposed driving circuit drives the weak PMOS pull up transistor only during the high output.

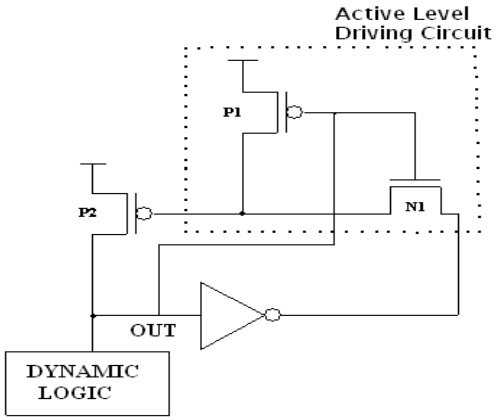


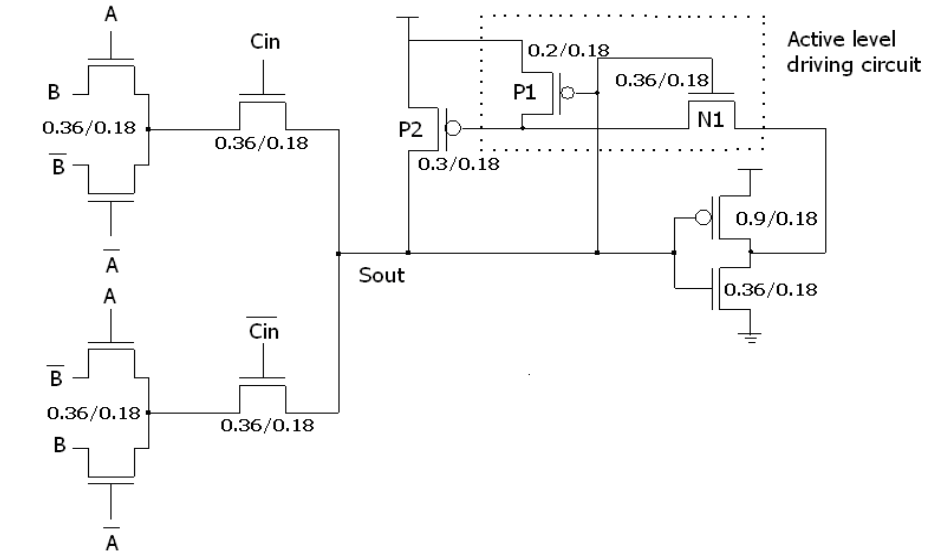
Fig. 3.Active level driving circuit

Whenever the output goes low, NMOS Transistor N_1 of active driving circuit is OFF and PMOS

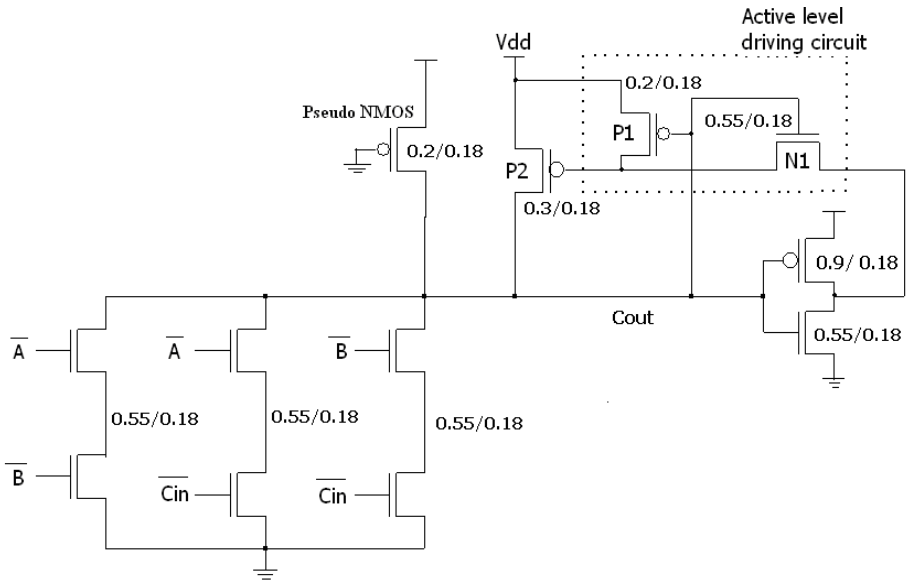
transistor P_1 is ON charging the gate of the PMOS pull-up transistor P_2 to V_{dd} , turning it completely OFF.

3.2 Implementation of ALDC in Pseudo NMOS-PT adder

The active level driving circuit in Fig.3 is connected in the Pseudo NMOS-PT full adder [See Fig.4] to drive the pull up PMOS transistor. For high S_{out} and C_{out} PMOS transistor P_{s1} and P_{c1} are OFF and NMOS transistors N_{s1} and N_{c1} are ON, thus the inverted S_{out} and C_{out} drives the gate of pull up PMOS transistor , minimizing the voltage step in case of S_{out} and contention between PMOS and NMOS network in case of carry. During active low i.e., when S_{out} and C_{out} are zero PMOS transistor P_{s1} and P_{c1} are ON and NMOS transistors N_{s1} and N_{c1} are OFF, charging the gate of pull up PMOS transistor to V_{dd} thus turning it to completely OFF. As the pull up PMOS transistor is brought into OFF state during low output by the ALDC , the line from V_{dd} to ground is open, reducing leakage power dissipation.



(a)



(b)

Fig. 4.(a) Sum block (b) Carry block of Pseudo NMOS - PT adder with ALDC.

3.2.1 Supply Voltage Optimization

The performance plot of proposed 1 bit adder cell for various supply voltages (Fig.5) indicates that noticeable power saving and power-delay-product (PDP) saving can be realized for supply voltage of 2.8 V. So the supply voltage used for the proposed design is 2.8 V.

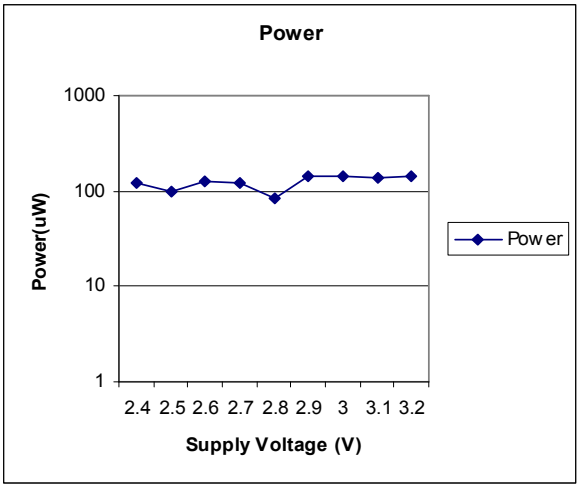
3.2.2 Simulation Results

Simulations were performed in 0.18-µm PD CMOS technology , with a supply voltage of 2.8v and clock frequency of 100 MHz. Transistor sizes used for the simulation are shown in Fig. 4(a) and Fig.4(b). For all possible input sets applicable to the full adder, the average power consumption and worst case delay are extracted. The results of simulation are summarized in table 1.

Table 1. Performance Comparison of 1 bit adders in CMOS 0.18µm technology with V_{dd} = 2.8v, f= 100MHz

	Static CMOS FA	**CPL FA**	**CMOS-BBL FA**	**BBL-PT FA**	**Pseudo NMOS-PT FA**	**Pseudo NMOS –PT FA with ALDC**
Total Power(µW)	1547.7	989.7	298	108.3	89.25	78.4
Delay (ns)	2.43	2.36	2	2.39	2.32	2.41
PDP (Joules)	3.75 E-12	2.33 E-12	0.59 E-12	0.26 E-12	0.26 E-12	0.18 E-12
Static Power (nW)	0.53	9.27	1.8	2.3	220	117
Transistor count	28	32	24	23	19	23

PDP – Power Delay Product; CPL FA – Complementary Pass transistor Logic Full Adder; CMOS- BBL FA – Complementary MOS Branch Based Logic Full Adder; BBL-PT FA – Branch Based Logic – Pass Transistor Full Adder; Pseudo NMOS-PT – Pseudo NMOS Pass Transistor; ALDC – Active Level Driving Circuit



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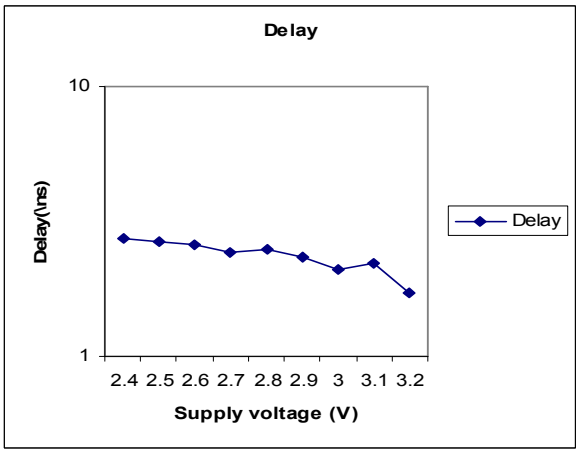

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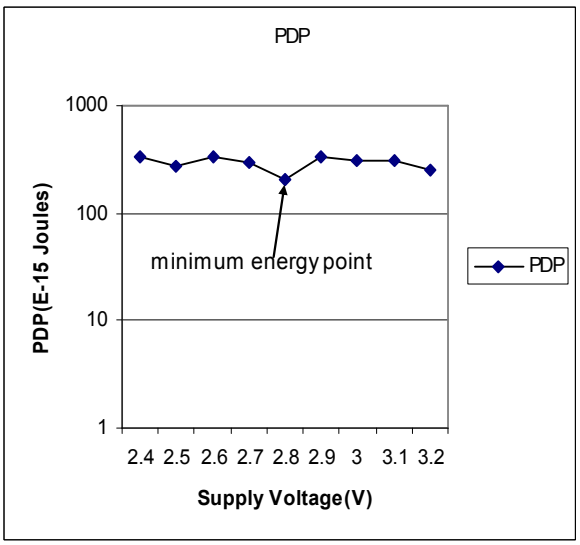


(c)

Fig 5. Comparison of (a) power (b)delay(c) power-delay-product(PDP) of 1 bit Pseudo NMOS-PT adder with ALDC for various supply voltages.

It can be noticed that Pseudo NMOS –PT adder demonstrates better power dissipation and PDP in comparison with static CMOS FA, CPL FA, CMOS- BBL FA and BBL-PT FA. Conversely , its shows the highest delay in comparison with CMOS-BBL FA due to PMOS pull up transistor. Pseudo NMOS-PT with ALDC adder outperforms all other adders in the *state-of –art* design in total power dissipation and PDP , thanks to the ALDC which charges the gate of the PMOS pull up transistor to V_{dd} , turning it to OFF for zero or low output, thus disconnecting the line from supply to ground, minimizing leakage power dissipation.

The performance parameters of proposed Pseudo-NMOS –PT adder and its optimized version, Pseudo NMOS-PT with ALDC are evaluated with various supply voltages. From the evaluation it is found that the power dissipation is better below V_{dd}= 2.8 V ,but the delay performance degrades.

3.2.2.1 Static Power in the Pseudo NMOS with ALDC Adder

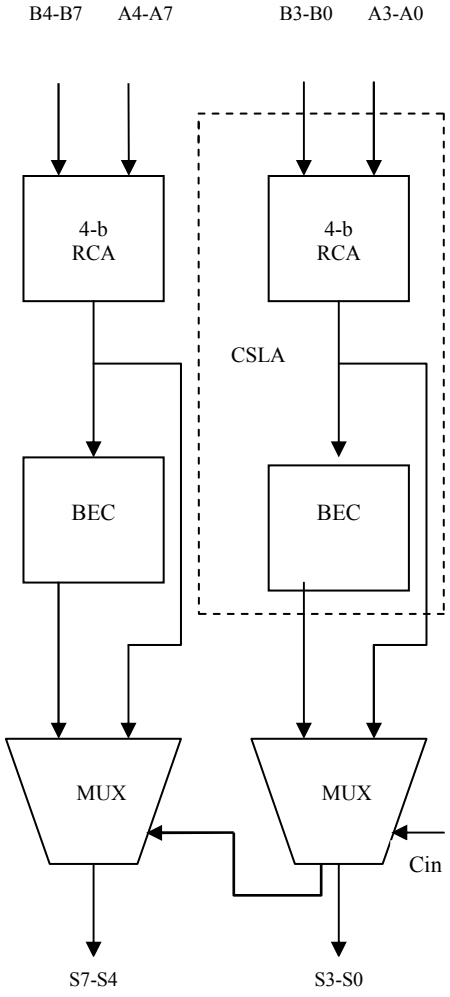
The static power dissipation of our proposed Pseudo NMOS-PT adder is high compared to static CMOS FA, CPL FA, CMOS- BBL FA and BBL-PT FA due to permanent ON of PMOS transistor used in carry block .The pull up PMOS transistor used in sum and carry block is not turned off completely due to the capacitance at the S_{out} and C_{out} node , which in addition contributes to the static power dissipation. The leakage power due to weak PMOS pull up transistor is reduced by the active level driving circuit , which charges the gate of pull up PMOS transistor to V_{dd} for active low output bringing it to completely OFF. From table I it can be seen that static power dissipation of Pseudo NMOS-PT adder with ALDC reduces by 46.8% compared to basic version.

4 Pseudo NMOS-PT adder based CSLA

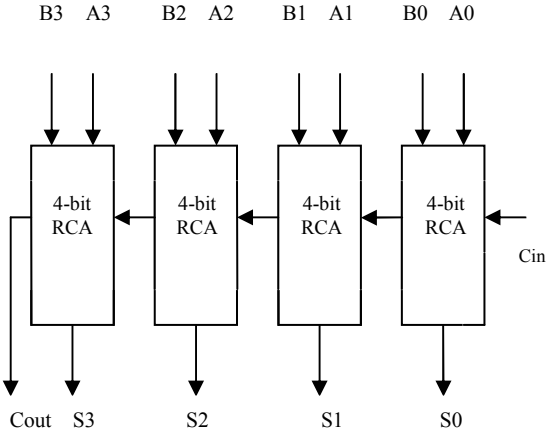
To determine if the cells that show good performance in 1-bit operation have enough driving capability and show similar performance when they are cascaded in large circuits, we chose 4-bit Carry Select Adder (CSLA) block for implementation.

The basic idea of the Carry Select Adder (CSLA) [11] is to use two blocks of Ripple-Carry Adders (RCA), one of which is fed with zero for carry-in while the other is fed with one for carry-in. Both the RCA blocks function in parallel. 2-1 multiplexers are used to select one of the pre-calculated sums from RCA blocks based on the carry-in. Also, the resulting carry-out is selected and

propagated to the next RCA block as carry input. The propagation delay of carry signal through n-bit adder block is reduced from O(n) to the number of stages times the delay of the multiplexers. But CSLA is not area efficient because multiple pairs of RCAs are required to generate partial sum and carry. So, the RCA with carry-in = 1 is replaced by Binary to Excess-1 Converter (BEC)[See Fig.5 and Fig.6] in the CSLA structure[11] to minimize area and reduce power consumption.



(a)



(b)

Fig.5. Block Diagram of (a) CSLA (b) 4-bit RCA

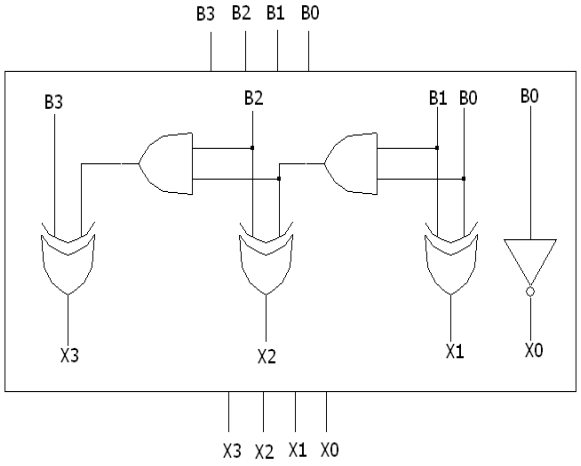


Fig.6. 4-bit BEC

A 4 bit RCA based on Pseudo NMOS-PT adder with ALDC is implemented in CSLA proposed in [11]. CSLA blocks with 4 adders in RCA were implemented with static CMOS FA, CPL FA, CMOS-BBL FA and BBL-PT FAs and compared using Vdd= 2.8 v and frequency 50 MHz. The results of comparison are summarized in table 2.

Table 2. Performance Comparison of CSLA implemented with various adders in CMOS 0.18µm technology with V_{dd} = 2.8V, f =50MHz

	Static CMOS FA	CPL FA	CMOS-BBL FA	BBL-PT FA	Pseudo NMOS-PT FA	Pseudo NMOS –PT FA with ALDC
Total Power (mW)	9.64	11.6	11.59	9.14	8.58	7.9
Delay (ns)	8.15	5.06	7.67	9.2	10.23	10.1
PDP (Joules)	7.85 E-11	5.87 E-11	8.88 E-11	8.4 E-11	8.77 E-11	7.98 E-11
Static Power (mW)	1.47	2.32	2.32	1.33	2.56	2.07
Transistor Count	112	128	96	92	76	92

PDP – Power Delay Product; CPL FA – Complementary Pass transistor Logic Full Adder; CMOS- BBL FA – Complementary MOS Branch Based Logic Full Adder; BBL-PT FA – Branch Based Logic – Pass Transistor Full Adder; Pseudo NMOS-PT – Pseudo NMOS Pass Transistor; ALDC – Active Level Driving Circuit

Simulation analysis shows that CPL FA based CSLA shows the best delay performance due to high driving capability**,** however the power consumption is more due to higher transistor count. The high driving capability of CPL FA based CSLA demonstrates best PDP performance than static CMOS FA, CMOS-BBL FA, BBL-PT FA and our Pseudo NMOS-PT FA based CSLAs. The Pseudo NMOS-PT adder based 4-bit CSLA shows a higher delay than the static CMOS FA, CMOS-BBL FA and BBL-PT based 4-bit CSLAs but dissipates less total power than the BBL-PT FA and CMOS-BBL FA, thanks to the reduced transistor count. With total power dissipation of Pseudo NMOS-PT with ALDC FA based CSLA circuit less by 8% compared with Pseudo NMOS-PT circuit, the Pseudo NMOS-PT with ALDC FA implemented circuit demonstrates better PDP performance. This gain in performance is due to the ALDC which turns OFF the weak pull up PMOS for active low outputs, minimizing leakage power component.

5 CONCLUSION

In this paper , we have presented a design of full adder based on Pseudo NMOS logic for carry and Pass transistor logic for sum. The optimization in performance of the adder has been carried out by implementing an ALDC for driving pull up PMOS transistor to further reduce the static and total power dissipation. Simulations using TSPICE in 180 nm technology have shown that Pseudo NMOS-PT adder with ALDC achieves a significantly better static power and total power dissipation when compared with its basic version without ALDC and other commonly used adders viz., CPL FA and CMOS-BBL FA. Next, the 4-bit CSLA circuit based on Pseudo NMOS-PT adder with ALDC achieves total power dissipation of 18% and 13.6% lower

compared to the 4-bit CSLA implemented with conventional static CMOS FA and BBL-PT FA featuring better PDP. We believe that , in complex designs such as ALUs and MAC , the benefits of our proposed Pseudo NMOS-PT adder with ADLC could be fully realized.

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