Restoration circuits for Low power Reduce Swing of 6T and 8T SRAM Cell With Improved Read and Write Margins

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Abstract: A paper that examines the factors thataffect the Static Noise Margin (SNM) of a StaticRandom Access memories. At an equivalent time,they specialise in optimizing Read and Writeoperation of 8T SRAM cell which is best than 6TSRAM cell Using Swing Restoration Dual NodeVoltage. The read and Write operation and improveStability analysis. This SRAM technique on thecircuit or architecture level is required to improveread and write operation. during this paperComparative Analysis of 6T and 8T SRAM Cellswith Improved Read and Write Margin is completedfor 180 nm Technology with Cadence Virtuososchematics Tool.This Paper is organized as follows: thecharacteristics of 6T SRAM cell are described arerepresented in section VIII. In section IX, proposed8T SRAM cell is described. In section X, Standard8T SRAM cell is described. Section XI includes thesimulation results which give comparison of variousparameters of 6T and 8T SRAM cells. In Section XIISimulation Results and DC analysis and sectionXIII conclusion the work.

Keywords: Low power SRAM, Swing Restoration,Dual Node Voltage, Read and Write Noise margin.
Received: March 5, 2019. Revised: September 11, 2020. Accepted: October 25, 2020. Published: December 21, 2020.

1. Introduction to Memory:

The most purpose of storage is that without a big amount of memory, a computer would merely be ready to perform fixed operations and immediately output the result. it's to be reconfigured whenever an operation must be performed.
Memories storage is as shown in Figure 1.

1.1. Primary Storage:

Primary storage, often mentioned simply as memory, It is that the just one directly accessible to the CPU. The CPU continuously reads instructions stored there and executes them as needed. Any data actively operated on is additionally stored there in uniform manner.

1.2. Secondary Storage:

Secondary storage (or external memory) differs from primary storage therein it's not directly accessible by the CPU. the pc usually uses its input/output channels to access auxiliary storage and transfers the specified data using intermediate area in primary storage. auxiliary storage doesn't lose the info when the device is powered down. It is non-volatile. Per unit, it's typically also two orders of magnitude less costly than primary storage.

1.3. Tertiary Storage:

Tertiary storage or tertiary memory provides a 3rd level of storage. It is involves a robotic mechanism which can mount and dismount removable mass storage media into a memory device consistent with the system's demands; this data is usually copied to auxiliary storage before use.

1.4. Offline Storage:

Off-line storage is employed to transfer information, since the detached medium are often easily physically transported. Additionally, just in case a disaster, for instance a fireplace, destroys the first data, a medium during a remote location will probably be unaffected, enabling disaster recovery. Off-line storage increases general information security.

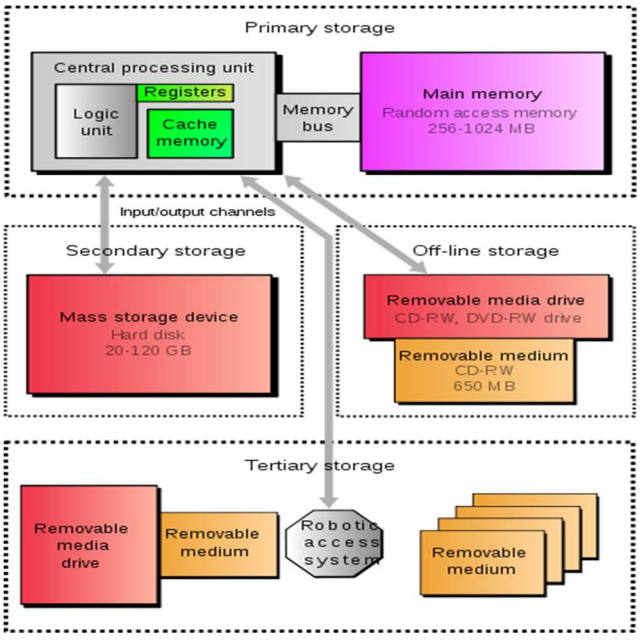
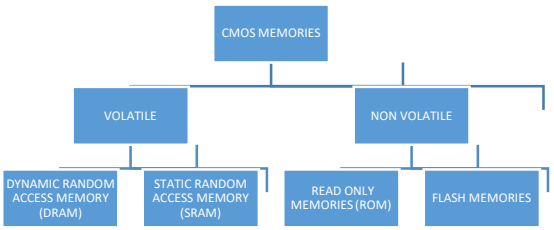


Figure1. Types of Computer data storage

2. Classification of Cmos Memories:



The memory can be classified as volatile and non-volatile memories.

The memory are often classified as volatile and non-volatile memories.

1) Volatile memories:
These are memories that need power to take care of the stored information. Random-access memory (RAM) may be a sort of computer data storage. It takes the shape of integrated circuits that allow stored data to be accessed in any order. "Random" refers to the thought that any piece of knowledge are often returned during a constant time, no matter its physical location and whether or not it's regarding the previous piece of knowledge.
a) Dynamic- Dynamic Random Access Memory (DRAM):
Dynamic random access memory that stores each little bit of data during a capacitor within an microsecond. That is real capacitors store charge, the knowledge eventually fades unless the capacitor charge is refreshed periodically. It is refresh requirement, it's a dynamic memory as against SRAM and other static memory. The advantage of DRAM is its structural simplicity just one transistor and a capacitor are required per bit, compared to 6 transistors in SRAM.
b) Static- Static Random Access Memory (SRAM):
Static Random Access Memory of semiconductor memory, it doesn't to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data reminisce but remains volatile within the conventional sense that data is eventually lost when the memory power is going off.

2) Non- Volatile Memories:
Non-volatile memory, NVM or nonvolatile storage, is memory which will retain the stored information even when not powered. samples of non-volatile memory include ROM, non-volatile storage and most sorts of magnetic memory devices.

a) Read Only Memory (ROM): may be a class of storage which is fabricated with desired data permanently fixed in it, thus it can't be modified.
b) FLASH: may be a non-volatile memory technology which will be electrically erased and reprogrammed. Since non-volatile storage is non-volatile, no power is required to take care of the knowledge stored within the chip.
Working of memory with processor:
The processor communicates with the memory system to memory interface. The processor sends the data over the address bus. For read, MemWrite is 0 and therefore the memory returns the info on the ReadData bus. For write, MemWrite is 1 and therefore the memory returns the info on the WriteData bus. the method is shown within the diagram below.

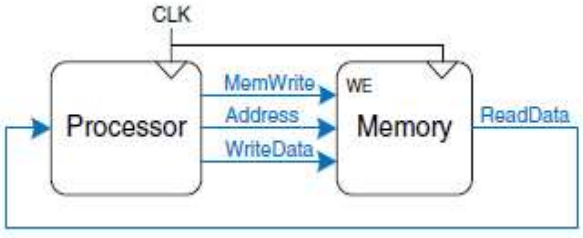


Figure 2.1 Memory Interface

Computers store most ordinarily used instructions and data in faster but smaller memory called cache. Cache is typically built out of SRAM on an equivalent chip because the processor. If the processor requests data that's available within the cache, it's returned quickly. this is often called cache hit. Otherwise, the processor retrieves the info from main memory (DRAM). this is often called cache miss.

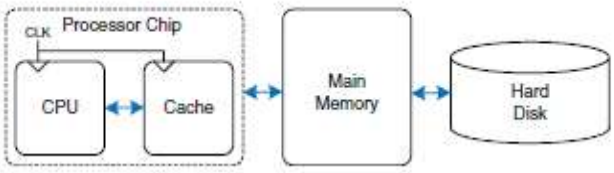


Figure 2.2 Cache

The performance analysis i.e. the miss rate, the hit rate and average access time (AMAT) where AMAT is that the average time a processor must await memory per load or store instruction.

$$Miss\ Rate = \frac{Number\ of\ misses}{Number\ of\ total\ memory\ accesses} = 1 - Hit\ Rate$$

$$Hit\ Rate = \frac{Number\ of\ hits}{Number\ of\ total\ memory\ accesses} = 1 - Miss\ Rate$$

$$AMAT = t_{cache} + MR_{cache}(t_{MM} + MR_{MM}t_{VM})$$

where t_{caches}, t_{MM}, and t_{VM} are the access times of the cache, main memory, and virtual memory, and MR_{cache} and MR_{MM} are the cache and main memory miss rates, respectively.

3. Static Random Access Memory (SRAM)

The following elements are required to create a SRAM,

• Row Decoder & Column Decoder: The operation of the SRAM starts with the detection of an address change within the address register, and therefore the decoders select one memory cell.

• 6T bit cell Array: is employed because it has fixed cell size and straightforward to style as a logic circuit. 6T CMOS performs read and write operation.

• Sense Amplifier: main function is to sense a read selected memory cell.•

• Control Circuit: to access the bit cells the read/write circuitry is implemented to regulate the info being read or written. this is often achieved by control circuitry which consists of tristate buffers.

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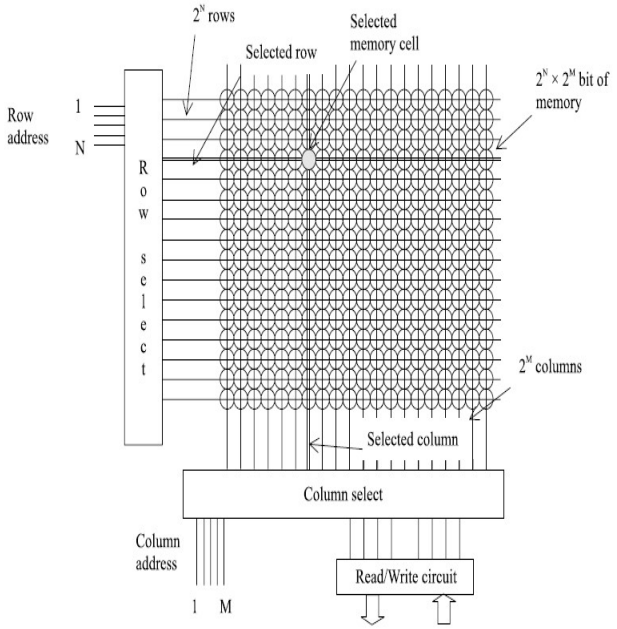


Figure3.1 Typical Memory Architecture

3.1. Row Decoder:

SRAM adopts a multi-divided memory cell array structure to realize high speed word decoding and reduce column power dissipation. The multi-stage decoder circuit technique is adopted because it has advantage over the one-stage decoder in reducing the amount transistors and fan-in. For column decoders, which select the specified bit pairs out of the set of the sets of bit pairs within the selected row a typical dynamic AND circuit might be used.

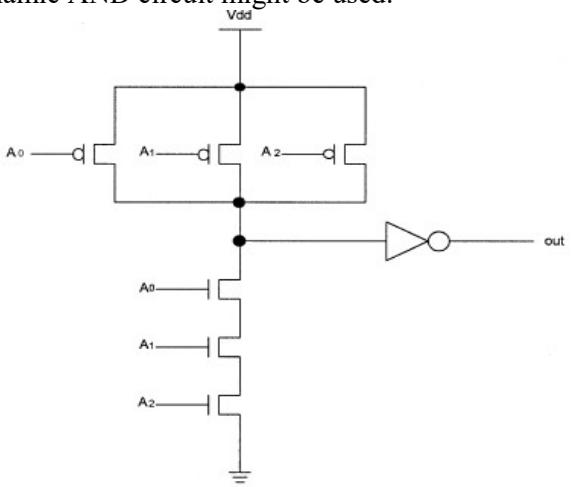


Figure 3.2 Static CMOS AND Gate

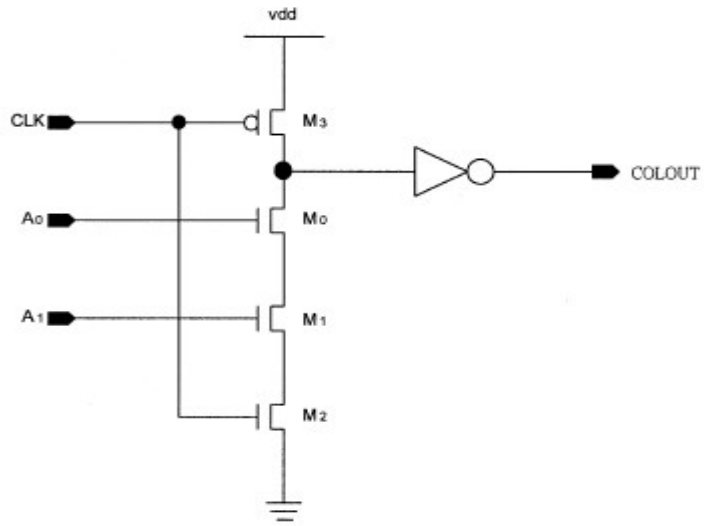


Figure 3.3 Dynamic CMOS AND Gate

Digital Analysis of Row Decoder:

The address lines i.e. the word line is generated using this logic. for instance, if we've 1024*32 bit memory, we'd like a 10:1024 (2^10) decoder. Since to get such an outsized decoder logic with and gates makes it slower, cascading of multiple smaller decoders is completed. Here, there are 2 approaches that were considered:

a. First we design 2:4 decoders □ 4:16□8:256, four of 8:256 and one 2:4 is employed to get 10:1024

b. We use 2:4 decoders and 3:8 decoders □ 5:32, then 33 of them are wont to generate 10:1024 i.e. first 5:32 is employed to get the primary stage and

therefore the remaining 32 are wont to generate the second stage of 1024 outputs.

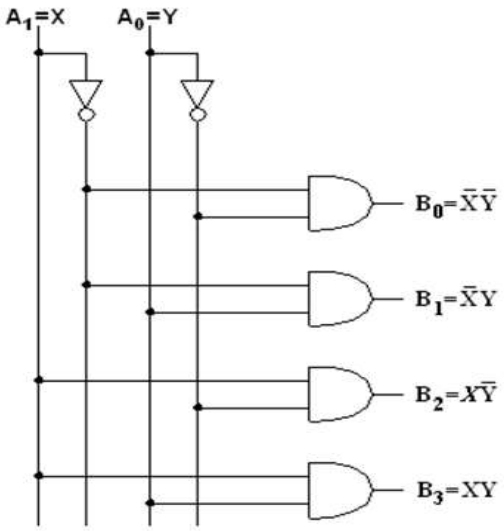


Figure 3.4 Decoders

Table 3.1 Truth table for 5:32 decoder

A	B	C	D	E	Output
0	0	0	0	0	DO
0	0	0	0	1	D1
0	0	0	1	0	D2
0	0	0	1	1	D3
0	0	1	0	0	D4
0	0	1	0	1	D5
0	0	1	1	0	D6
0	0	1	1	1	D7
0	1	0	0	0	D8
0	1	0	0	1	D9
0	1	0	1	0	D10
0	1	0	1	1	D11
0	1	1	0	0	D12
0	1	1	0	1	D13
0	1	1	1	0	D14
0	1	1	1	1	D15
1	0	0	0	0	D16
1	0	0	0	1	D17
1	0	0	1	0	D18
1	0	0	1	1	D19
1	0	1	0	0	D20
1	0	1	0	1	D21
1	0	1	1	0	D22
1	0	1	1	1	D23
1	1	0	0	0	D24
1	1	0	0	1	D25
1	1	0	1	0	D26
1	1	0	1	1	D27
1	1	1	0	0	D28
1	1	1	0	1	D29
1	1	1	1	0	D30
1	1	1	1	1	D31

3.2. 6T Bit Cell Array:

6T Bit Cell Array: The basic cell for static RAM consists of 6 transistors during which there are two pass gates. We are using 2 inverters, which are cross coupled and that they store the info being read or written whereas the pass transistors purpose is to pick the cell which the word line activates and pass the info inputs to be read or written to the cross coupled inverters. The circuit diagram of 6T SRAM bit cell is shown below.

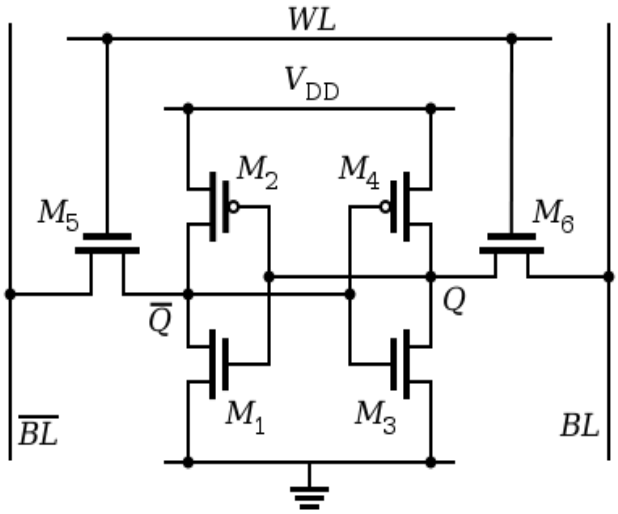


Figure 3.5 6T SRAM Cell

Digital Analysis 6T SRAM Cell:

1. READ: Assume that the worth of memory is 1 stored at Q. The read cycle is started and therefore the word line WL is asserted enabling both access transistors. Data stored in Q and Qbar are transferred to the bit lines by leaving BL at its precharged value and discharging BLbar through M1 and M5 to logical 0. It is BL side the transistors M4 and M6 pull the bit line toward Vdd a logical 1.
2. WRITE: Assume that the worth of memory is 1 stored at Q. the worth to be written is placed on BL and BLbar. The write cycle is started and therefore the word line WL is asserted enabling both access transistors. Lets say, we would like to write down 0, BL is adequate to 0, Q is adequate to 1 thus the transistors M6 and M5 change stage and therefore the value gets written.
3. Sense Amplifier: It is association with memory cells, are key elements in defining the performance

and environmental tolerance of CMOS memories. In an integrated memory circuit sensing means the detection and determination of the info content of a specific memory cell.
CMOS memories are required to extend speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it involves memory sense amplifier design. With increase memory capacity, usually comes an increase bit-line parasitic capacitance. This increased bit line capacitance successively slows down voltage sensing and makes bit line voltage swings expensive.

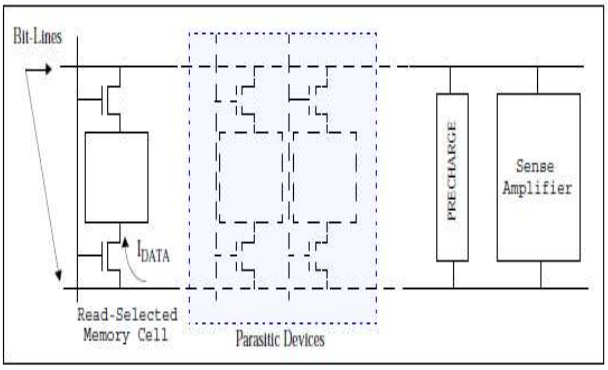


Figure3.6 Typical Sense Amplifier

The main function of sense amplifier is to detect stored data from a read selected memory cell. The memory cell being read the current Idata that removes some charge (dQ) stored on the pre-charged bit lines. Since the bit lines are very long and are shared by other similar cells, It is parasitic resistance Rbl and capacitance Cbl are large. That is resulting bit line voltage swing (dVbl) caused by removal of dQ from the bit line is extremely small dVbl=dQ/Cbl. Sense amplifiers are wont to translate this small voltage signal to a full signal which will be further employed by digital logic. regeneration Differential Voltage Sense Amplifier:

Positive Feedback Differential Voltage Sense Amplifier:

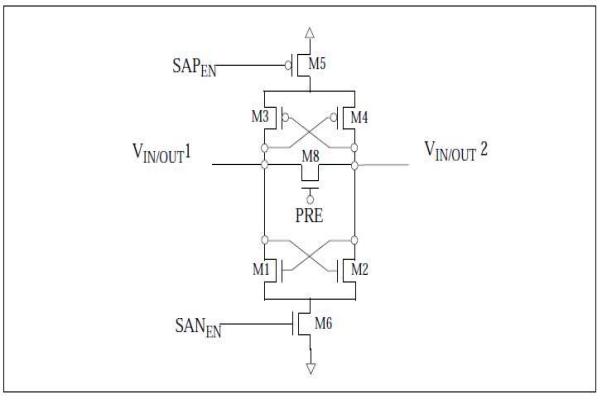


Figure3.7 Positive feedback voltage sense amplifier

Digital analysis of Positive Feedback Voltage Sense Amplifier:

It is regeneration amplifier has 2 data nodes Vin/out1 and Vin/out2 and three control nodes SANen, SAPen and PRE. . the info nodes act as input and output to the sense amplifier and its operation is as follows:

1. the info nodes are equalized using PRE

2. The memory cell being read is asserted and alittle voltage difference forms on nodes Vin/out1 and Vin/out2

3. While M1 and M2 are biased to be operating within the saturation region M6 is turned on by SANen

4. As both Vin/out1 and Vin/out2 are decreasing in voltage so is that the difference between them One of them decreases much faster then the other and causes M1 or M2 to enter cutoff while the other starts operating in linear region.

5. one among them decreases much faster then the opposite and causes M1 or M2 to enter cutoff and the other starts operating in linear region.

6. At now M5 is turned on by SAPen which pulls the signal rapidly apart

At now since Vin/out1 and Vin/out2 are directly connected to bit lines the info is automatically written to the read memory cell. Due to its regeneration this voltage sensing amplifier achieves a really high differential gain. This high gain minimizes sensing time by having the ability to sense small voltage swings on the bit line.

3. Control Read/Write Circuit:

The write-in buffers are enabled in such how on have them control the bit lines. More precisely, by setting WE and OE the info terminal D is formed to drive one BL and its conjugate BLB in direct and complemented form respectively. Digital Analysis of knowledge Read: This can be achieved by setting WE=0 which disables the write-in buffers, thereby permitting the memory cell selected to exert control over bit lines BL and BLB. Further by setting OE=1 propagates the state stored therein cell to the info terminal D via the enabled output buffer. Digital Analysis of knowledge Write: This is achieved by setting WE=1 and OE=0 and therefore the data terminal D drives the bit lines. The word line is activated causing the cross-connected inverters within the selected cell to assume the worth of bit lines imposed externally. After the cell is deselected, the regeneration mechanism maintains that state indefinitely until the cell's content is overwritten or the availability voltage gets turned off. Figure3.8 Read/Write negative feedback circuit

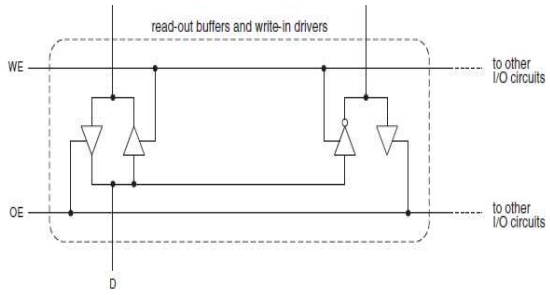


Figure3.8 Read/Write Control Circuit

3.4. Tristate Buffers:

Tristate buffers are the buffers which are wont to control the read and write operations. The write enable and output enable signals are generated through these buffers.

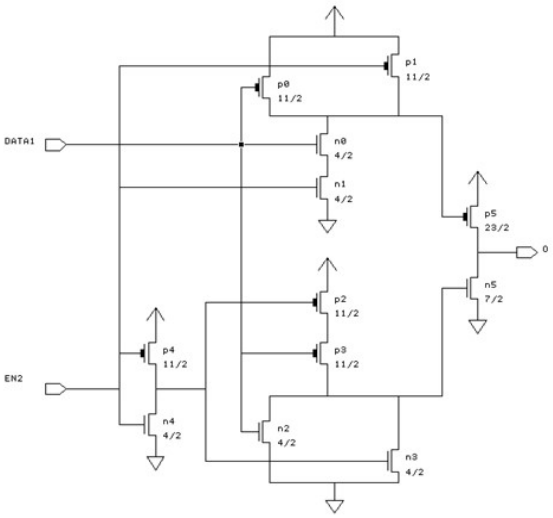


Figure 3.9 CMOS Implementation of Tristate Buffer

4. Detailed Analysis of 6T Cell Read Operation

The Figure given below shows a typical static Random Access memory cell. The SRAM Circuit consists of a flip-flop comprising two cross-coupled inverters and two access transistors Q5 and Q6.

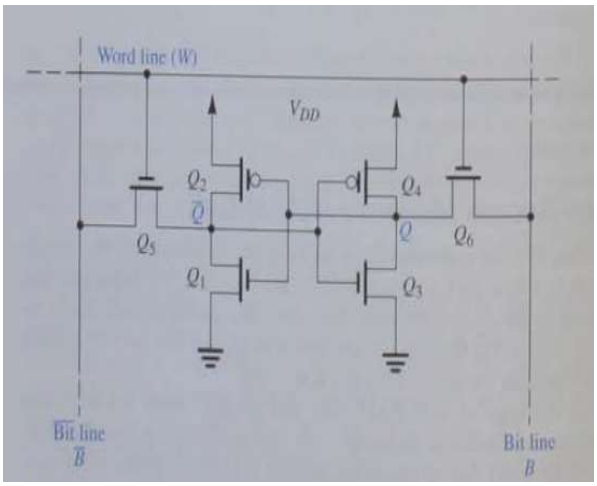


Figure 4.1 Typical Static Memory Cell

It is a read operation, the bit lines are pre-charged to Vdd. The read operation is initiated by enabling the word line and connecting bit lines, BL and BLB to the interior nodes of the cell.

Assume that the cell is storing a 1. during this case Q are going to be at Vdd and Qbar are going to be at 0 V. When the word line is chosen and access

transistors are turned Q5 and Q6 are turned on.

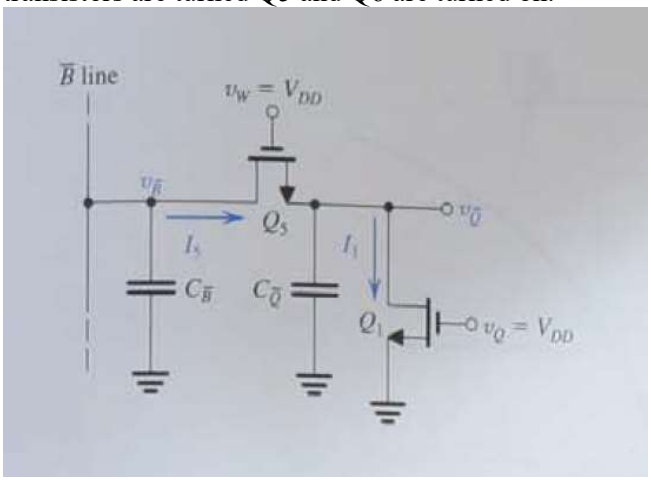


Figure 4.2 Operation performed during Read 1

From the above given figure, we see that current flows from Bbar line through Q5. This current charges CQbar. It is Equilibrium is reached when CQbar is charged to VQbar at which I1 equals I5. to supply a non destructive read operation, the subsequent design constraints are to be taken care of:

1. VQbar should be not up to Vtn of subsequent inverter i.e. within the figure it should be not up to Vtn of Q3. Vtn is that the threshold voltage of individual NMOS and is process dependent.
2. a). ratio of NMOS pass transistor for read 1 is given below

$$\frac{(W/L)_5}{(W/L)_1} \leq \frac{1}{\left(1-\frac{V_{tn}}{V_{DD}-V_{tn}}\right)^2} - 1$$

…… for the above circuit

$$\frac{(W/L)_a}{(W/L)_n} \leq \frac{1}{\left(1-\frac{V_{tn}}{V_{DD}-V_{tn}}\right)^2} - 1$$

…… general form

b). The ratio for read 0 is same as above apart from the very fact that the access transistors are different i.e. ratio if Q6/Q2 = Q5/Q1.

3. In read 1 operation, VBL is precharge voltage and VBLB is discharged to ΔV.

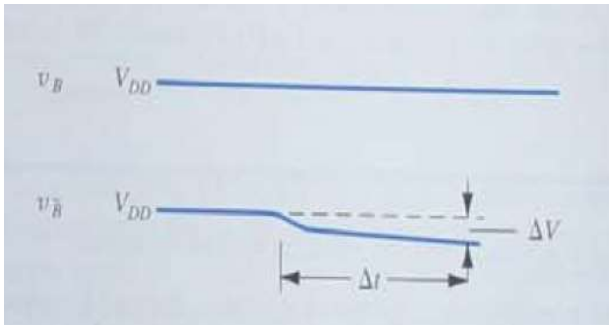


Figure 4.3 Bit line during Read 1 operation

Whereas in read 0 operation, VBLB precharge voltage and VBL is discharged to ΔV.

4. It is time required for the bit line voltage to discharge to ΔV by capacitor CB is given by the equation given below,

…time delay to reach ΔV

$$\Delta t = \frac{C_B\ \Delta V}{I_5}$$

…time delay to reach ΔV

5. Introduction SϿ ϛ

Low power Static Random Access Memories have become a critical component of many VLSI chips. That is a consideration for microprocessors where the on chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory [P. Barnes 2010, S. Hesley, et.al, 2009]. one of the major issues in the design of an SRAM cell in stability. The cell stability analysis of the sensitivity of the memory to process tolerances and operating conditions.

The stability of Static Random access memory cell in the presence of DC noise is measured by the static noise margin (SNM). Static Noise Margin is the amount of voltage noise required at the output nodes to flip the state of the cell. This can be obtained using using the voltage transfer characteristic (VTC) of the two cross coupled inverters of the SRAM cell [10].

Figure 7.1 illustrates the schematic of a 6 transistor SRAM cell for simulating the static noise margin. The sources Vn are the noise sources at the state

nodes of the cell [15].

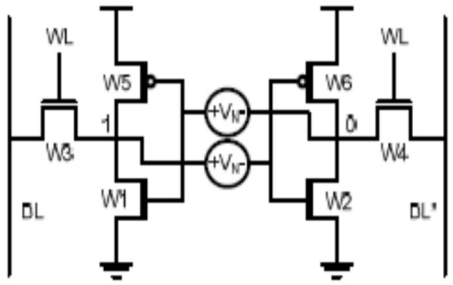


Fig.7.1 Schematic of a 6T SRAM bit cell with noise voltage sources for measuring SNM [10].

The cross-coupled inverters maintain a bi-stable state and their output nodes retain the data stored in the cell. However, as the noise Vn increases, the stability of the cell degrades because of the fluctuations at the node voltages. The Static Noise Margin quantifies the allowed levels of these noise voltages and thus the ability of these inverters to retain their state in the presence of noise.

The goal of this paper is to determine the effect of several circuit parameters on the SNM of the 6T SRAM cell designed in 180-nm CMOS process technology and compare it with the model derived in [10].
The SNM of the SRAM Cell When in standby or retain mode, read operation, and write operation. The SNM of the SRAM cell is obtained by plotting the VTCs of the Two cross-coupled inverters. The VTC of one of the inverters is flipped with respect to the line y = x in order to form a "butterfly curve". The SNM is the side of the smaller square that can be fitted inside the "eye" of the graph as shown in Figure 7.1 [10]

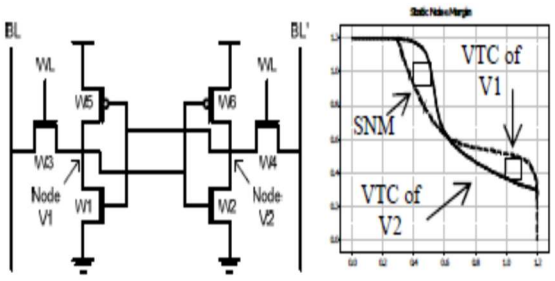


Fig.7.2 Schematic of a 6T SRAM bit cell and sample SNM-the side of the largest square fitted inside the graph [16].

6. Six Transistor (6¢) Sram Cell

In a conventional 6T SRAM cell, the data storage nodes are directly accessed through the bit-line access transistors during read operations, as shown in Fig.8.1. While reading, the storage node voltages are disturbed between cross-coupled inverter pair and bit lines. The BL and BLB are the bit lines and WL is the word line. The access transistors are controlled by WL (word line) to perform the operation of read and write operation. Bit lines act as input and output nodes. During a read operation, bit lines transfer the data from SRAM cells to a sense amplifier. Based on the technology the minimum length of the transistors is 180nm [10].

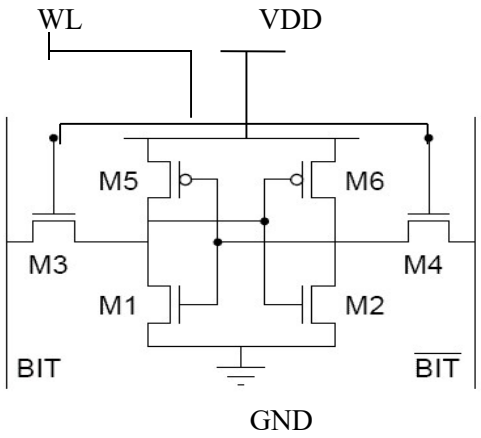


Fig.8.1 6T SRAM Cell [10]

7. Proposed Eight Transistor (8¢) Sram Cell

This is proposed SRAM, Fig.9.1 Dual Voltage with Swing Restoration Logic Perform node voltage in Hold, read and write operation and other parameters like Delay, Stability, are used. Comparison between Low power 6T SRAM and proposed 8T SRAM Cell designs is done. The comparison results revels that read, write and hold mode operation for 8T SRAM cell is better than 6T SRAM cell. This is because higher noise margin are obtained which ensure good write ability for the bit-cell [14].

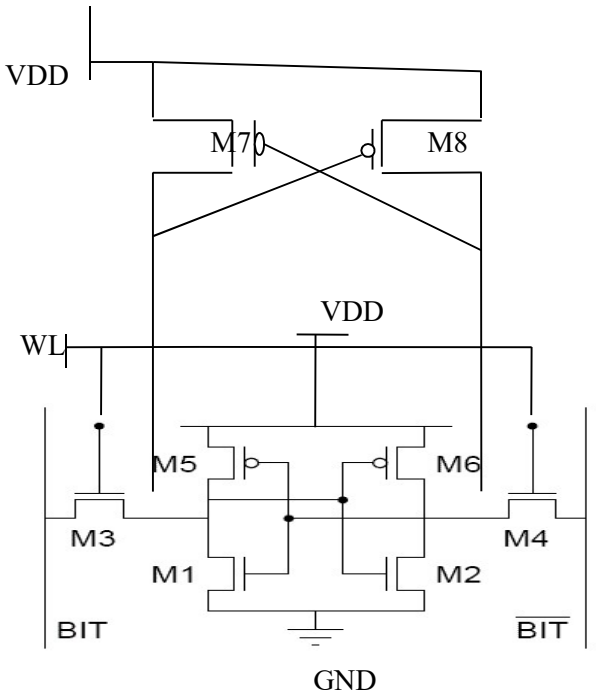


Fig.9.1 Proposed 8T SRAM Cell [14]

8. Standard 8¢ -SRAM Cell

The standard 8T-SRAM Cell in shown in Fig.10.1. That's Seen, the read and write cycles use different wordlines and bitlines. Note that the standard 8T SRAM cell uses a single-ended read scheme which reduces the swing of bitlines. That's 8T-SRAM cell provides significantly improved RSNM (similar to Hold Static Noise Margin (HSNM) of the standard 6T-SRAM cell) with similar access time, write time, and write margin [17].

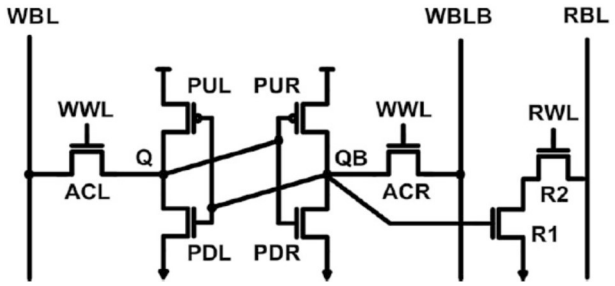


Fig.10.1 STANDARD 8T-SRAM CELL [17]

9. Simulation and Results

Analysis of proposed 8T SRAM cell in terms of write ability, read stability and hold static noise has been carried out in this section. These results are compared with standard 6T and 8T SRAM cell. The circuit is characterized by using the 180nm Technology with the supply voltage of 1.2 volt.

9.1. Hold Stability

Static noise margin (SNM) is the most common approach to measure hold stability and read stability of the cell. Hold stability is calculated when the SRAM cell is in hold state.

In hold state the word lines are off, so the cell is totally disconnected from the bit lines. SNM defines the largest noise that can be imposed to the storage nodes before flipping the content of the cell. Fig.11.1, 11.2 and 11.3 shows the hold static noise margin of 6T, Proposed 8T and standard 8T SRAM cells respectively.

9.2. Read Stability

The Read stability is measured by read static noise margin (RSNM) in SRAM Cell. In the proposed 8T SRAM cell due to storing nodes isolation we get better RSNM comparable to conventional 6T SRAM and standard 8T SRAM Cells. Fig. 11.4, 11.5 and 11.6 represents the read stability of 6T SRAM and proposed 8T and standard 8T SRAM cells respectively.

9.3. Write Stability

The Write stability is measured by write static noise margin (WSNM). In the proposed 8T SRAM cell due to storing nodes isolation we get better WSNM comparable to conventional 6T SRAM and standard 8T SRAM Cells. Fig. 11.7, 11.8 and 11.9 represents the write stability of 6T SRAM and proposed 8T and standard 8T SRAM cells respectively.

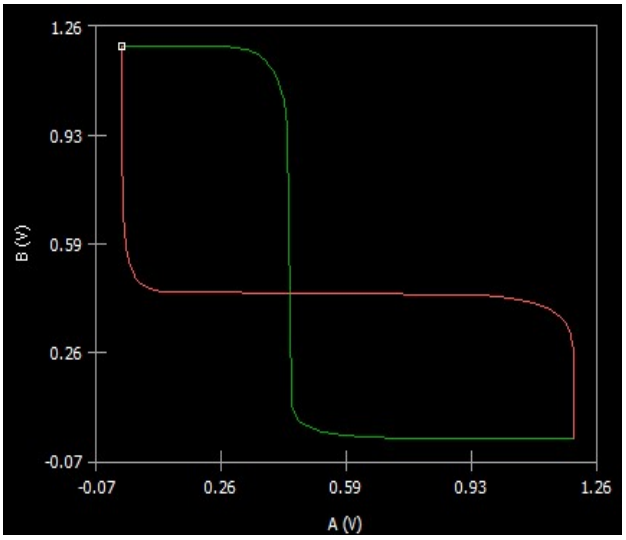


Fig.11.1 HSNM 6T SRAM CELL

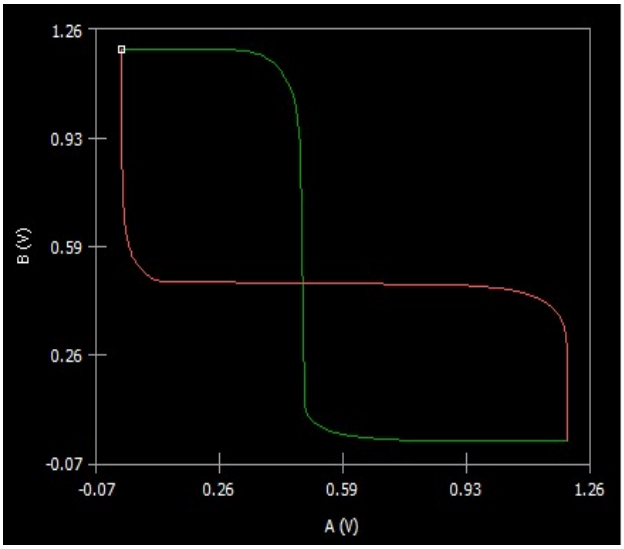


Fig.11.2 HSNM PROPOSED 8T SRAM CELL

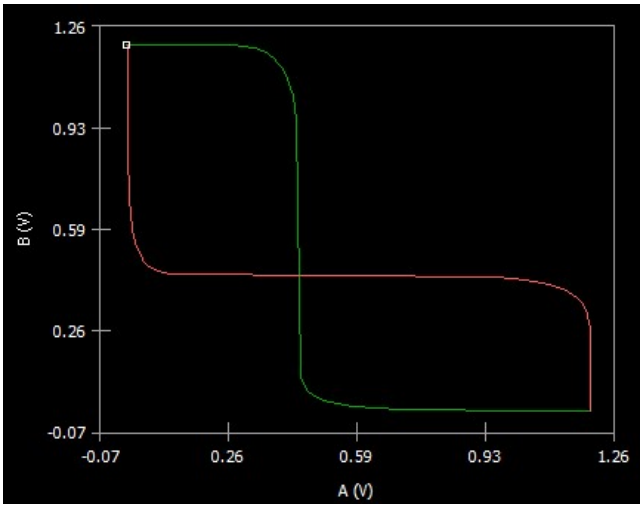


Fig.11.3 HSNM STANDARD 8T SRAM CELL

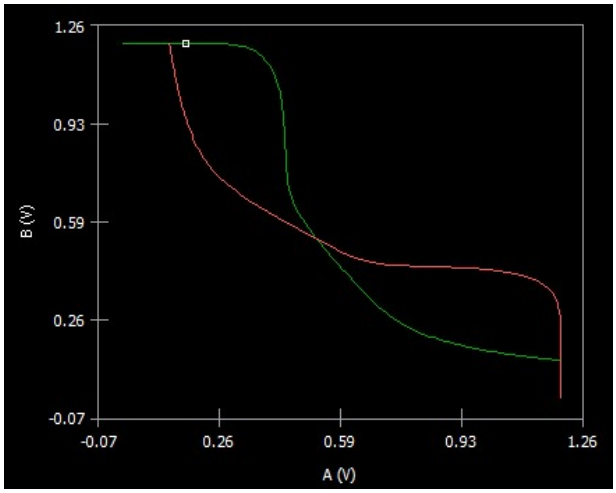


Fig.11.4 RSNM 6T SRAM CELL

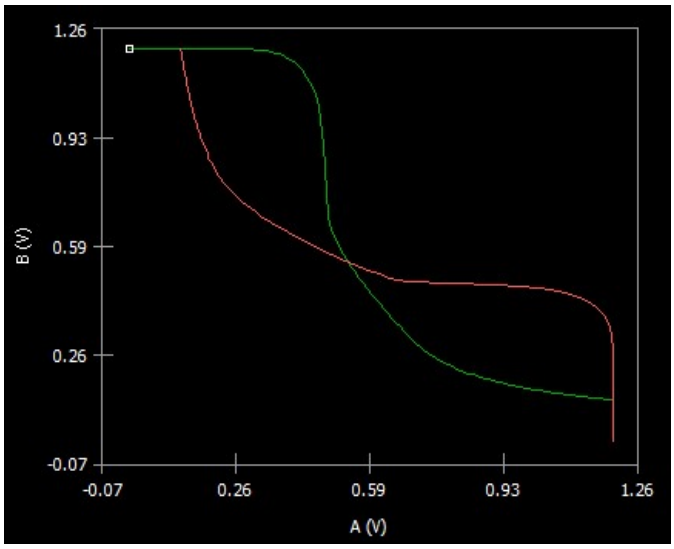


Fig.11.5 RSNM PROPOSED 8T SRAM CELL

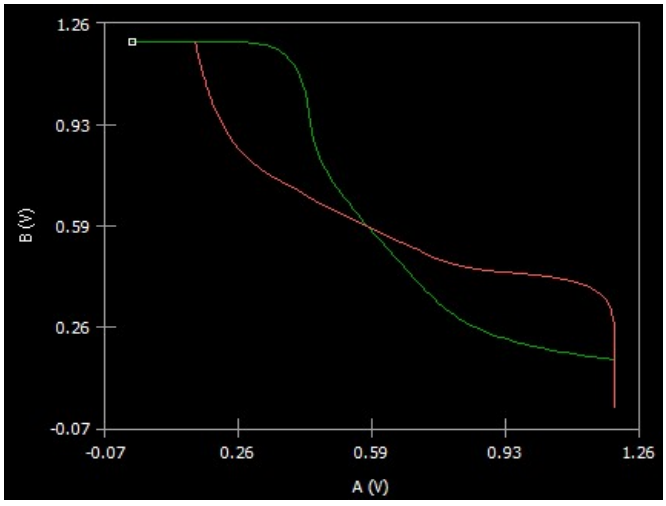


Fig.11.6 RSNM STANDARD 8T SRAM CELL

Table 11.1: Comparison of Hold SNM and Read SNM

CELL	Read SNM (in volts)	Hold SNM (in volts)
6T SRAM	0.0711	0.125
PROPOSED 8T SRAM	0.1000	0.125
STANDARD 8T SRAM	0.0999	0.125

Write Trip point:- Write trip point is the measure of write ability of the cell. It shows how difficult it is to the storing nodes of the cell.

The bit-line voltage is swept from 0 to Vdd, and the flipping of the cell, when Q and Q bar flip their their content is captured. The value of bit-line voltage at the crossing point of internal storage nodes Q and QB bar represents write trip point.

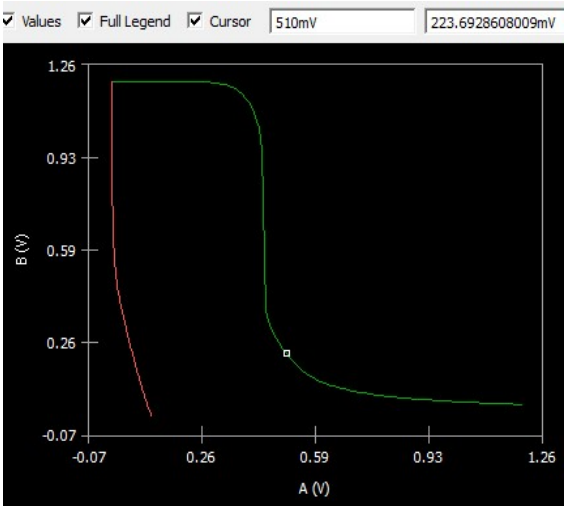


Fig.11.7 6T SRAM Write Trip Point

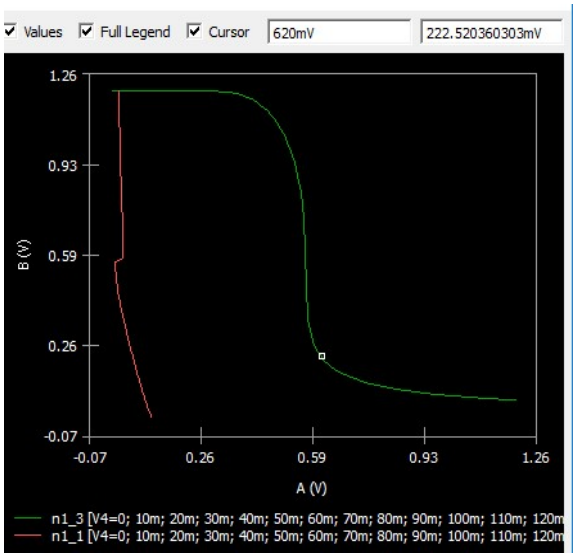


Fig.11.8 PROPOSED 8T SRAM Write Trip Point

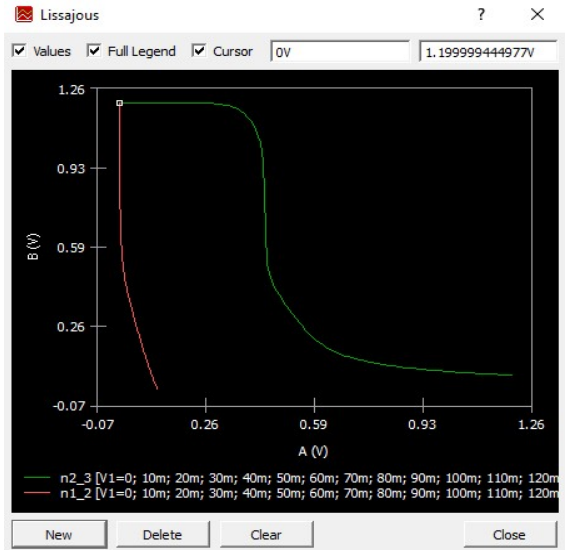


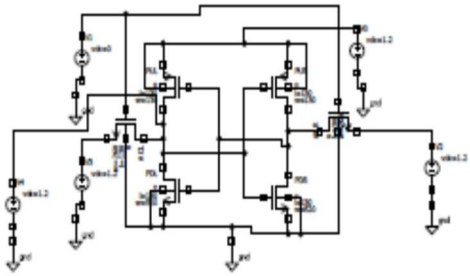
Fig.11.9 STANDARD 8T SRAM Write Trip Point

Table 11.2: Comparison for write trip point of 6T SRAM and Standard 8T and proposed 8T SRAM cells

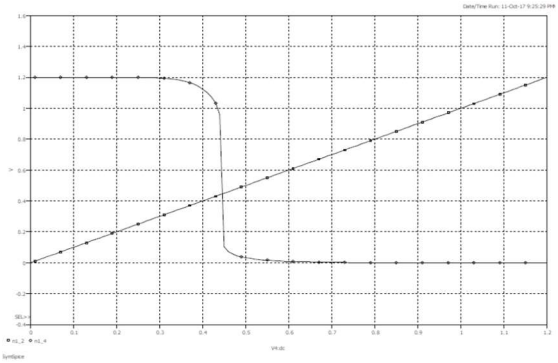
CELL	Write trip point
6T SRAM	900mv
PROPOSED 8T SRAM	675mv
STANDARD 8T SRAM	726mv

10. Simulation Results and DC Analysis

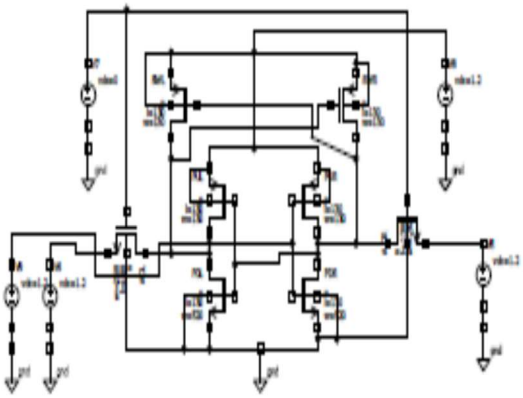
12.a 6T SRAM cell output



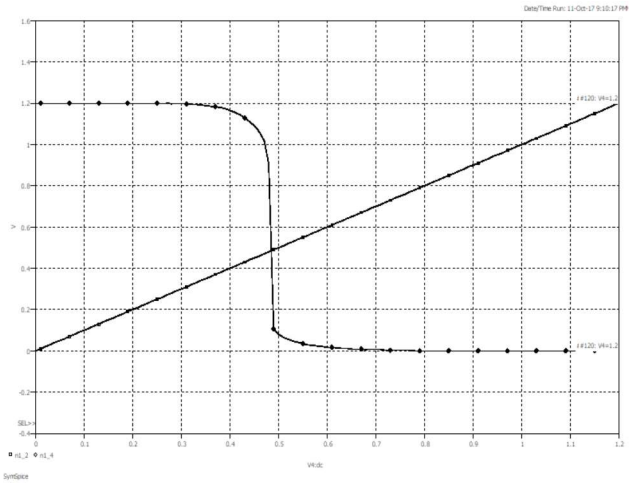
12.b 6T SRAM cell DC analysis



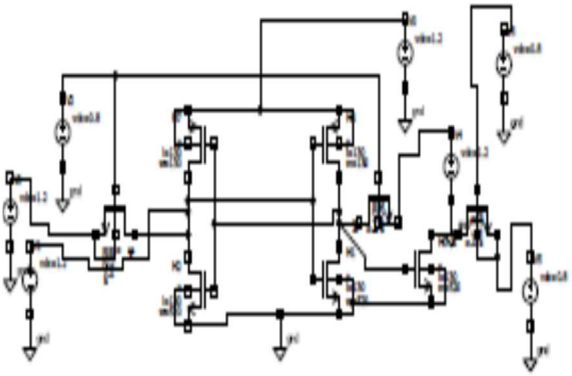
12.C PROPOSED 8T SRAM CELL OUTPUT



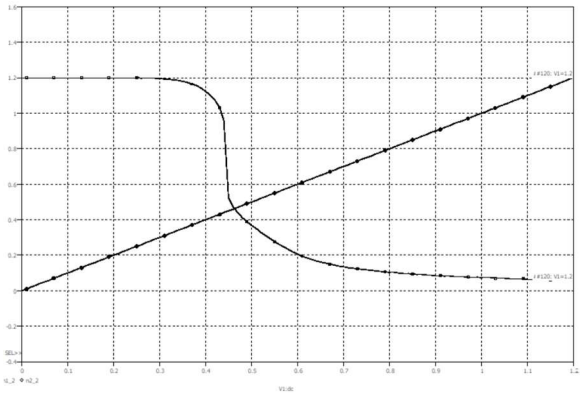
12.D PROPOSED 8T SRAM CELL DC ANALYSIS



12.e STANDARD 8T SRAM CELL OUTPUT



12.f. STANDARD 8T SRAM cell DC analysis



11. Conclusion

A low power and swing node restoration Static Random Access memory logic circuit technique is presented in the paper. In this paper comparative analysis of 6T and 8T SRAM cells in 180nm Technology is also presented.

This is the proposed SRAM cell and Dual node voltage with Swing Restoration logic perform D.C. analysis Hold mode operation. D.C. analysis HOLD operation good noise margin proposed 8T SRAM cell is better than 6T SRAM and STANDARD 8T SRAM Cells. This conclusion is good for power consumption is low. Then PROPOSED 8T SRAM Cell Write mode is power analysis is better Then 6T SRAM and STANDARD 8T SRAM Cells. Then speed is higher for proposed 8T SRAM Cell.

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